



UR6511

Preliminary

LINEAR INTEGRATED CIRCUIT

**2A DDR BUS TERMINATION
REGULATOR**

■ **DESCRIPTION**

The **UR6511** is a linear regulator providing up to 2A transient current sourcing and sinking capability for DDR bus terminator applications while regulating an output voltage to within 20mV. It contains a high speed operational amplifier which provides fast load transient response and only requires 10uF of ceramic output capacitance.

The **UR6511** output termination voltage tracks the reference voltage applied at V_{REF} pin. A resistor divider connected to V_{IN} , GND and V_{REF} pins is used to force the reference voltage to V_{REF} pin. Additional features include current limiting protection and thermal shutdown protection.

■ **FEATURES**

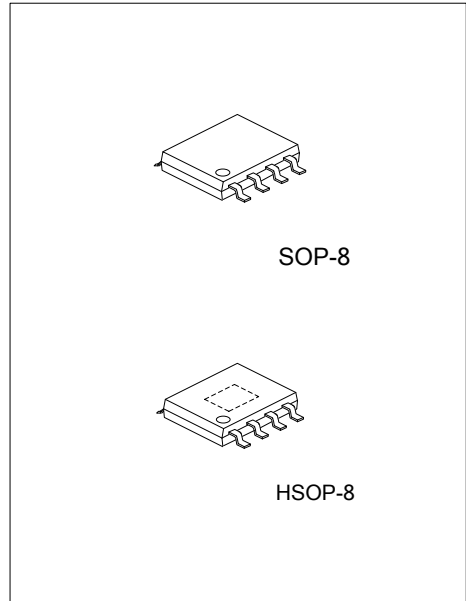
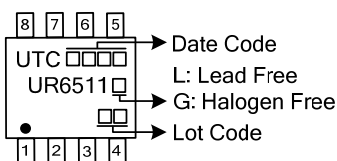
- *DDR1/ DDR2/DDR3/Low Power DDR3 termination voltage applications
- *Sink and Source Current: 2A
- *Low output voltage offset within 20mV
- *Adjustable output voltage by external resistors
- *Integrated power MOS devices
- *Suspend to RAM(STR) functionality
- *Current Limiting Protection
- *Thermal Shutdown Protection
- *Cost-effective and easy to use

■ **ORDERING INFORMATION**

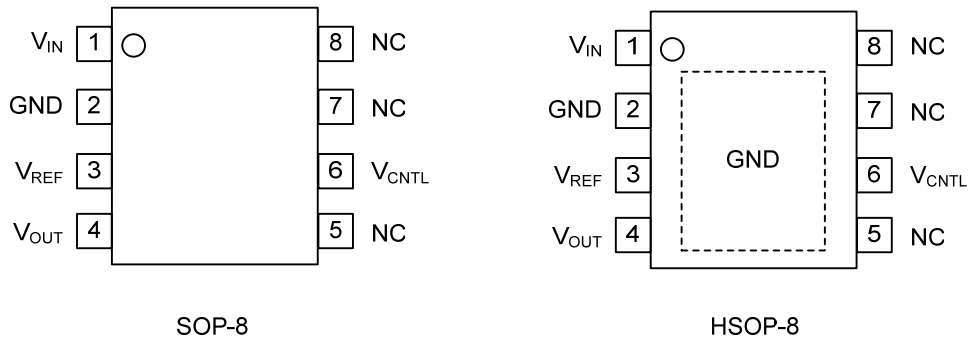
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UR6511L-S08-R	UR6511G-S08-R	SOP-8	Tape Reel
UR6511L-SH2-R	UR6511G-SH2-R	HSOP-8	Tape Reel

<p>UR6511G-S08-R</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S08: SOP-8, SH2: HSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ **MARKING**



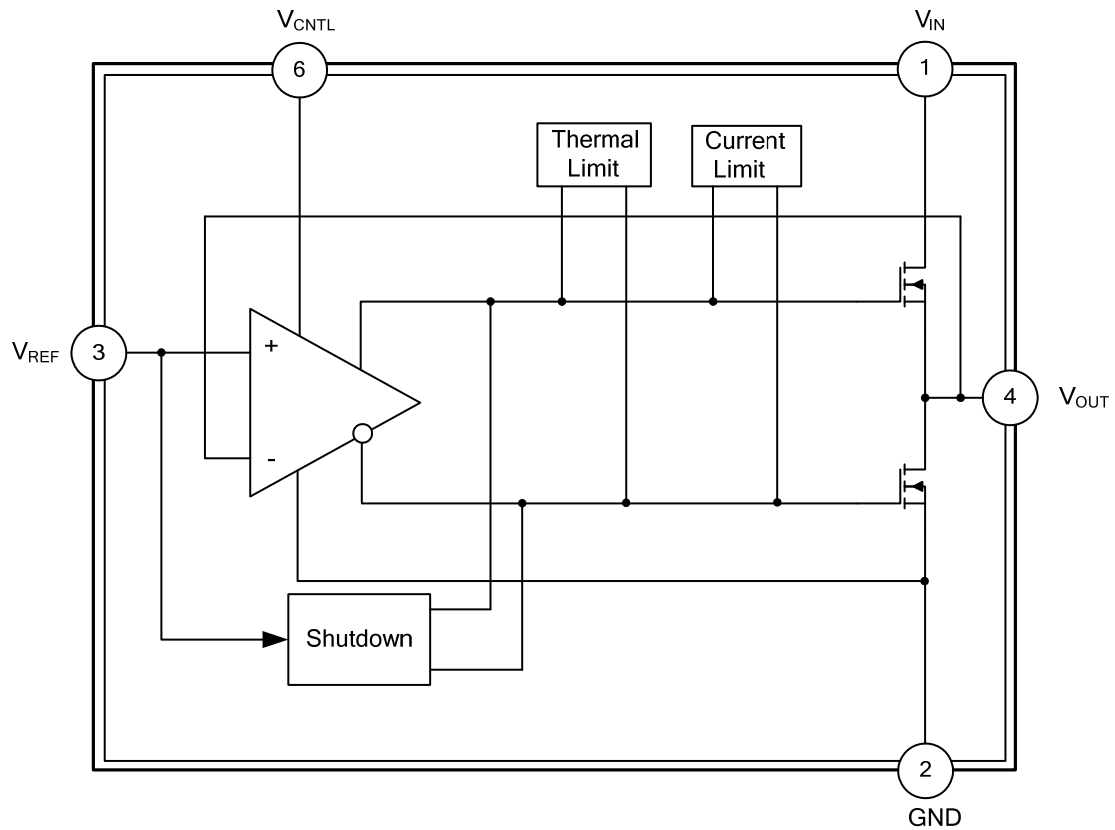
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

No.	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	V _{IN}	I	Power supply pin for the V _{OUT} output
2	GND	O	Ground pin
3	V _{REF}	I	Reference voltage input and active-low shutdown control pin
4	V _{OUT}	O	Output voltage pin
5, 7, 8	NC		
6	V _{CNTL}	I	Power supply pin for the internal control circuits

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V _{CNTL} Control Voltage	V _{CNTL}	7	V
V _{IN} Supply Voltage	V _{IN}	7	V
Power Dissipation (T _A =25°C)	P _D	0.87	W
Junction Temperature	T _J	+150	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ _{JA}	143	°C/W
Junction to Case	θ _{JC}	45	°C/W

■ RECOMMENDED OPERATING CONDITIONS (Note)

PARAMETER	SYMBOL	RATINGS	UNIT
V _{CNTL} Control Voltage	V _{CNTL}	3.0 ~ 5.5	V
V _{IN} Supply Voltage	V _{IN}	1.0 ~ 5.5	V
Junction Temperature	T _J	-40 ~ +125	°C
Ambient Temperature	T _A	-40 ~ +85	°C

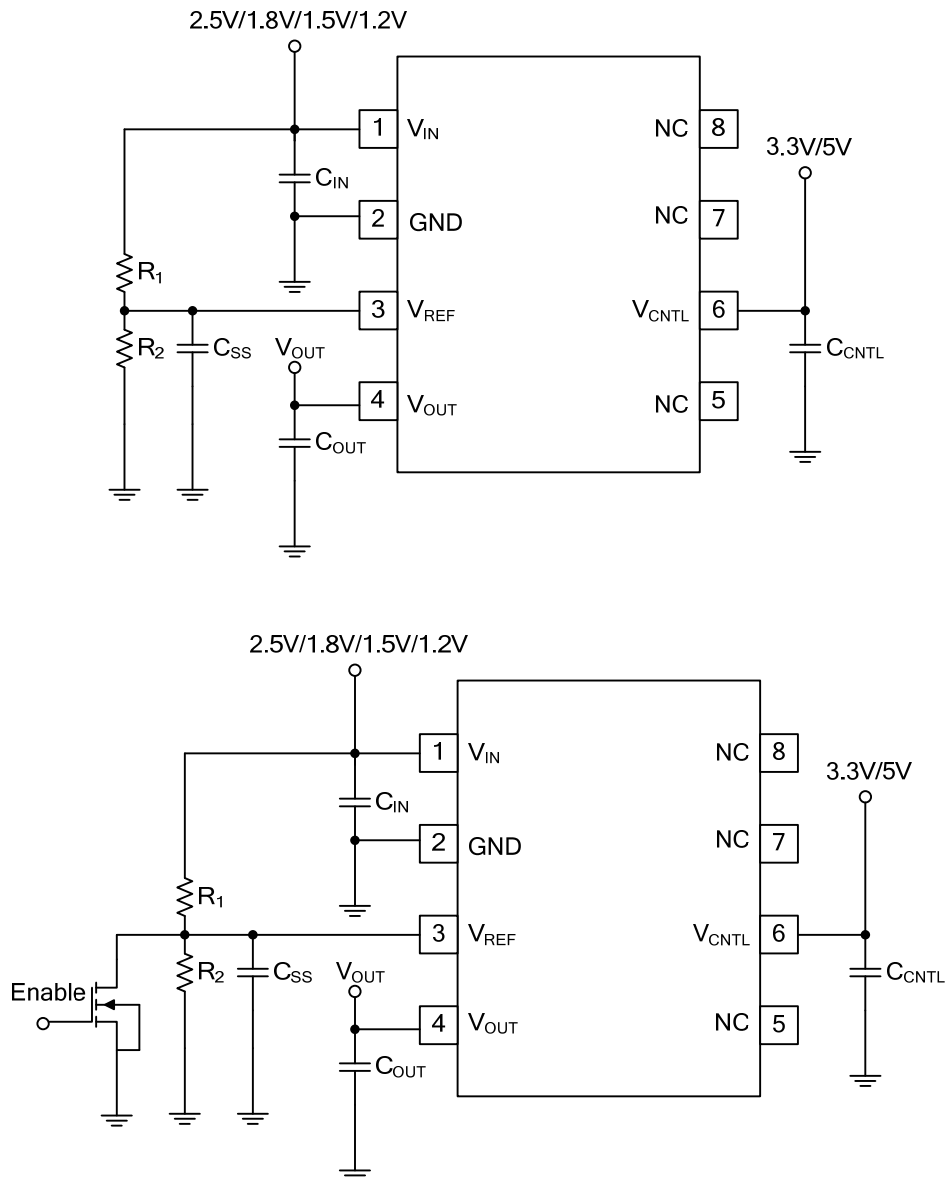
Note: All voltage values are with respect to the network ground terminal unless otherwise noted.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

(V_{IN}=2.5V/1.8V/1.5V, V_{CNTL}=3.3V/5V, V_{REF}=1.25V/0.9V/0.75V, C_{OUT} = 10μF (Ceramic))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
Operation Current of V _{CNTL}	I _{CNTL}	I _{OUT} = 0A, V _{CNTL} = 5V		0.7	1.5	mA
Standby Current	I _{STB}	V _{REF} < 0.15V, V _{CNTL} = 5V		30	50	μA
OUTPUT VOLTAGE (DDR/DDR II/DDR III)						
Output Voltage Offset (V _{REF} -V _{OUT})	V _{OS}	I _{OUT} = 0A	-10		10	mV
Load Regulation	ΔV _{LOAD}	I _{OUT} = ±2A	-20		20	mV
PROTECTION						
Current Limit	I _{LIMIT}		2			A
Thermal Shutdown Temperature	T _{SD}	V _{CNTL} = 3.3V~5V		165		°C
Thermal Shutdown Hysteresis	ΔT _{SD}	V _{CNTL} = 3.3V~5V		30		°C
V_{REF} Shutdown						
Shutdown Threshold	V _{IH}	Enable	0.4			V
	V _{IL}	Shutdown			0.15	V

■ TYPICAL APPLICATIONS CIRCUITS



$R_1=R_2=1\text{K}\Omega\sim 5\text{K}\Omega$, $C_{\text{OUT}}=10\mu\text{F}$ (Ceramic)under the worst case testing condition

$C_{\text{SS}}=0.1\mu\text{F}$ to $1\mu\text{F}$, $C_{\text{IN}}=10\mu\text{F}$ (Low ESR), $C_{\text{CNTL}}=0.1\mu\text{F}$

$$V_{\text{REF}} = \frac{R_2}{R_1 + R_2} V_{\text{IN}}(\text{V}), V_{\text{OUT}} \text{ track } V_{\text{REF}}$$

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