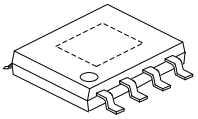
UR6517 *LINEAR INTEGRATED CIRCUIT*

1.8A DDR BUS TERMINATION REGULATOR



HSOP-8

■ DESCRIPTION

The **UR6517** is a linear regulator providing up to 1.8A transient current sourcing and sinking capability for DDR bus terminator applications while regulating an output voltage to within 20mV. It contains a high speed operational amplifier which provides fast load transient response and only requires 10uF of ceramic output capacitance.

The **UR6517** output termination voltage tracks the reference voltage applied at V_{REF} pin. A resistor divider connected to V_{IN}, GND and V_{REF} pins is used to force the reference voltage to V_{REF} pin. Additional features include current limiting protection and thermal shutdown protection.

■ FEATURES

*DDR1/ DDR2/DDR3/DDR4 termination voltage applications
*Sink and Source Current
  DDR2 1.8A Sink/Source @ V_{IN}=1.8V
  DDR3 1.5A Sink/Source @ V_{IN}=1.5V
  LPDDR3 1.2A Sink/Source @ V_{IN}=1.35V
  DDR4 1.2A Sink/Source @ V_{IN}=1.2V
*Low output voltage offset within 20mV
*Adjustable output voltage by external resistors
*Integrated power MOS devices
*Suspend to RAM(STR) functionality
*Current Limiting Protection
*Thermal Shutdown Protection
*Cost-effective and easy to use

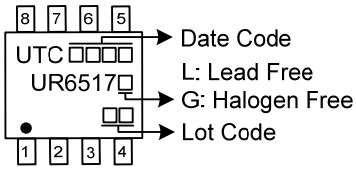
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UR6517L-SH2-R	UR6517G-SH2-R	HSOP-8	Tape Reel

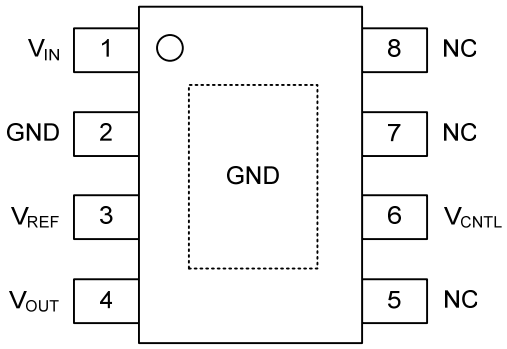
UR6517G-SH2-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) SH2: HSOP-8
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



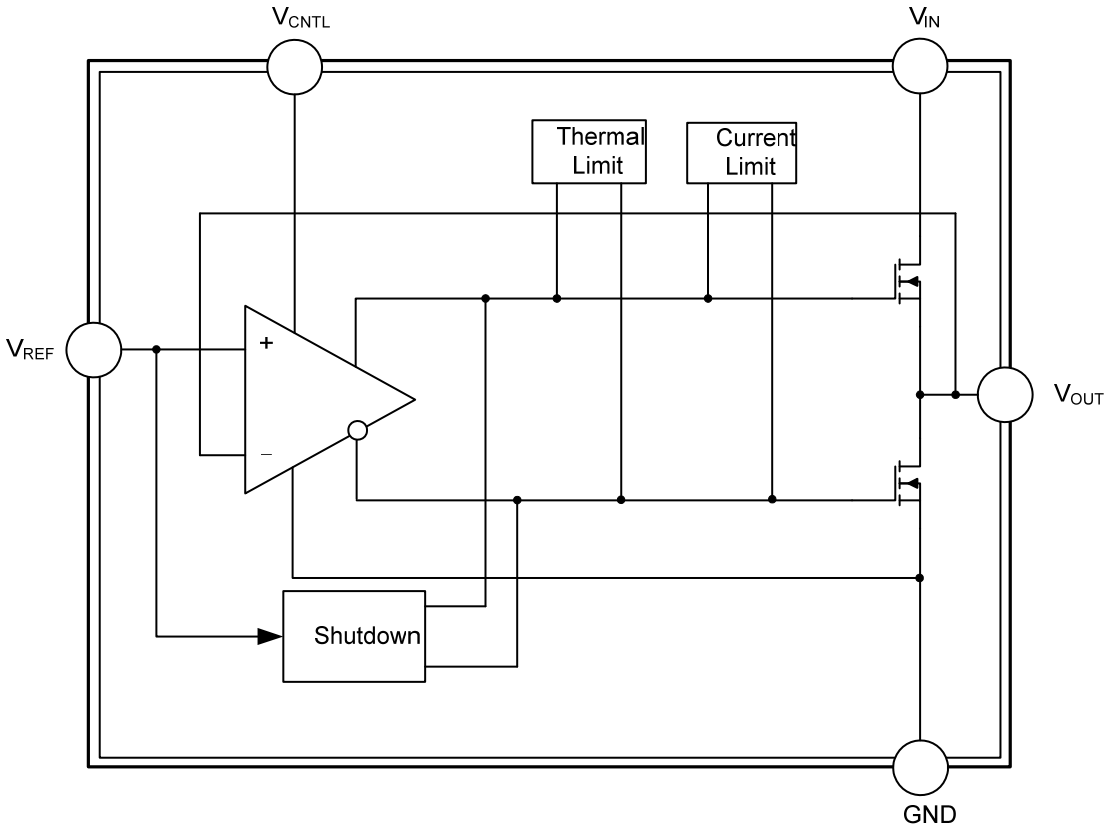
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN NO	PIN NAME	PIN DESCRIPTION
6	V_{CNTL}	Power supply pin for the internal control circuits
2	GND	Ground pin
1	V_{IN}	Power supply pin for the V_{OUT} output
3	V_{REF}	Reference voltage input and active-low shutdown control pin
4	V_{OUT}	Output voltage pin
5, 7, 8	NC	No connect
Exposed Pad	GND	Connect exposed pad to GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{CNTL} Control Voltage	V_{CNTL}	-0.3 ~ +6	V
V_{IN} Supply Voltage	V_{IN}	-0.3 ~ +6	V
Power Dissipation (T_A=25°C)	P_D	1.163	W
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Maximum Junction to Ambient (Note)	θ_{JA}	86	°C/W
Maximum Junction to Case	θ_{JC}	15	°C/W

Note: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

■ RECOMMENDED OPERATING CONDITIONS (Note)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{CNTL} Control Voltage	V_{CNTL}	5±5%	V
V_{IN} Supply Voltage	V_{IN}	1.0 ~ 5.5	V
Ambient Temperature	T_A	-40 ~ +85	°C
Junction Temperature	T_J	-40 ~ +125	°C

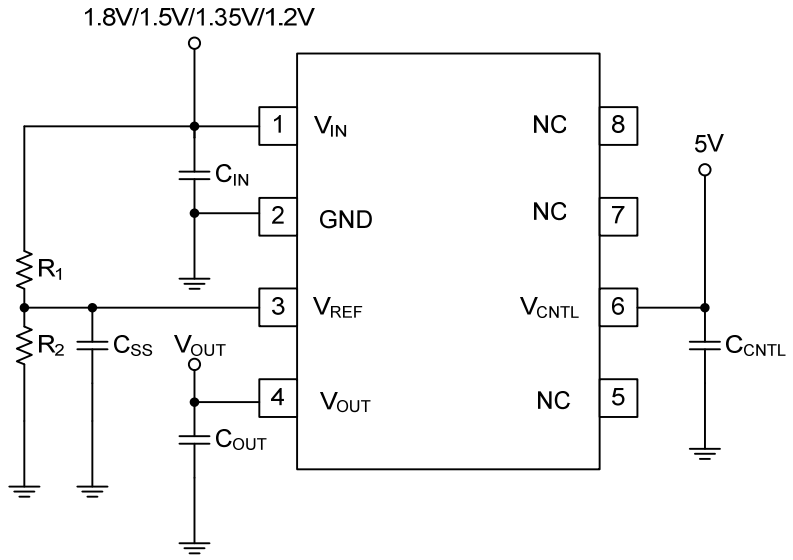
Note: All voltage values are with respect to the network ground terminal unless otherwise noted.

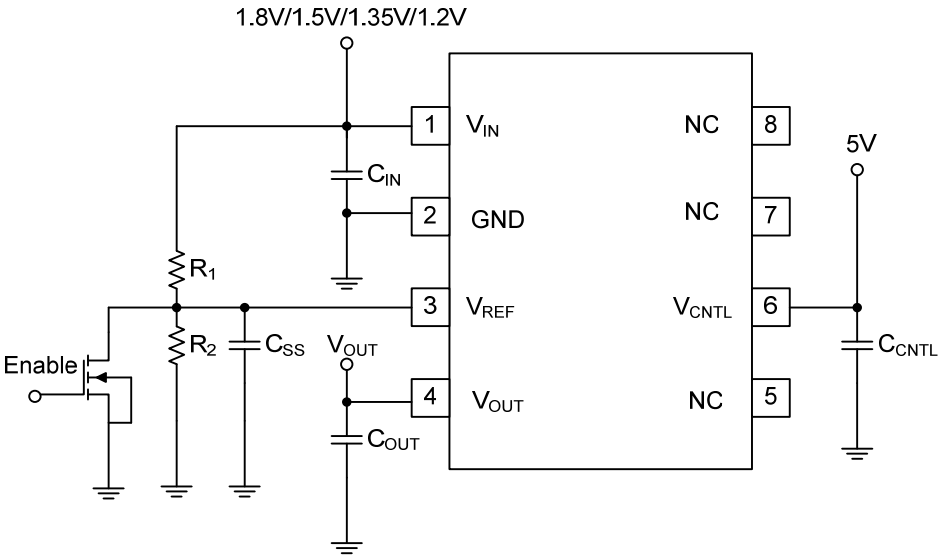
■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

(V_{IN}=1.8V/1.5V, V_{CNTL}=5V, V_{REF}=0.9V/0.75V, C_{OUT} = 10μF (Ceramic))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
Operation Current of V_{CNTL}	I_{CNTL}	I_{OUT} =0A		0.7	2.5	mA
V_{CNTL} Power On Reset	V_{POR}	V_{CNTL} Rising		3.6		V
Standby Current	I_{STB}	V_{REF}<0.2V, R_{LOAD}=180Ω		20	90	μA
OUTPUT VOLTAGE (DDR/DDR II/DDR III)						
Output Voltage Offset (V_{REF}-V_{OUT})	V_{OS}	I_{OUT} =0A	-20		20	mV
Load Regulation	ΔV_{LOAD}	V_{IN}=1.8V,I_{OUT} =±1.8A	-20		20	mV
		V_{IN}=1.5V,I_{OUT} =±1.5A				
		V_{IN}=1.35V,I_{OUT} =±1.2A				
		V_{IN}=1.2V,I_{OUT} =±1.2A				
PROTECTION						
Current Limit	I_{LIMIT}	V_{IN}=1.8V/1.5V		2.5		A
Short Circuit Current	I_{SHORT}	V_{IN}=1.8V/1.5V/1.35V/1.2V V_{OUT} <0.2V		1.5		A
Thermal Shutdown Temperature	T_{SD}	V_{CNTL}=5V	125	170		°C
Thermal Shutdown Hysteresis	ΔT_{SD}	V_{CNTL}=5V		35		°C
V_{REF} Shutdown						
Shutdown Threshold	V_{IH}	Enable	0.4			V
	V_{IL}	Shutdown			0.15	V

■ TYPICAL APPLICATIONS CIRCUITS





R1=R2=100KΩ, C_{OUT}=10μF(Ceramic)under the worst case testing condition
C_{SS}=1nF to 0.1μF, C_{IN}=10μF(Low ESR), C_{CNT}L=1μF

$$V_{REF} = \frac{R_2}{R_1 + R_2} V_{IN}(V)$$, V_{OUT} track V_{REF}

■ FUNCTIONAL PIN DESCRIPTION

V_{IN}

Input voltage which supplies current to the output pin. Connect this pin to a well-decoupled supply voltage. To prevent the input rail from dropping during large load transient, a large, low ESR capacitor is recommended to use. The capacitor should be placed as close as possible to the V_{IN} pin.

GND (Exposed Pad)

Common Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

V_{CNTL}

VCNTL supplies the internal control circuitry and provides the drive voltage. The driving capability of output current is proportioned to the V_{CNTL}. Connect this pin to 5V bias supply to handle large output current with at least 1μF capacitor from this pin to GND. An important note is that V_{IN} should be kept lower or equal to V_{CNTL}.

REFEN

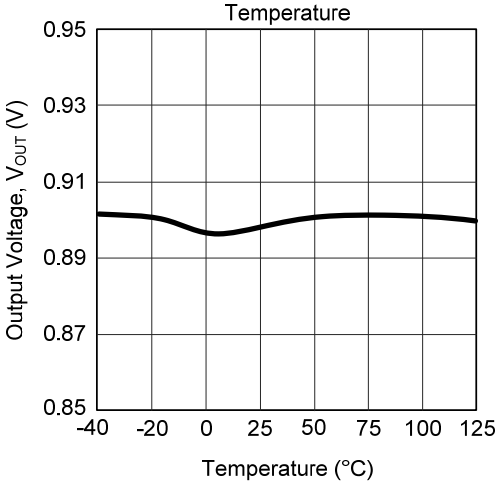
Reference voltage input and active low shutdown control pin. Two resistors dividing down the V_{IN} voltage on this pin to create the regulated output voltage. Pulling this pin to ground turns off the device by an open-drain, such as 2N7002, signal N-MOSFET.

V_{OUT}

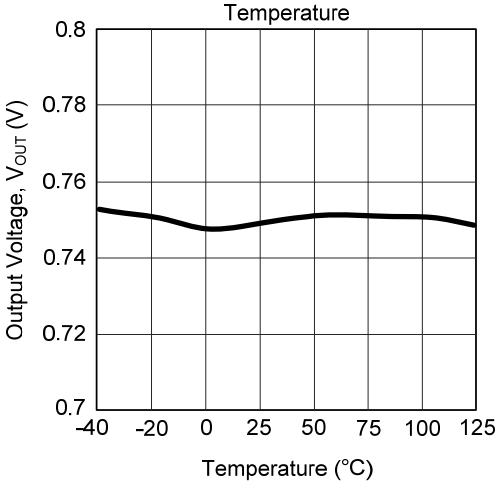
Regulator output. V is regulated to REFEN voltage that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output rail. To maintain adequate large signal transient response, typical value of 10μF ceramic capacitors are recommended to reduce the effects of current transients on V_{OUT}.

■ TYPICAL CHARACTERISTICS

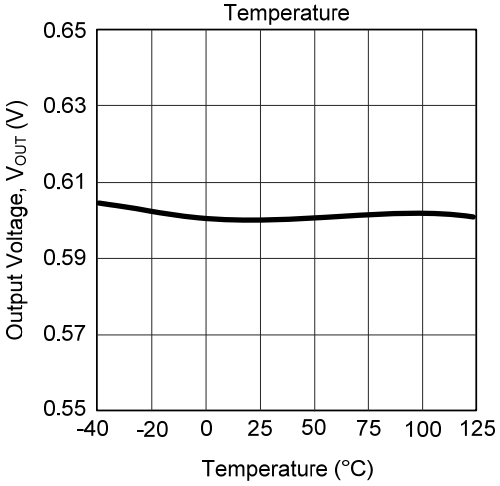
DDR II Output Voltage vs. Temperature



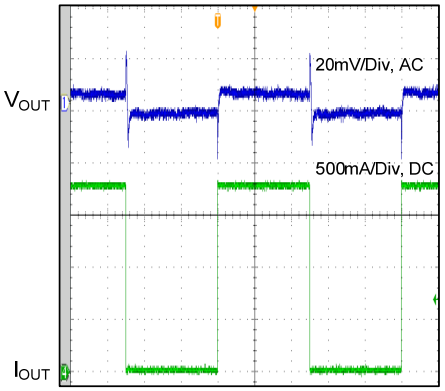
DDR III Output Voltage vs. Temperature



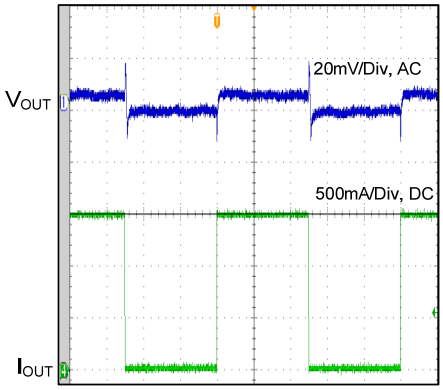
Low-V DDR III Output Voltage vs. Temperature



$0.9V_{TT}$ @ 1.8A Transient Response
V_{IN}=1.8V, V_{REF}=0.9V, V_{CTRL}=5V



$0.75V_{TT}$ @ 1.5A Transient Response
V_{IN}=1.5V, V_{REF}=0.75V, V_{CTRL}=5V



$0.6V_{TT}$ @ 1.2A Transient Response
V_{IN}=1.2V, V_{REF}=0.6V, V_{CTRL}=5V