4-Output Ultra-Low Additive Jitter Differential Clock Buffer/Level Translator

US5D304
Datasheet

Description

The US5D304 is a 2.1-GHz,4-output differential high-performance clock fanout buffer.

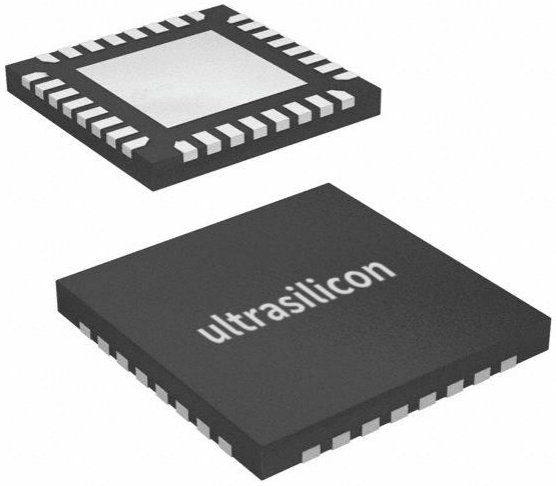
The input clock can be selected from two differential inputs or one crystal input. The selected input clock is distributed to two banks of 2 differential outputs and one LVCMOS output. Output banks can be configured as LVPECL,LVDS,or HCSL drivers,or disabled.The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The outputs are at a defined level when inputs are open.

The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by a single-ended clock.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

Applications

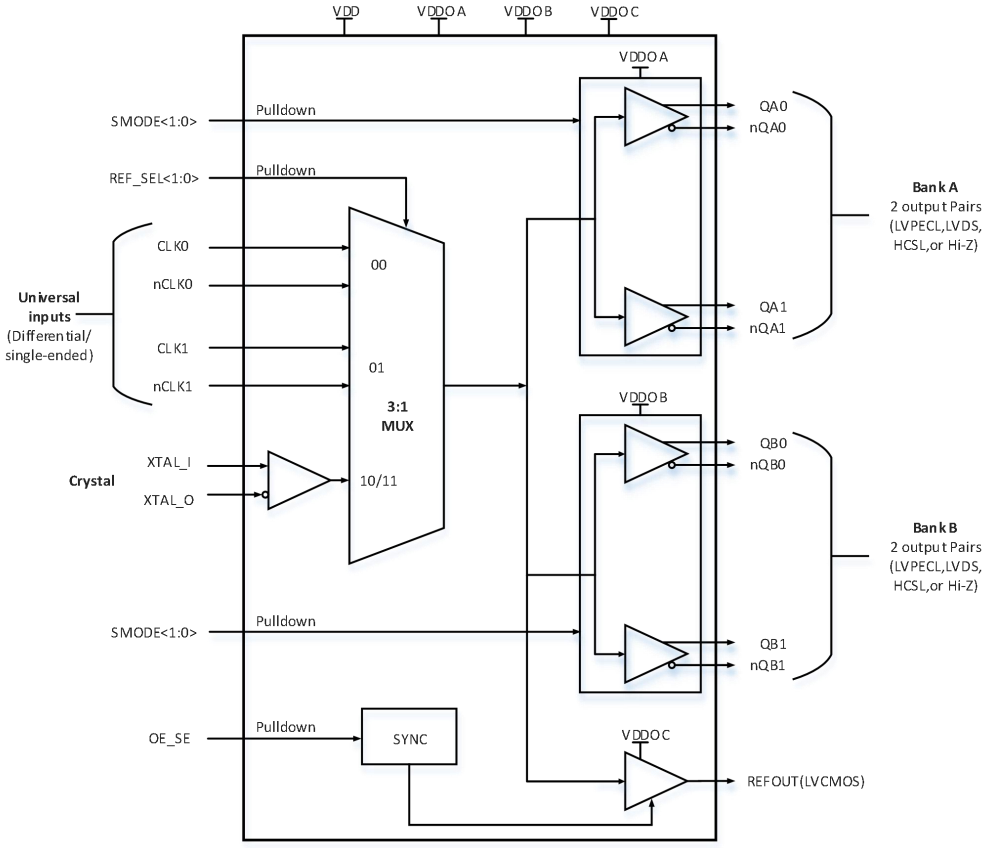
- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0)
- Remote Radio Units and Baseband Units



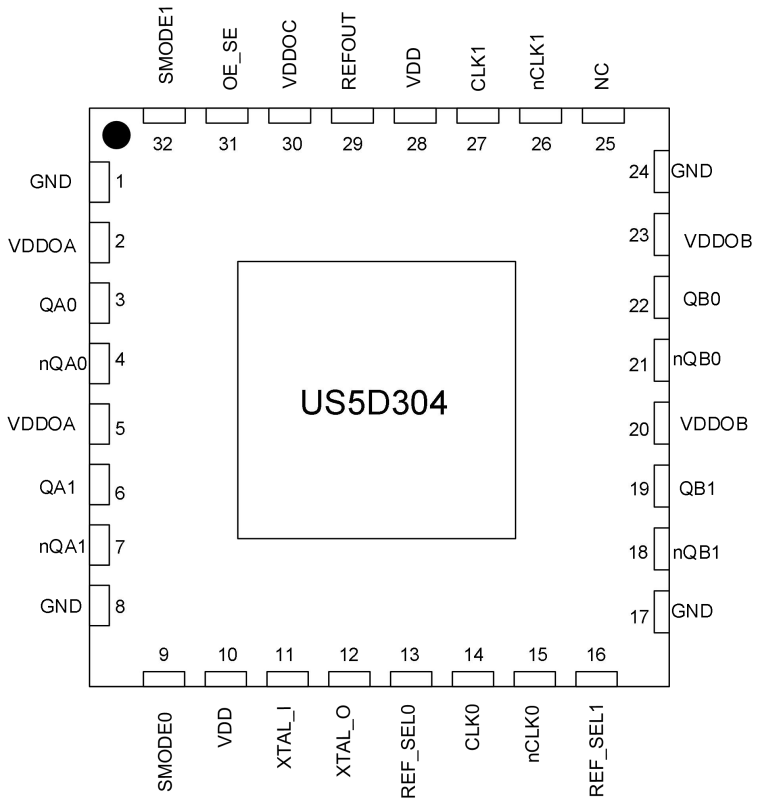
Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL, HSTL or Single Ended
- Crystal Input accepts 10MHz to 40MHz Crystal or Single Ended Clock
- Maximum Output Frequency
  LVPECL - 2.1GHz
  LVDS - 2.1GHz
  HCSL - 250MHz
  LVCMOS - 250MHz
- Four differential output pairs that can be configured as LVPECL or LVDS or HCSL or HiZ
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: 20ps (typical)
- Part-to-part skew: 200ps (typical)
- Additive RMS phase jitter @ 156.25MHz:
  12.5 fs RMS (10kHz - 1 MHz), typical @ 3.3V/ 3.3V
  50.5 fs RMS (10kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage modes:
  V_{DD}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- Industrial Temperature Range:-40°C to 85°C
- Pin-to-Pin compatible with lmk00304
- Available in a 32-pin,5mm*5mm WQFN package

Block Diagram



Pin Assignment for 5mm x 5mm 32-Lead WQFN Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions[1]

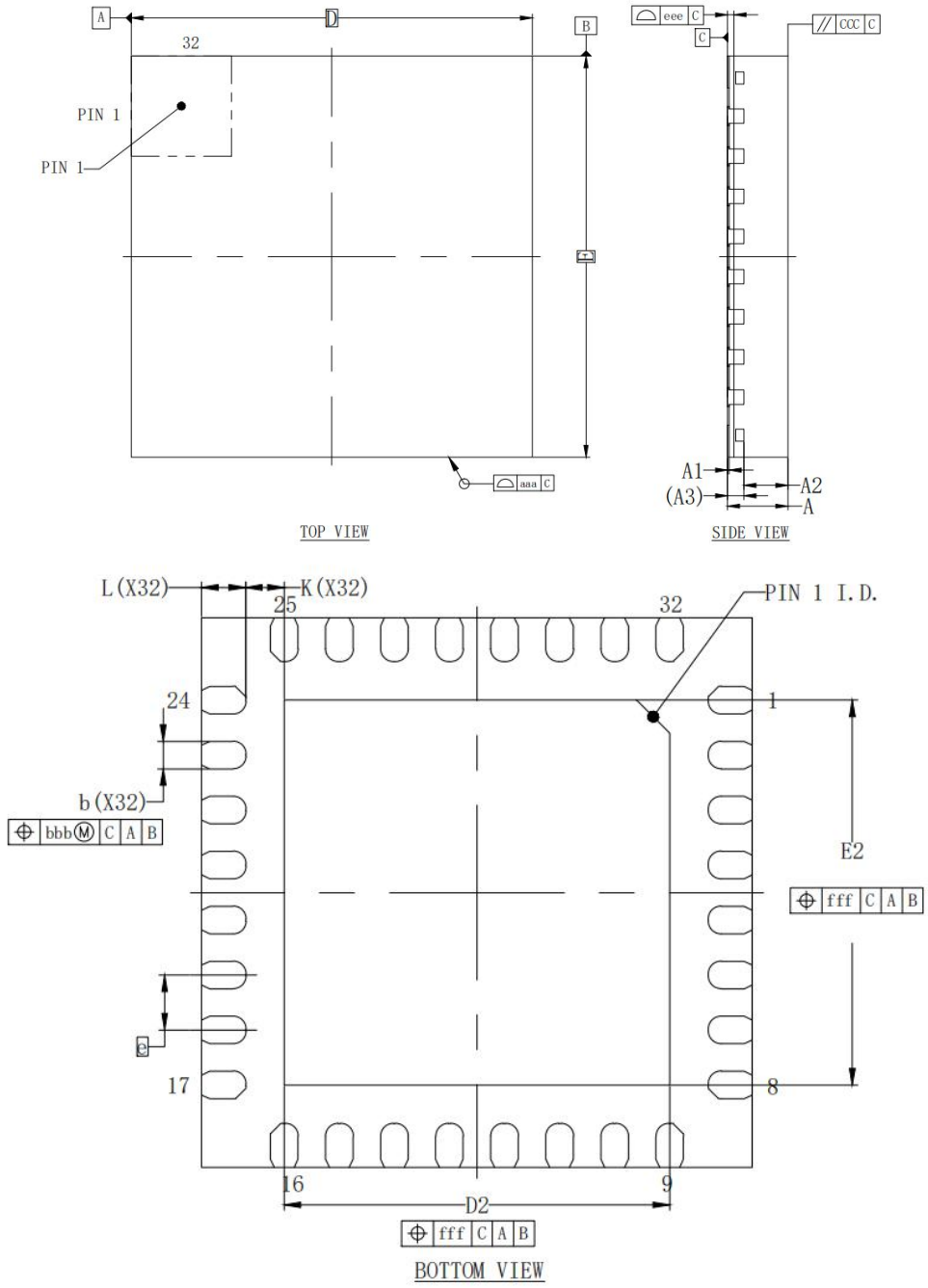
Number	Name	Type		Description
1	GND	Power		Ground.
2	V_{DDOA}	Power		Output supply pins for Bank QA outputs. 3.3V or 2.5V.
3	QA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
4	nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5	V_{DDOA}	Power		Output supply pins for Bank QA outputs. 3.3V or 2.5V.
6	QA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
7	nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
8	V_{DDOA}	Power		Output supply pins for Bank QA outputs. 3.3V or 2.5V.
9	SMODE0	Input	Pulldown	Output driver select for Bank A outputs. See Table 8 for function. LVCMOS/LVTTL interface levels.
10	V_{DD}	Power		Power supply for Core and input Buffer blocks, 3.3V or 2.5V.
11	XTAL_I	Input		Crystal oscillator interface.
12	XTAL_O	Input		Crystal oscillator interface.
13	REF_SEL0	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function.
14	CLK0	Input	Pulldown	Non-inverting differential clock. Internally biased to ground.
15	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internally biased to $0.5V_{DD.}$
16	REF_SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function.
17	GND	Power		Ground.
18	nQB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
19	QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
20	V_{DDOB}	Power		Output supply pins for Bank QB outputs. 3.3V or 2.5V.
21	nQB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
22	QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
23	V_{DDOB}	Power		Output supply pins for Bank QB outputs. 3.3V or 2.5V.
24	GND	Power		Ground.
25	nc	Unused		No connect pin.
26	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock. Internally biased to $0.5V_{DD.}$
27	CLK1	Input	Pulldown	Non-inverting differential clock. Internally biased to ground.
28	V_{DD}	Power		Power supply for Core and input Buffer blocks, 3.3V or 2.5V.
29	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels.
30	VDDOC	Power		Output supply pin for REFOUT output.
31	OE_SE	Input	Pulldown	REFOUT output enable. LVCMOS/LVTTL interface levels. See Table 4.
32	SMODE1	Input	Pulldown	Output driver select for Bank A outputs. See Table 8 for function. LVCMOS/LVTTL interface levels.

NOTE 1. *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2: Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OE_SE, SMODE[1:0], REF_SEL[1:0]			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				50		kΩ
R_{PULLUP}	Input Pullup/down Resistor	nCLK0			40/40		kΩ
		nCLK1			40/40		kΩ
C_{PD}	Power Dissipation Capacitance	REFOUT	VDDOC = 3.465V		5.3		pF
		REFOUT	VDDOC = 2.625V		6.3		pF
R_{OUT}	Output Impedance	REFOUT	VDDOC = 3.3V		50		Ω
		REFOUT	VDDOC = 2.5V		60		Ω

PACKAGE DIMENSIONS

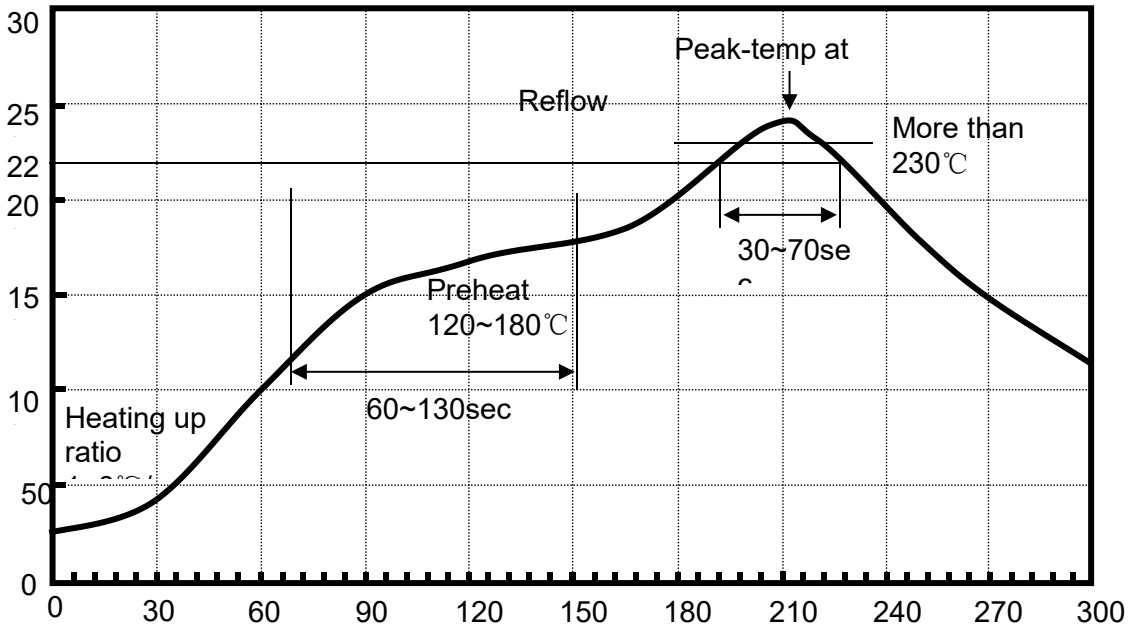


Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		5.0 BSC	
	Y	E		5.0 BSC	
Exposed Pad Size	X	D2	3.40	3.50	3.60
	Y	E2	3.40	3.50	3.60
Total Thickness		A	0.70	0.75	0.80
Stand Off		A1	0	0.02	0.05
Molding Thickness		A2		0.55	
LF Thickness		A3		0.203 REF	
Lead Width		b	0.20	0.25	0.30
Lead Length		L	0.30	0.40	0.50
Lead Pitch		e		0.50 BSC	
Lead tip to Exposed Pad		K		0.35 REF	
Package Edge Tolerance		aaa		0.10	
Lead Offset		bbb		0.10	
Molding Flatness		ccc		0.10	
Coplanarity		eee		0.08	
Exposed Pad Offset		fff		0.10	

Note：

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Colanarity applies to the terminals and all other bottom surface metallization.

Reflow profile



Recommended Temperature Sn95.5Ag4.0Cu0.5