极景微半导体

8-Output Ultra-Low Additive Jitter Differential Clock Buffer/Level Translator

US5D308
Datasheet

Description

The US5D308 is a 2.1-Ghz,8-output differential high-performance clock fanout buffer.

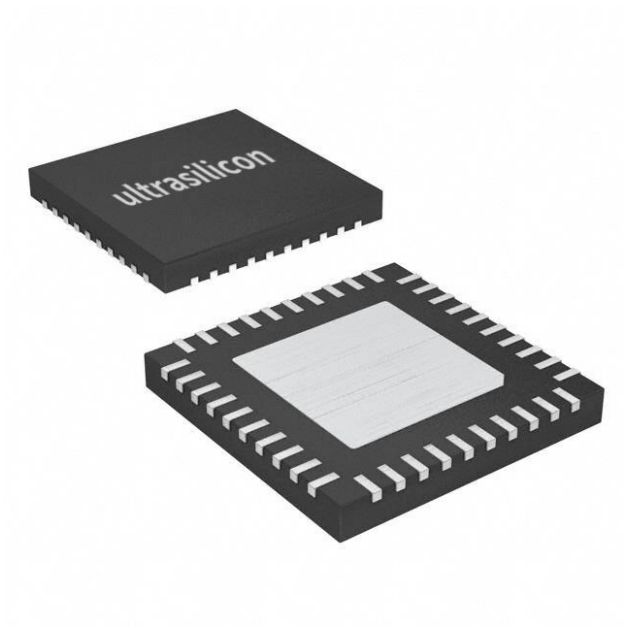
The input clock can be selected from two differential inputs or one crystal input. The selected input clock is distributed to two banks of 4 differential outputs and one LVCMOS output. Both differential output banks can be independently configured as LVPECL,LVDS,or HCSL drivers,or disabled.The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The outputs are at a defined level when inputs are open.

The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by a single-ended clock.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0)
- Remote Radio Units and Baseband Units

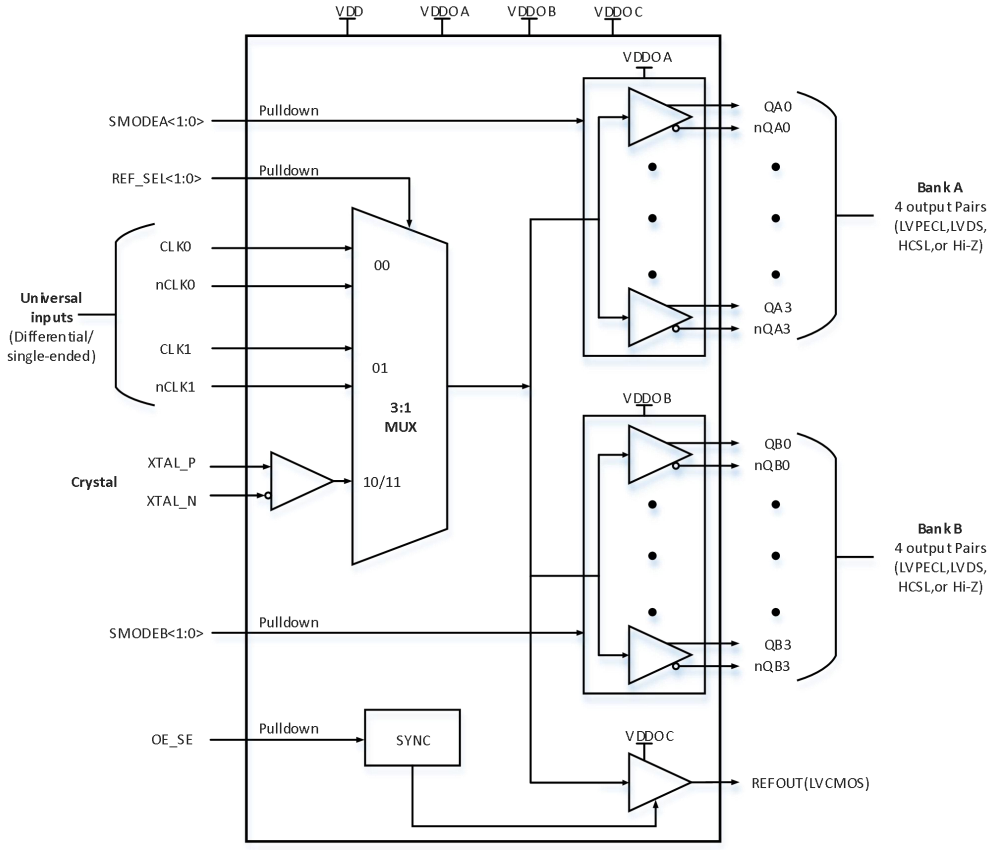


Features

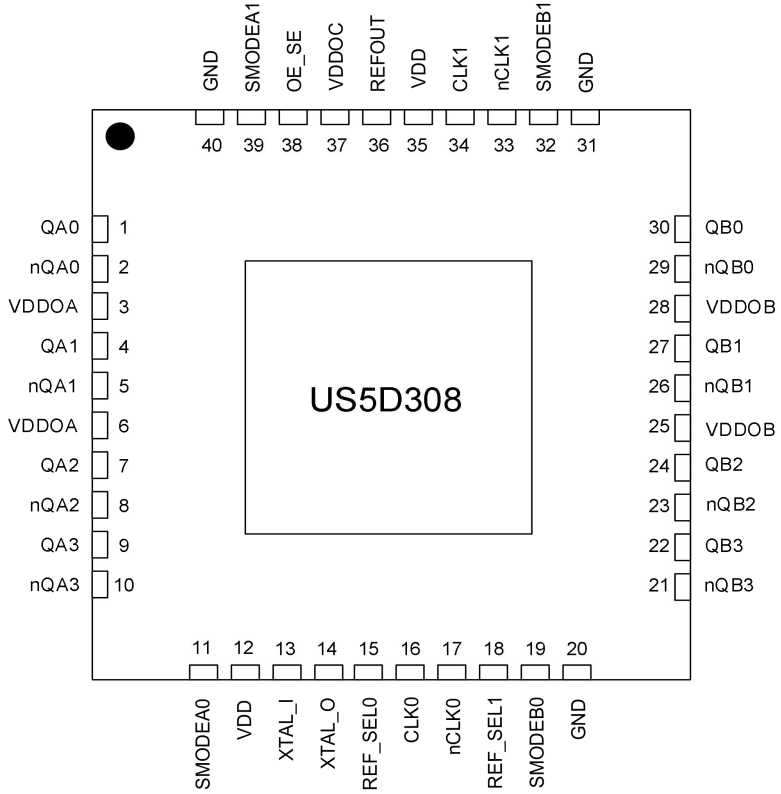
- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL, HSTL or Single Ended
- Crystal Input accepts 10MHz to 40MHz Crystal or Single Ended Clock
- Maximum Output Frequency
  LVPECL - 2.1GHz
  LVDS - 2.1GHz
  HCSL - 250MHz
  LVCMOS - 250MHz
- Two banks, each has four differential output pairs that can be configured as LVPECL or LVDS or HCSL or HiZ
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: 20ps (typical)
  (Bank A and Bank B at the same output level)
- Part-to-part skew: 200ps (typical)
- Additive RMS phase jitter @ 156.25MHz:
  12.5 fs RMS (10kHz - 1 MHz), typical @ 3.3V/ 3.3V
  50.5 fs RMS (10kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage modes:
  V_{DD}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- Industrial Temperature Range:-40°C to 85°C
- Compatible with lmk00308
- Available in a 40-pin, 6mm*6mm WQFN package

E-mail: sales@ultrasilicon.com.cn

Block Diagram



Pin Assignment for 6mm x 6mm 40-Lead WQFN Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions[1]

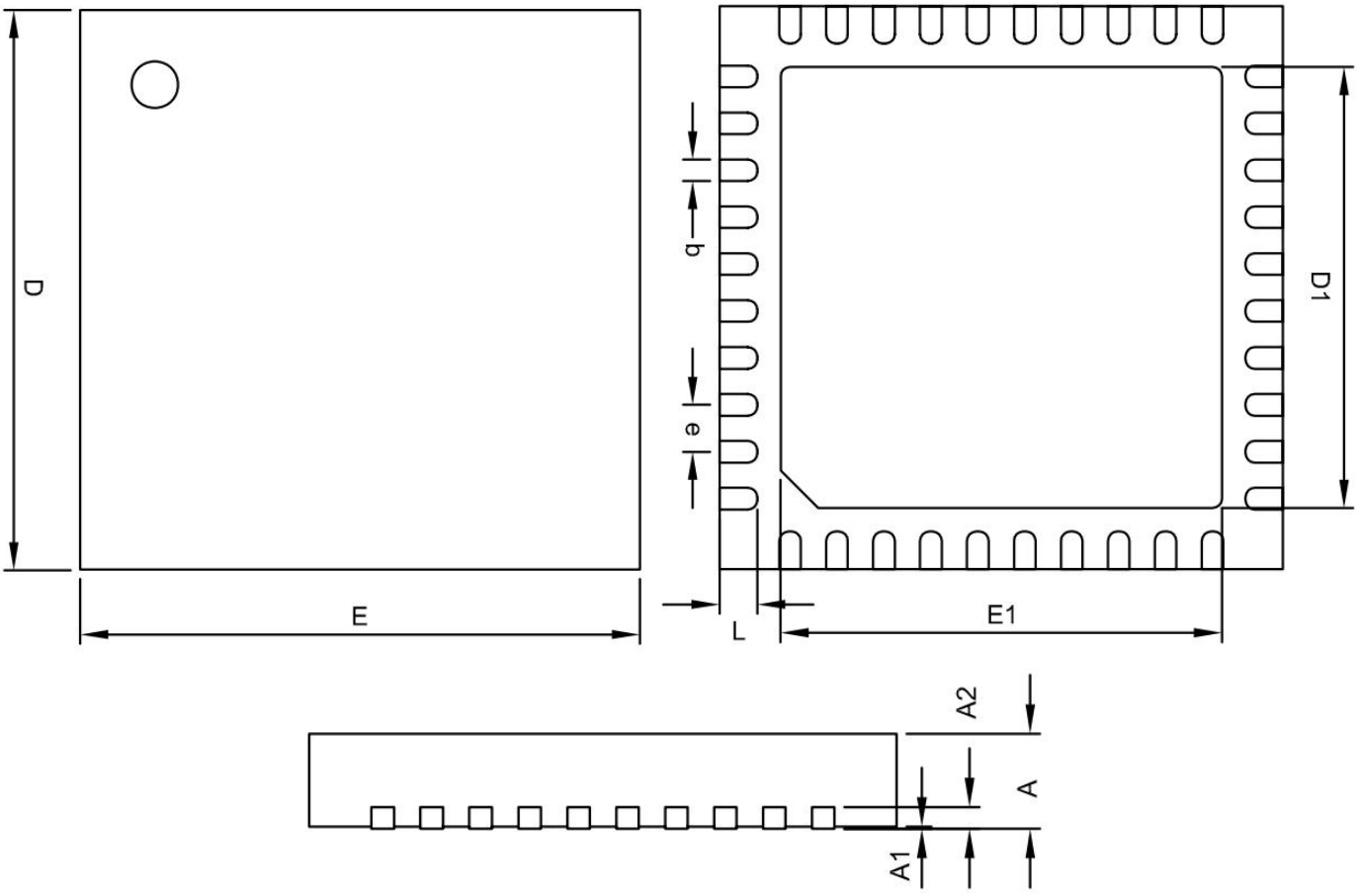
Number	Name	Type		Description
1	QA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
2	nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
3	V_{DDOA}	Power		Output supply pins for Bank QA outputs. 3.3V or 2.5V.
4	QA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5	nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
6	V_{DDOA}	Power		Output supply pins for Bank QA outputs. 3.3V or 2.5V.
7	QA2	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
8	nQA2	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
9	QA3	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
10	nQA3	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
11	SMODEA0	Input	Pulldown	Output driver select for Bank A outputs. See Table 8 for function. LVCMOS/LVTTL interface levels.
12	V_{DD}	Power		Power supply for Core and input Buffer blocks, 3.3V or 2.5V.
13	XTAL_I	Input		Crystal oscillator interface.
14	XTAL_O	Input		Crystal oscillator interface.
15	REF_SEL0	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function.
16	CLK0	Input	Pulldown	Non-inverting differential clock. Internally biased to ground.
17	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internally biased to $0.5V_{DD}$.
18	REF_SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function.
19	SMODEB0	Input	Pulldown	Output driver select for Bank B outputs. See Table 9 for function. LVCMOS/LVTTL interface levels.
20	GND	Power		Ground.
21	nQB3	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
22	QB3	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
23	nQB2	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
24	QB2	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
25	V_{DDOB}	Power		Output supply pins for Bank QB outputs. 3.3V or 2.5V.
26	nQB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
27	QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
28	V_{DDOB}	Power		Output supply pins for Bank QB outputs. 3.3V or 2.5V.
29	nQB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
30	QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
31	GND	Power		Ground.
32	SMODEB1	Input	Pulldown	Output driver select for Bank B outputs. See Table 9 for function. LVCMOS/LVTTL interface levels.

Table 1: Pin Descriptions[1] (Continued)

Number	Name	Type		Description
33	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock. Internally biased to $0.5V_{DD.}$
34	CLK1	Input	Pulldown	Non-inverting differential clock. Internally biased to ground.
35	V_{DD}	Power		Power supply for Core and input Buffer blocks, 3.3V or 2.5V.
36	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels.
37	VDDOC	Power		Output supply pin for REFOUT output.
38	OE_SE	Input	Pulldown	REFOUT output enable. LVCMOS/LVTTL interface levels. See Table 4.
39	SMODEA1	Input	Pulldown	Output driver select for Bank A outputs. See Table 8 for function. LVCMOS/LVTTL interface levels.
40	GND	Power		Ground.
ePad	GND_{EP}	Power		Connect ePad to ground to ensure proper heat dissipation.

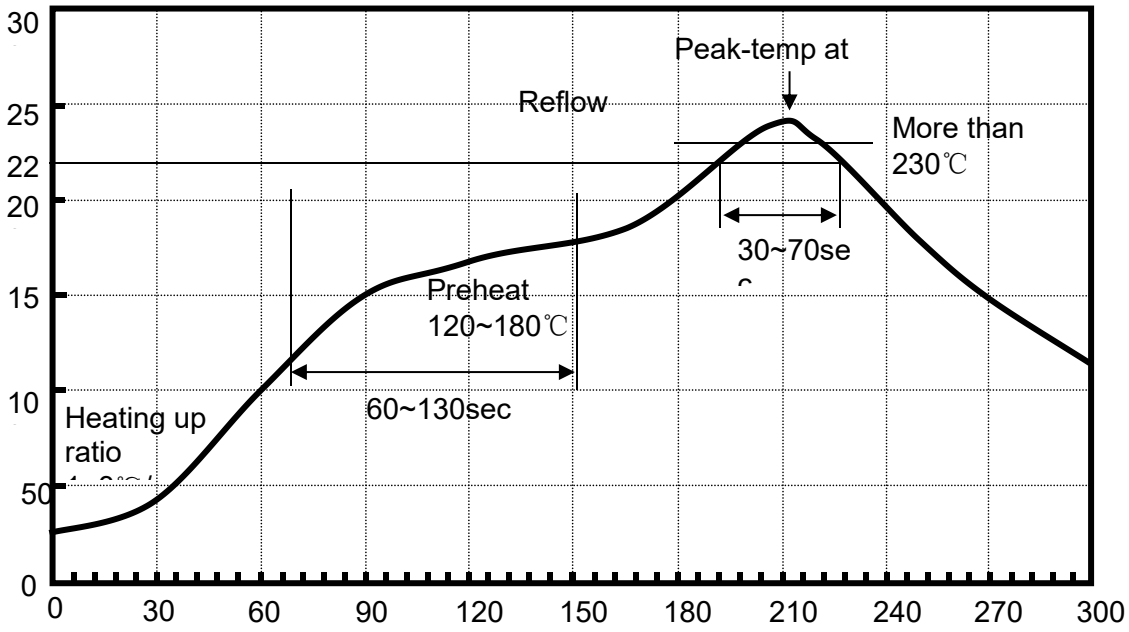
NOTE 1. *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

PACKAGE DIMENSIONS



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	5.95	6.00	6.05	0.2343	0.2362	0.2382
E	5.95	6.00	6.05	0.2343	0.2362	0.2382
D1	4.55	4.65	4.75	0.1791	0.1831	0.1870
E1	4.55	4.65	4.75	0.1791	0.1831	0.1870
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Reflow profile



Recommended Temperature Sn95.5Ag4.0Cu0.5