

Description

The US5S104, US5S106, US5S108, US5S110, US5S112 is a modular high-performance, low-skew, general-purpose clock fanout buffer family. These clock buffers are designed with a modular approach in mind.

Five different fan-out variations, 1:4 to 1:12, are available. All of the devices are pin-compatible to each other for easy handling.

All family members share the same high performing characteristics such as low additive jitter, low skew, and wide operating temperature range.

All family members support an asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

Operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from -40°C to 85°C.

Features

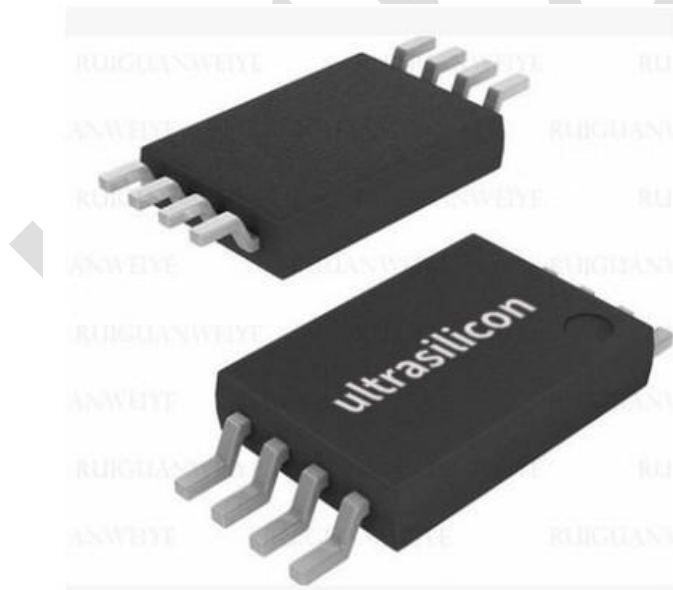
- High-Performance 1:4 LVCMOS Clock Buffer
- Extremely low additive jitter < 25-fs nominal
- Output Skew < 55 ps (Typical)
- Very low propagation delay < 3 ns
- Synchronous Output Enable Is Available
- Outputs Operate up to 250 MHz for 3.3V
- Outputs Operate up to 200 MHz for 2.5V and 1.8V
- Supply voltage: 3.3V, 2.5V or 1.8V
- Industrial Temperature Range: -40°C to 85°C
- Available in 8-Pin TSSOP Package

Applications

- General-Purpose Communication, Industrial, and Consumer Applications

Device Information

Part Number	Package	Body Size(NOM)
US5S104	TSSOP-8	3.00mm x 4.40mm



The schematic diagram illustrates the internal structure of the US5S104 component. It features a central logic block with four input pins on the left: CLKIN, 1G, Y0, and GND. The CLKIN pin is connected to a series of four inverters, which are then connected to the Y0, Y1, Y2, and Y3 pins. The 1G pin is connected to the Y0, Y1, Y2, and Y3 pins. The Y0, Y1, Y2, and Y3 pins are connected to the Y0, Y1, Y2, and Y3 pins. The GND pin is connected to the Y0, Y1, Y2, and Y3 pins. The output pins are labeled Y0, Y1, Y2, and Y3, and are grouped under the label LVCMOS. The component is labeled US5S104.

Table 1: Pin Descriptions

Number	Name	Type	Description
1	CLKIN	Input	Single-ended clock input with internal 150-k Ω (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
2	1G	Input	Global Output Enable with internal 50-k Ω (typical) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. HIGH: outputs enabled LOW: outputs disabled
3	Y0	Output	LVC MOS output 0. Typically connected to a receiver. Unused outputs can be left floating.
4	GND	Power	Ground.
5	Y2	Output	LVC MOS output 2. Typically connected to a receiver. Unused outputs can be left floating.
6	VDD	Power	DC power supply, 1.8V – 3.6V. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1- μ F capacitor near the pin.
7	Y3	Output	LVC MOS output 3. Typically connected to a receiver. Unused outputs can be left floating.
8	Y1	Output	LVC MOS output 1. Typically connected to a receiver. Unused outputs can be left floating.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

Item	Rating
V _{DD} : Supply voltage	0.5V to 3.6V
V _{CLKIN} : Input voltage (CLKIN)	
V _{IN} : Input voltage (1G)	
V _{Yn} : Output pins (Yn)	-0.5V to V _{DD} + 0.3 V
T _{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T _A	Ambient air temperature	-40	-	85	°C
T _J	Junction temperature		-	125	°C
V _{DD}	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V
		2.5-5%	2.5	2.5+5%	
		1.8-5%	1.8	1.8+5%	

Electrical Characteristics

VDD = 3.3 V $\pm$ 5 %, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD}	Core supply current	All-outputs active, f _{IN} = 100 MHz, C _L = 5pF, V _{DD} = 1.8 V		11		mA
		All-outputs active, f _{IN} = 100 MHz, C _L = 5pF, V _{DD} = 2.5 V		16		
		All-outputs active, f _{IN} = 100 MHz, C _L = 5pF, V _{DD} = 3.3 V		22		
CLOCK INPUT						
f _{IN_SE}	Input frequency	V _{DD} = 3.3 V	0.1		250	MHz
		V _{DD} = 2.5 V and 1.8 V	0.1		200	
V _{IH}	Input high voltage		0.7 x V _{DD}			V
V _{IL}	Input low voltage				0.3 x V _{DD}	
d _{VIN/dt}	Input slew rate	20% - 80% of input swing	0.1			V/ns
I _{IN_LEAK}	Input leakage current		−50		50	μA
C _{IN_SE}	Input capacitance	at 25°C		7		pF
CLOCK OUTPUT FOR ALL V _{DD} LEVELS						
f _{OUT}	Output frequency	V _{DD} = 3.3 V	0.1		250	MHz
		V _{DD} = 2.5 V and 1.8 V	0.1		200	
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t _{START}	Start-up time before output is active	See (1)			3	ms
t _{1G_ON}	Output enable time	See (2)			5	cycles
t _{1G_OFF}	Output disable time	See (3)			5	cycles
CLOCK OUTPUT FOR V _{DD} = 3.3 V ± 5%						
V _{OH}	Output high voltage	I _{OH} = −1 mA	2.8			V
V _{OL}	Output low voltage	I _{OL} = 1 mA			0.2	
t _{RISE-FALL}	Output rise and fall time	20/80%, C _L = 5 pF, f _{IN} = 156.25 MHz		0.35	0.7	ns
t _{OUTPUT-SKEW}	Output-output skew	See (4)		25	50	ps
t _{PART-SKEW}	Part-to-part skew				450	
t _{PROPDELAY}	Propagation delay	See (5)		1.5	2	ns
t _{JITTER-ADD}	Additive Jitter	f _{IN} =100 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		20	35	fs, RMS
R _{OUT}	Output impedance			50		Ω
CLOCK OUTPUT FOR V _{DD} = 2.5 V ± 5%						
V _{OH}	Output high voltage	I _{OH} = −1 mA	0.8 x V _{DD}			V
V _{OL}	Output low voltage	I _{OL} = 1 mA			0.2 x V _{DD}	
t _{RISE-FALL}	Output rise and fall time	20/80%, C _L = 5 pF, f _{IN} = 156.25 MHz		0.33	0.8	ns
t _{OUTPUT-SKEW}	Output-output skew	See (4)			50	ps
t _{PART-SKEW}	Part-to-part skew				400	
t _{PROPDELAY}	Propagation delay	See (5)		1.5	2.5	ns
t _{JITTER-ADD}	Additive Jitter	f _{IN} =100 MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		25	45	fs, RMS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{OUT}	Output impedance		50		Ω

- (1) Measured from V_{DD} stable to output active, when 1G = HIGH.
(2) Measured from 1G rising edge crossing V_{IH} to first rising edge of Y_n.
(3) Measured from 1G falling edge crossing V_{IL} to last falling edge of Y_n.
(4) Measured from rising edge of any Y_n output to any other Y_m output.
(5) Measured from rising edge of CLKIN to any Y_n output.

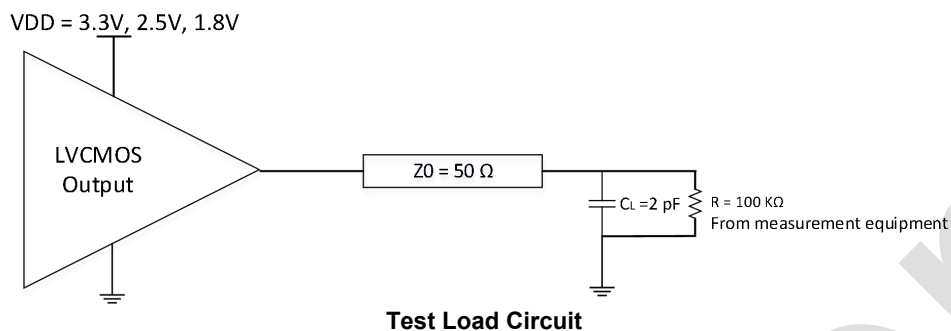
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK OUTPUT FOR V _{DD} = 1.8 V ± 5%						
V _{OH}	Output high voltage	I _{OH} = -1 mA	0.8 x V _{DD}			V
V _{OL}	Output low voltage	I _{OL} = 1 mA			0.2 x V _{DD}	
t _{RISE-FALL}	Output rise and fall time	20/80%, C _L = 5 pF, f _{IN} = 156.25 MHz		0.38	1	ns
t _{OUTPUT-SKEW}	Output-output skew	See (4)			50	ps
t _{PART-SKEW}	Part-to-part skew				900	ps
t _{PROP-DELAY}	Propagation delay	See (5)		1.5	3	ns
t _{JITTER-ADD}	Additive Jitter	f _{IN} = 100MHz, Input slew rate = 2 V/ns, Integration range = 12 kHz - 20 MHz		55	85	fs, RMS
R _{OUT}	Output impedance			50		Ω
GENERAL PURPOSE INPUT (1G)						
V _{IH}	High-level input voltage		0.7 x V _{DD}			V
V _{IL}	Low-level input voltage				0.3 x V _{DD}	
I _{IH}	Input high-level current	V _{IH} = V _{DD_REF}			67	μA
I _{IL}	Input low-level current	V _{IL} = GND			1	
Power dissipation capacitance per output						
C _{pd}		V _{DD} = 3.3V; f = 10MHz			8	pF
		V _{DD} = 2.5V; f = 10MHz			7	
		V _{DD} = 1.8V; f = 10MHz			6.5	

Timing Requirements

V_{DD} = 3.3 V ± 5 %, -40°C ≤ T_A ≤ 85°C

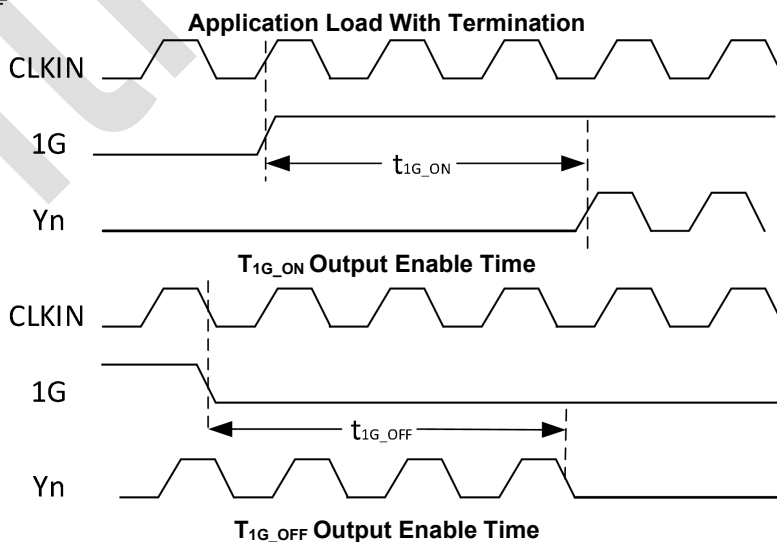
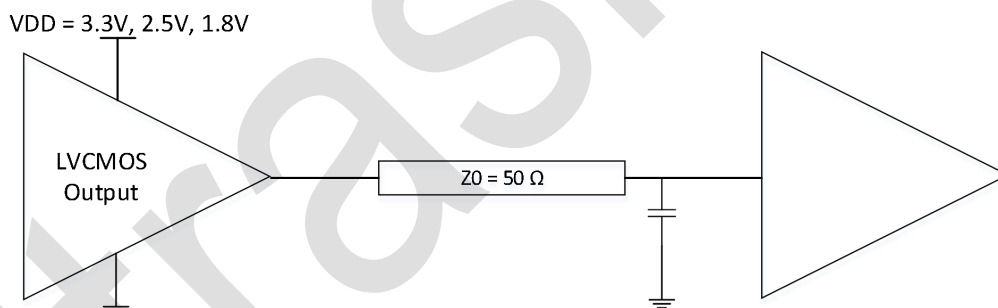
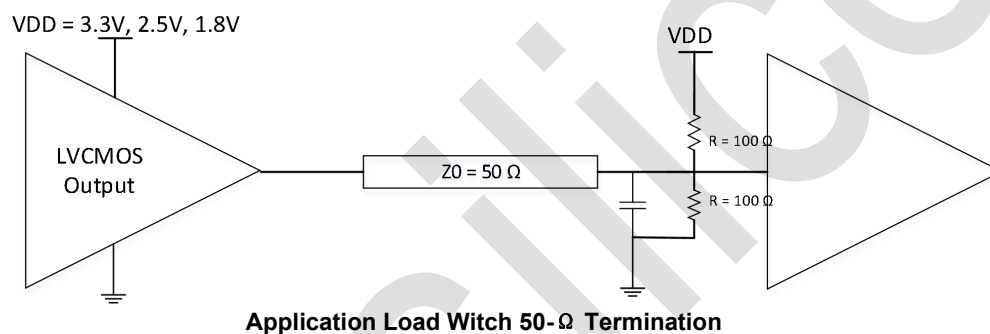
Power Supply	Min	Typ	Max	Unit
V/t _{RAMP}	0.1	-	50	V/rms

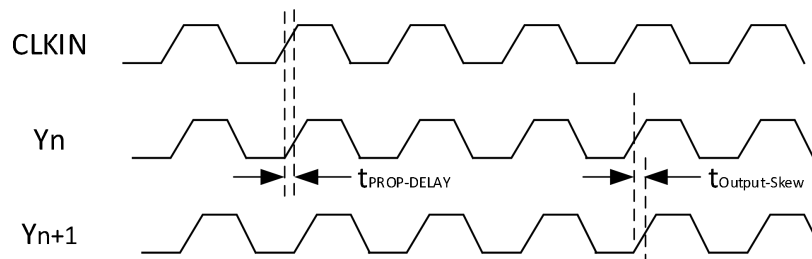
Parameter Measurement Information



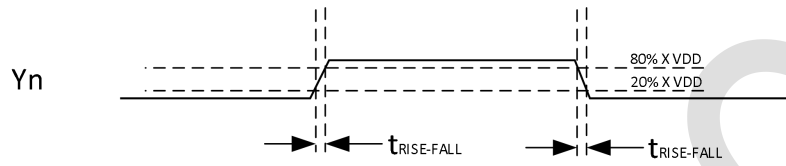
Note:

1. C_L include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: Clock Frequency $\leq 250\text{MHz}$, $Z_0 = 50 \Omega$, $t_r < 1.2\text{ns}$, $t_f < 1.2\text{ns}$



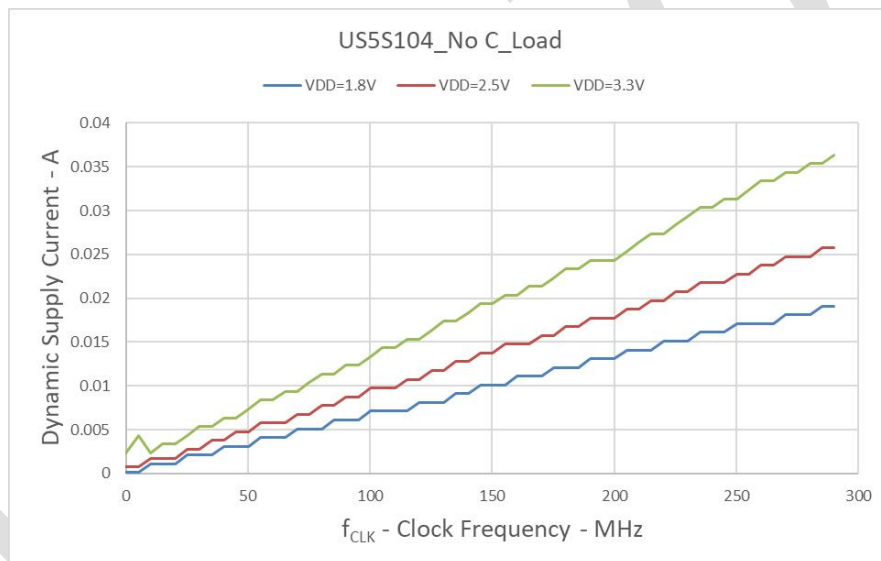


Propagation Delay $t_{\text{PROP-DELAY}}$ and Output Skew $t_{\text{OUTPUT-SKEW}}$

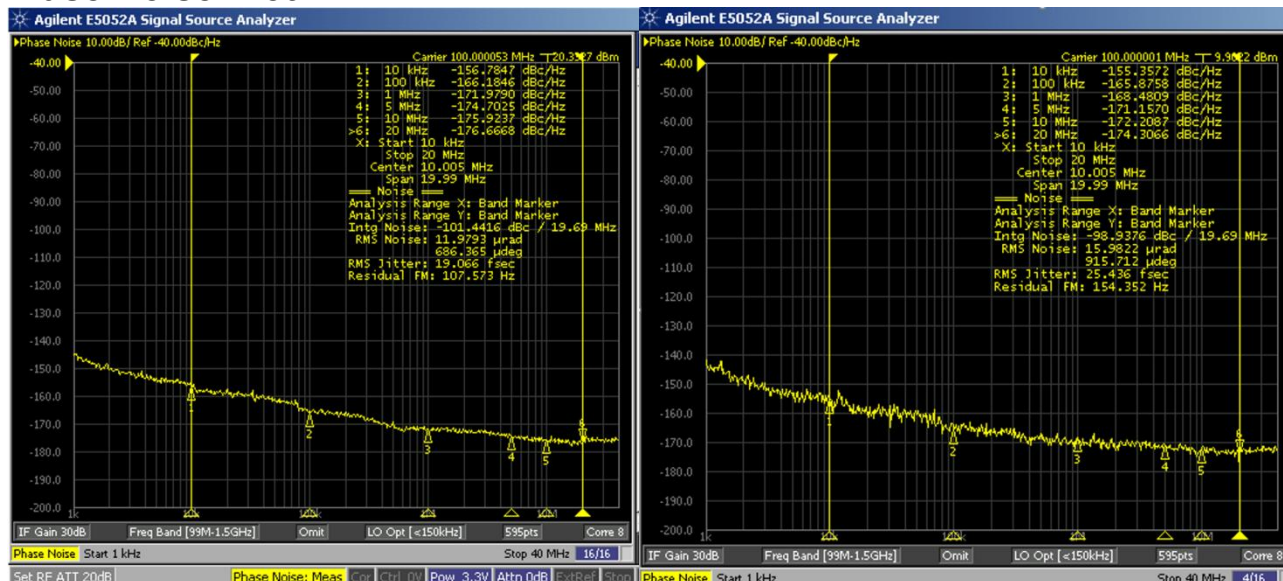


Rise and Fall Time $t_{\text{RISE-FALL}}$

Dynamic Supply Current vs. Clock Frequency



Phase Noise Plot



Wenzel 100MHz OCXO(19fs)

Output Phase Noise(25.5fs)

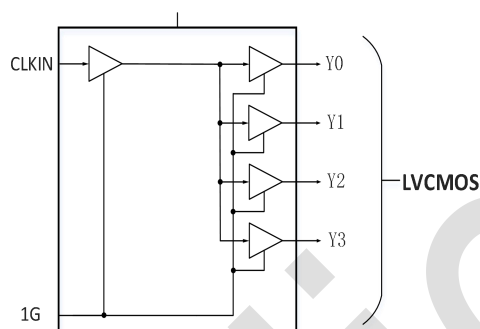
The additive phase jitter for this device was measured using the Wenzel 100MHz OCXO(19fs) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Detailed Description

Overview

The US5S10x family of devices is part of a low-jitter and low-skew LVCMOS fan-out buffer solution. For best signal integrity, it is important to match the characteristic impedance of the US5S10x's output driver with that of the transmission line.

Functional Block Diagram



Feature Description

The outputs of the US5S10x can be disabled by driving the synchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. Supply and ground pins must be connected to V_{DD} and GND, respectively.

Device Functional Modes

The US5S10x operates from 1.8-V, 2.5-V, or 3.3-V supplies. Table 1 shows the output logics of the US5S10x.

Table 1. Output Logic Table

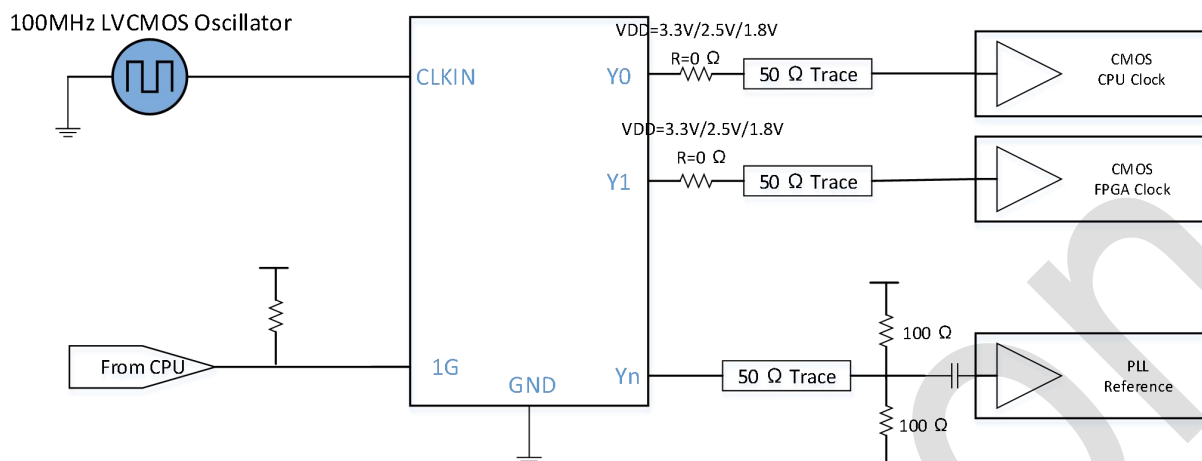
Inputs		Outputs
CLKIN	1G	Y_n
X	L	L
L	H	L
H	H	H

Application and Implementation

Application Information

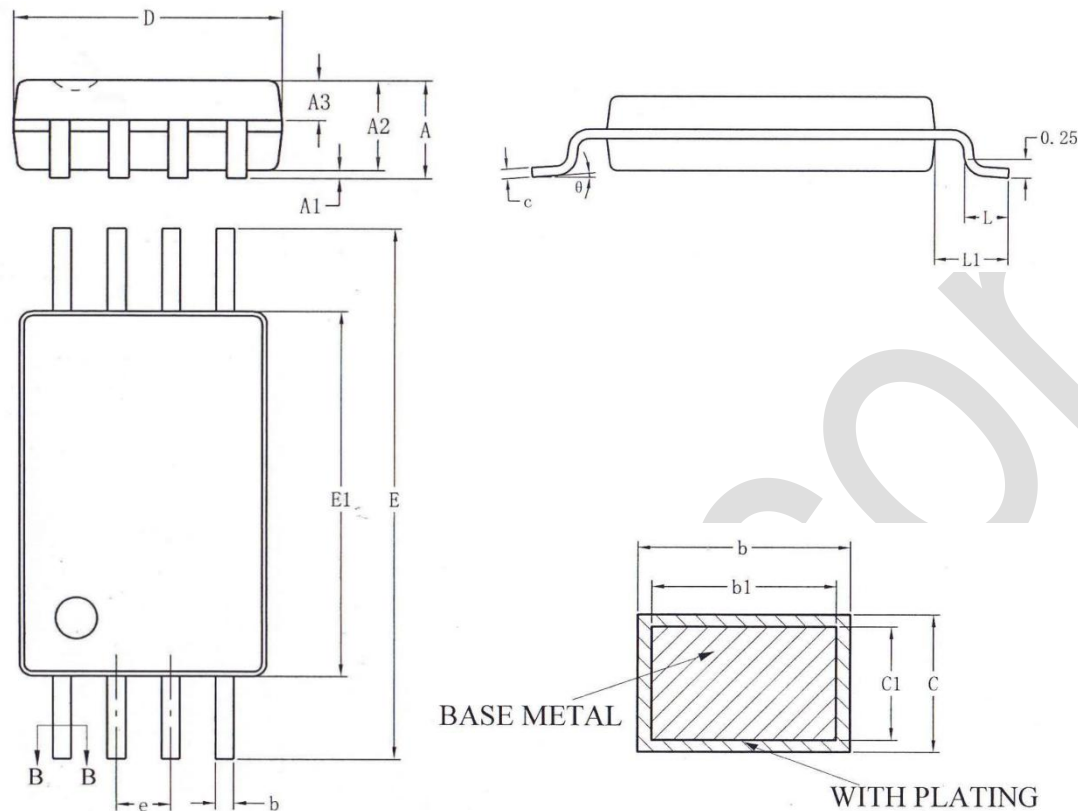
The US5S10x family is a low additive jitter LVCMOS buffer solution that can operate up to 250-MHz at $V_{DD} = 3.3\text{ V}$ and 200 MHz at $V_{DD} = 2.5\text{ V}$ to 1.8 V. Low output skew as well as the ability for synchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

Typical Application



System Configuration Example

PACKAGE DIMENSIONS



SYMBOL	Millimeter		
	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°

Reflow profile

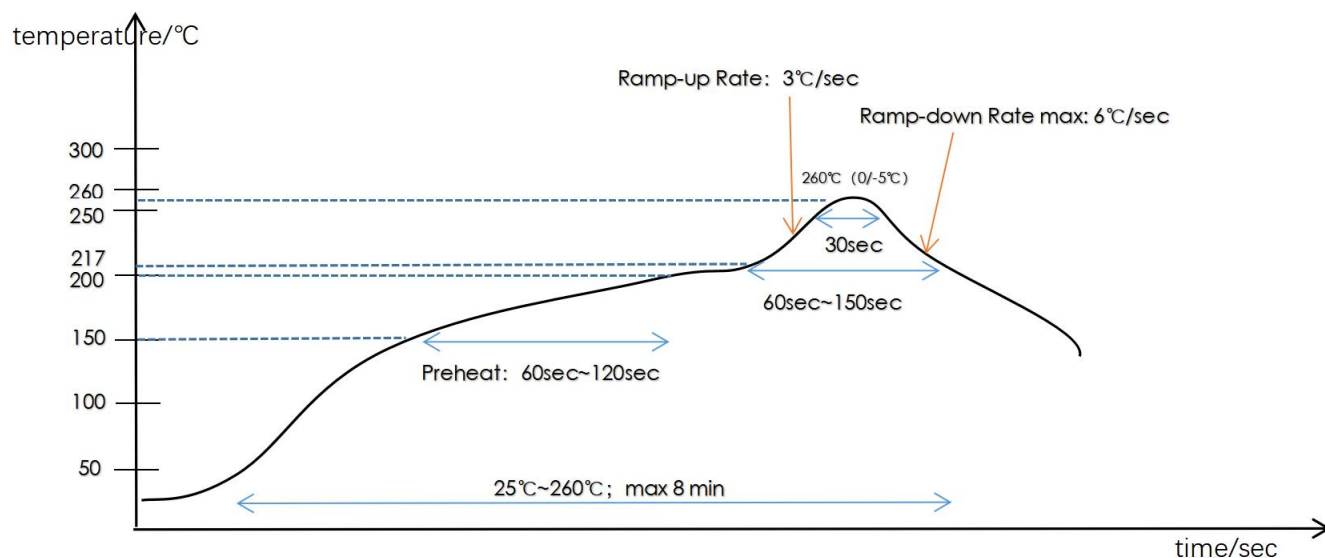
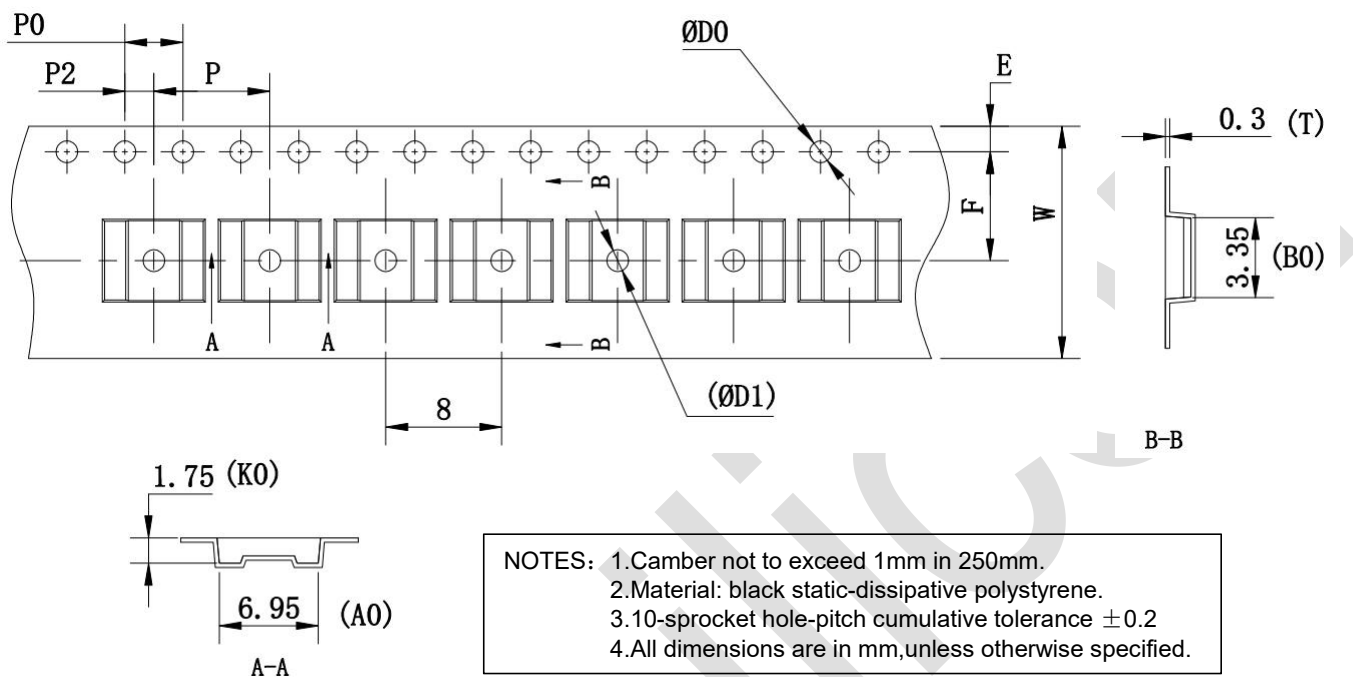


Figure1: Recommended Temperature(PB-Free)

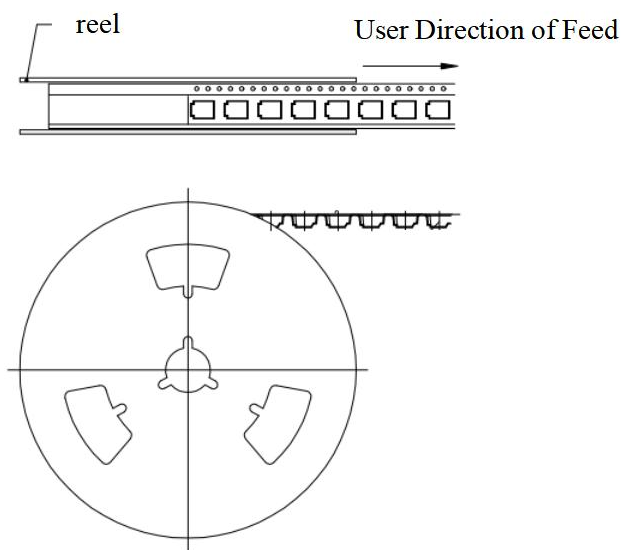
Reflow Condition	Convection or IR/Convection
Average ramp-up rate (217 °C to Peak)	3 °C/second max.
Preheat temperature 175(±25) °C	60-120 seconds
Temperature maintained above 217 °C	60-150 seconds
Time within 5 °C of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5 °C
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
Maximum number of reflow cycles	≤ 3

Tape and Reel information

Tape:



Reel:



330*100*16

Revision History

Date	Description of Change	Revision
2022.05.05	First Draft.	1.0
2023.02.10	Operating frequency range change。	1.5