USB4640/USB4640i

High Speed Inter-Chip (HSIC) USB 2.0 Hub and Flash Media Controller

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB4640/USB4640i is a Hi-Speed HSIC USB hub and card reader combo solution with an upstream port compliant to HSIC 1.0, a supplement to the USB 2.0 specification. The two downstream ports are compliant with the USB 2.0 specification.

High Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s. The HSIC interface is an industry standard 2-pin digital interface which uses standard USB software. The SMSC USB4640/USB4640i provides an ultra fast interface between an HSIC enabled host and today's popular flash media formats. The controller allows read/write capability to flash media from the following families:

- Secure Digital™ (SD)
- MultiMediaCard™ (MMC)
- Memory Stick® (MS)
- xD Picture Card™ (xD)[1]

The USB4640/USB4640i offers a versatile, cost-effective, and energy-efficient hub controller with 2 downstream USB 2.0 ports. This combo solution leverages SMSC's innovative technology that delivers industry-leading data throughput in mixed-speed USB environments. Average sustained transfer rates exceeding 35 MB/s are possible[2].

Highlights

- Upstream HSIC port and 2 exposed Hi-Speed USB 2.0 downstream ports for external peripheral expansion
- The dedicated flash media reader is internally attached to a 3rd downstream port of the hub as a USB Compound Device
  - a single or multiplexed flash media reader interface
- **PortMap**
  - Flexible port mapping and port disable sequencing supports multiple platform designs
- **PortSwap**
  - Programmable USB differential-pair pin locations eases PCB design by aligning USB signal traces directly to connectors
- **PHYBoost**
  - Programmable USB transceiver drive strength recovers signal integrity

Features

- Compliance with the following flash media card specifications SD 2.0 / MMC 4.2 / MS 1.43 / MS-Pro 1.02 / MS-Pro-HG 1.01 / MS-Duo 1.10 / xD 1.2
- Low-power digital HSIC interface offers a replacement for onboard host and device connection for analog USB bus cable
- HSIC interface enables printers, mobile PCs, ultra-mobile PCs, and cell phone products to reduce the total power budget while taking full advantage of USB connectivity and compatibility with existing USB drivers and software
- External 1.2 V reference allows upstream and downstream HSIC links to use the same voltage reference
- Supports a single external 3.3 V supply source; internal regulators provide 1.8 V internal core voltage for additional bill of materials and power savings
- The transaction translator (TT) in the hub supports operation of Full-Speed and Low-Speed peripherals
- 9 K RAM | 64 K on-chip ROM
- Enhanced EMI rejection and ESD protection performance
- Hub and flash media reader/writer configuration from a single source: External I²C® ROM or external SPI ROM
  - Configures internal code using an external I²C EEPROM
  - Supports external code using an SPI Flash EEPROM
  - Customizable vendor ID, product ID, and language ID if using an external EEPROM
- Up to 9 configurable GPIOs for special functions
- The USB4640 supports the commercial temperature range of 0°C to +70°C
- The USB4640i supports the industrial temperature range of -40°C to +85°C
- 48-pin QFN lead-free, RoHS compliant package (7x7 mm)

Applications

- 3G/4G handsets, smartphones, cell phones, and other mobile devices
- Desktop and mobile PCs
- Printers
- GPS navigation systems
- Media players/viewers
- Consumer A/V
- Set-top boxes
- Industrial products

1.For xD-Picture Card™ support, please obtain a user license from the xD-Picture Card License Office.
2.Host and media dependent.

ORDER NUMBERS:

USB4640/USB4640i-HZH for 48-PIN, QFN LEAD-FREE RoHS COMPLIANT PACKAGE

Please contact your local SMSC representative for more information.

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Chapter 1 Overview

The SMSC USB4640/USB4640i is a Hi-Speed HSIC USB hub and card reader combo solution with an upstream port compliant to HSIC 1.0, a supplement to the USB 2.0 specification. The two downstream ports are compliant with the USB 2.0 specification. In addition, The dedicated flash media reader/writer is internally attached to a 3rd downstream port of the hub as a USB Compound device.

High Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s. Please refer to the “High-Speed Inter-Chip USB Electrical Specification Revision 1.0 as of September 23, 2007” which can be found at http://www.usb.org/developers/docs/docs. This combo solution supports today’s popular multi-format flash media cards. This multi-format flash media controller and USB hub combo features two exposed downstream USB ports available for external peripheral expansion.

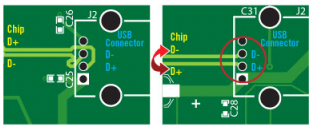
The USB4640/USB4640i will attach to an upstream port as a Full-Speed hub or as a Full-/Hi-Speed hub. The hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed hub) downstream devices on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

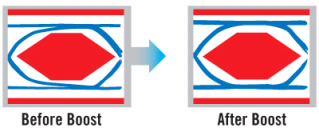
The USB4640/USB4640i includes programmable features such as:

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB4640/USB4640i hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB4640/USB4640i automatically reorders the remaining ports to match the USB host controller’s port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.



PHYBoost which enables four programmable levels of USB signal drive strengths in downstream port transceivers. PHYBoost attempts to restore USB signal integrity. The diagram on the right shows an example of Hi-Speed USB eye diagrams before (PHYBoost at 0%) and after (PHYBoost at 12%) signal integrity restoration in a compromised system environment.



Hardware Features

- Single chip HSIC hub and flash media controller combo
- USB4640 supports the commercial temperature range of 0°C to +70°C
- USB4640i supports the industrial temperature range of -40°C to +85°C
- Transaction translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI interface
- Onboard 24 MHz crystal driver circuit
- Optional external 24 MHz clock input which must be a 1.8 V signal
- Code execution via SPI ROM which must meet
  - 30 MHz or 60 MHz operation support
  - Single bit or dual bit mode support
  - Mode 0 or mode 3 SPI support

  Compliance with the following flash media card specifications:
- Secure Digital 2.0 / MultiMediaCard 4.2
  - SD 2.0, SD-HS, SD-HC
  - TransFlash™ and reduced form factor media
  - 1/4/8 bit MMC 4.2
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo, MS-HS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2
- Up to 9 GPIOs: Configuration and polarity for special function use
  - The number of actual GPIOs depends on the implementation configuration used
  - One GPIO available with up to 200 mA drive and protected “fold-back” short circuit current
- 8051 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 KB ROM | 9 KB RAM
- Integrated regulator for 1.8 V core operation

Software Features

- Hub and flash media reader/writer configuration from a single source:
  External I^2C ROM or external SPI ROM
- If the OEM is using an external EEPROM or an external SPI ROM, the following features are available:
  - Customizable vendor ID, product ID, and device ID
  - 12-hex digits maximum for the serial number string
  - 28-character manufacturer ID and product strings for the flash media reader/writer

OEM Selectable Hub Features

A default configuration is available in the USB4640/USB4640i following a reset. The USB4640/USB4640i may also be configured by an external I^2C EEPROM or via external SPI ROM flash.

- Compound Device support on a port-by-port basis
  - a port is permanently hardwired to a downstream USB peripheral device
- Select over-current sensing and port power control on an individual or ganged (all ports together) basis to match the OEM's choice of circuit board component selection
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs
- Configure the delay time for turning on downstream port power
- Bus- or self-powered selection
- Hub port disable or non-removable configurations
- Flexible port mapping and disable sequencing supports multiple platform designs
- Programmable USB differential-pair pin location eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength recovers USB signal integrity using 4 levels of signal drive strength
- Indicate the maximum current that the 2-port hub consumes
- Indicate the maximum current required for the hub controller

Chapter 2 Acronyms

ACK: Handshake packet (positive acknowledgement)

EOF: End of (micro) Frame

FM: Flash Media

FMC: Flash Media Controller

FS: Full-Speed Device

LS: Low-Speed Device

HS: Hi-Speed Device

I²C®: Inter-Integrated Circuit[1]

MMC: MultiMediaCard

MS: Memory Stick

MSC: Memory Stick Controller

OCS: Over-current Sense

PHY: Physical Layer

PLL: Phase-Locked Loop

RXD: Received eXchange Data

SD: Secure Digital

SDC: Secure Digital Controller

TXD: Transmit eXchange Data

UART: Universal Asynchronous Receiver-Transmitter

UCHAR: Unsigned Character

UINT: Unsigned Integer

1.I²C is a registered trademark of Philips Corporation.

Chapter 3 Pin Configuration

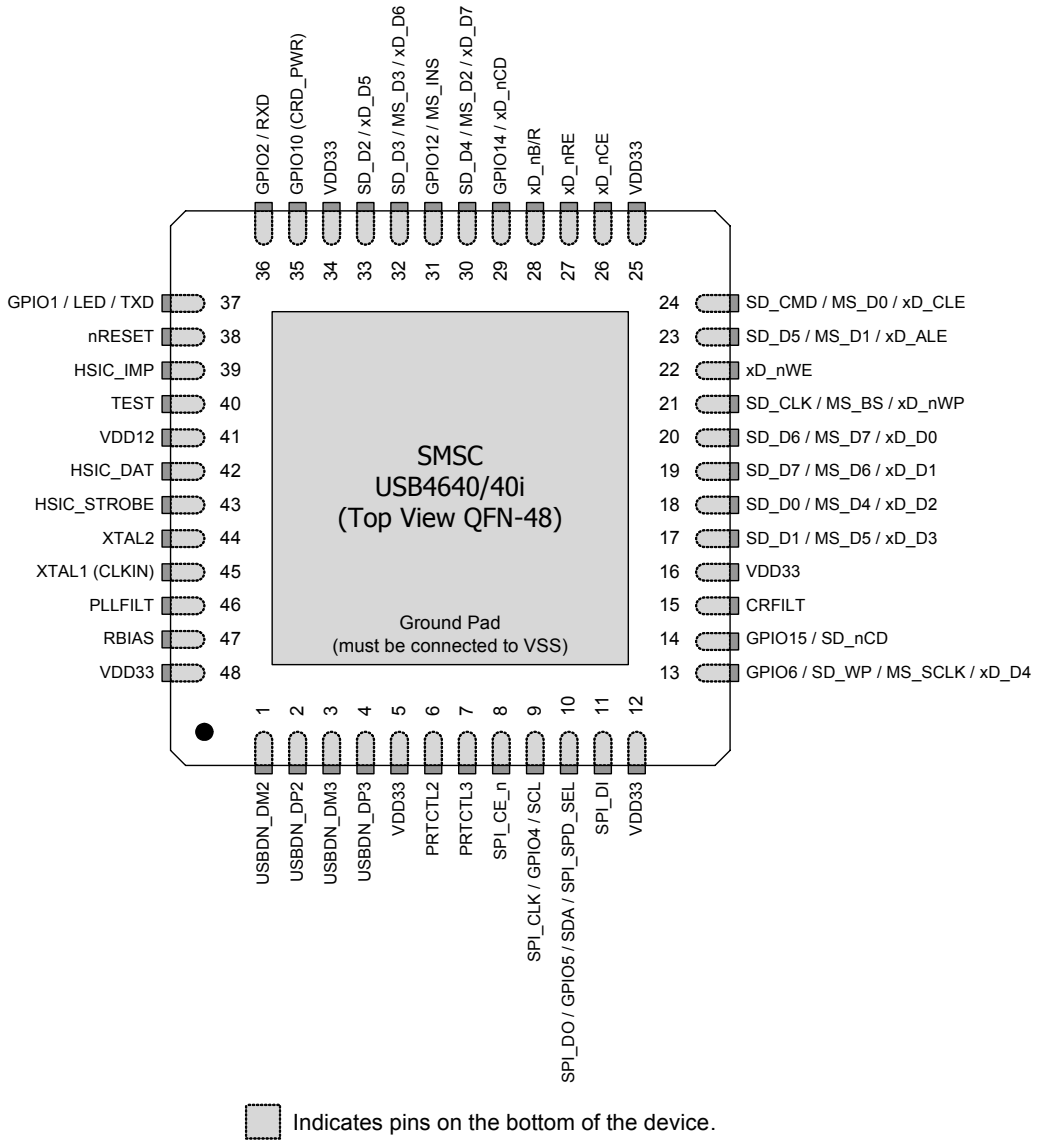


Figure 3.1 USB4640/USB4640i 48-Pin QFN

Chapter 4 Block Diagram

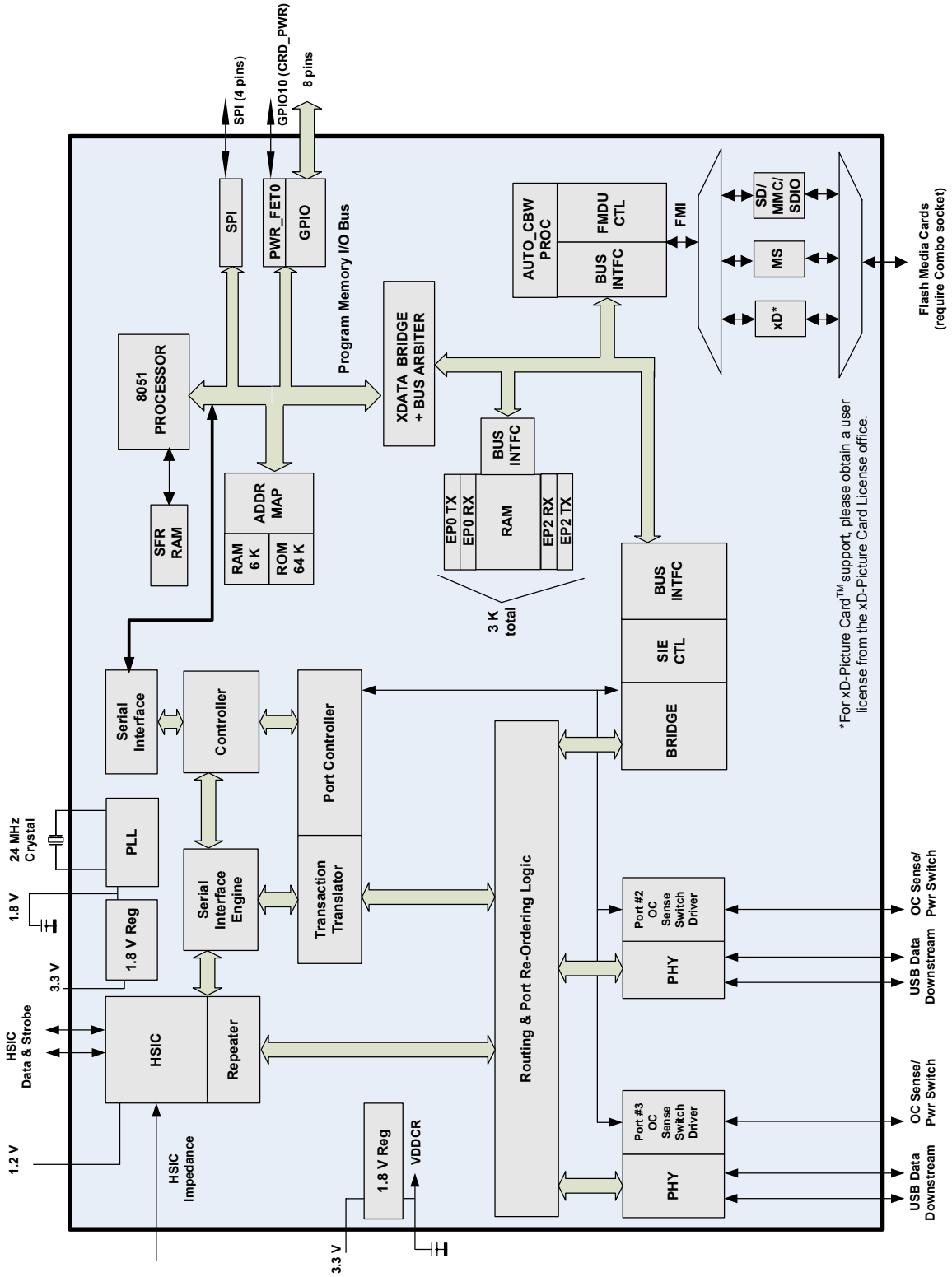


Figure 4.1 USB4640/USB4640i Block Diagram

Chapter 5 Pin Table

5.1 48-Pin Table

Table 5.1 USB4640/USB4640i 48-Pin Table

UPSTREAM HSIC INTERFACE (3 PINS)			
HSIC_IMP	HSIC_DAT	HSIC_STROBE	
DOWNSTREAM USB INTERFACE (3 PINS)			
XTAL1 (CLKIN)	XTAL2	RBIAS	
DOWNSTREAM 2-PORT USB INTERFACE (6 PINS)			
USBDN_DP2	USBDN_DM2	PRTCTL2	PRTCTL3
USBDN_DP3	USBDN_DM3		
SECURE DIGITAL / MEMORY STICK / xD INTERFACE (18 PINS)			
SD_D7 / MS_D6 / xD_D1	SD_D6 / MS_D7 / xD_D0	SD_D5 / MS_D1 / xD_ALE	SD_D4 / MS_D2 / xD_D7
SD_D3 / MS_D3 / xD_D6	SD_D2 / xD_D5	SD_D1 / MS_D5 / xD_D3	SD_D0 / MS_D4 / xD_D2
SD_CLK / MS_BS / xD_nWP	SD_CMD / MS_D0 / xD_CLE	GPIO15 / SD_nCD	GPIO12 / MS_INS
GPIO6 / SD_WP / MS_SCLK / xD_D4	GPIO14 / xD_nCD	xD_nWE	xD_nB/R
xD_nRE	xD_nCE		
SPI INTERFACE (4 PINS)			
SPI_CE_n	SPI_CLK / GPIO4 / SCL	SPI_DO / GPIO5 / SDA / SPI_SPD_SEL	SPI_DI

Table 5.1 USB4640/USB4640i 48-Pin Table

MISC (5 PINS)			
nRESET	TEST	GPIO1 / LED / TXD	GPIO2 / RXD
GPIO10 (CRD_PWR)			
POWER (9 PINS)			
(6) VDD33	VDD12	CRFILT	PLLFILT
TOTAL 48			

Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions below are applied when using the internal default firmware and can be referenced in Chapter 8, "Configuration Options," on page 28. Please reference Chapter 2, "Acronyms," on page 10 for a list of the acronyms used.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present in the signal name, the signal is asserted at a high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

6.1 USB4640/USB4640i Pin Descriptions

Table 6.1 USB4640/USB4640i Pin Descriptions

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
UPSTREAM HSIC INTERFACE			
HSIC_IMP	39	I	HSIC Impedance Control This pin selects the driver impedance of the HSIC_DAT and HSIC_STROBE pins. ‘1’ = approximately 50 Ω impedance ‘0’ = approximately 40 Ω impedance
HSIC_DAT	42	I/O	HSIC Data This is the bi-directional double data rate (DDR) data signal that is synchronous to the HSIC_STROBE signal as defined in the High-Speed Inter-Chip USB Specification, Version 1.0.
HSIC_STROBE	43	I/O	HSIC Strobe This pin is the bi-directional data strobe signal that is defined in the High-Speed Inter-Chip USB Specification, Version 1.0.
DOWNSTREAM USB INTERFACE			
USBDN_DM [3:2] USBDN_DP [3:2]	3 1 4 2	I/O-U	USB Bus Data These pins connect to the downstream USB bus data signals and can be swapped using the PortSwap feature (See Section 8.4.4.20, "F1h: Port Swap," on page 47).

Table 6.1 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
PRTCTL[3:2]	7 6	I/OD6PU	USB Power Enable As an output, these pins enable power to downstream USB peripheral devices and have weak internal pull-up resistors. See Section 6.3, "Port Power Control" for diagram and usage instructions. As an input, when the power is enabled, these pins monitor the over-current condition. When an over-current condition is detected, the pins turn the power off.
RBIAS	47	I-R	USB Transceiver Bias A 12.0 kΩ, ±1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents.
XTAL1 (CLKIN)	45	ICLKx	24 MHz Crystal Input or External Clock Input This pin can be connected to one terminal of the crystal or it can be connected to an external 24 MHz clock when a crystal is not used.
XTAL2	44	OCLKx	24 MHz Crystal Output This is the other terminal of the crystal or it is left open when an external clock source is used to drive XTAL1(CLKIN).
SECURE DIGITAL INTERFACE			
SD_D[7:0]	19 20 23 30 32 33 17 18	I/O8PU	Secure Digital Data 7-0 These are the bi-directional data signals SD_D0 - SD_D7 with weak pull-up resistors.
SD_CLK	21	O8	Secure Digital Clock This is an output clock signal to the SD/MMC device.
SD_CMD	24	I/O8PU	Secure Digital Command This is a bi-directional signal that connects to the CMD signal of the SD/MMC device. The bi-directional signal has a weak internal pull-up resistor.
GPIO15 /	14	I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD_nCD		I/O8PU	Secure Digital Card Detect GPIO This is a GPIO designated by the default firmware as the Secure Digital card detection pin and has an internal pull-up.

Table 6.1 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
GPIO6 /	13	I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SD_WP		I/O8	Secure Digital Write Protected GPIO This is a GPIO designated by the default firmware as the Secure Digital card interface mechanical write protect detect pin.
MEMORY STICK INTERFACE			
MS_BS	21	O8	Memory Stick Bus State This pin is connected to the bus state pin of the MS device. It is used to control the Bus States 0, 1, 2, and 3 (BS0, BS1, and BS3) of the MS device.
GPIO12 /	31	I/O8	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
MS_INS		IPU	Memory Stick Card Insertion GPIO This is a GPIO designated by the default software as the Memory Stick card detection pin and has a weak internal pull-up resistor.
MS_SCLK	13	O8	Memory Stick System Clock This pin is an output clock signal to the MS device.
MS_D[7:0]	20 19 17 18 32 30 23 24	I/O8PD	Memory Stick System Data In/Out These pins are the bi-directional data signals for the MS device. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either the memory stick controller MSC or the MS device on MS_D0. MS_D0, MS_D2, and MS_D3 have weak pull-down resistors. MS_D1 has a pull-down resistor if it is in parallel mode. Otherwise, it is disabled. In 4- or 8-bit parallel modes, all MS_D7 - MS_D0 signals have weak pull-down resistors.
xD-PICTURE CARD INTERFACE			
xD_D[7:0]	30 32 33 13 17 18 19 20	I/O8PD	xD-Picture Card Data 7-0 These pins are the bi-directional data signals xD_D7 - xD_D0 and have weak internal pull-down resistors.
xD_ALE	23	O8PD	xD-Picture Card Address Strobe This pin is an active high Address Latch Enable (ALE) signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.

Table 6.1 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
xD_nB/R	28	IPU	xD-Picture Card Busy or Data Ready This pin is connected to the BSY/RDY pin of the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nCE	26	O8PU	xD-Picture Card Chip Enable This pin is an active low chip enable signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_CLE	24	O8PD	xD-Picture Card Command Strobe This pin is an active high Command Latch Enable signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.
GPIO14 /	29	I/O6	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
xD_nCD		I/O8	xD-Picture Card Detection GPIO This is a GPIO designated by the default firmware as the xD-Picture Card detection pin and has an internal pull-up.
xD_nRE	27	O8PU	xD-Picture Card Read Enable This pin is an active low read strobe signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nWE	22	O8PU	xD-Picture Card Write Enable This pin is an active low write strobe signal for the xD-Picture Card device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).

Table 6.1 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
xD_nWP	21	O8PD	xD-Picture Card Write Protect This pin is an active low write protect signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.
SPI INTERFACE			
SPI_CE_n	8	O12	SPI Chip Enable This is the active low chip enable output. If the SPI interface is enabled, this pin must be driven high in power down states.
SPI_CLK /	9	I/O12	This is the SPI clock out to the serial ROM. See Section 6.4, "ROM BOOT Sequence" for diagram and usage instructions. During reset, drive this pin low.
GPIO4 /		I/O6	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SCL			When configured, this is the I^2C EEPROM clock pin.
SPI_DO /	10	I/O12	This is the data out for the SPI port. See Section 6.4, "ROM BOOT Sequence" for diagram and usage instructions.
GPIO5 /		I/O6	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
SDA /			This pin is the data pin when the device is connected to the optional I^2C EEPROM.
SPI_SPD_SEL		I/O12	This pin is used to select the speed of the SPI interface. During nRESET assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When nRESET is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality, the internal pull-down will be disabled. ‘0’ = 30 MHz (No external resistor should be applied.) ‘1’ = 60 MHz (A 10 K external pull-up resistor must be applied.) If the latched value is '1', then the pin is tri-stated when the chip is in the suspend state. If the latched value is '0', then the pin is driven low during a suspend state.
SPI_DI	11	I/O12PD	This is the SPI data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
MISC			
GPIO1 /	37	I/O6	General Purpose I/O This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
LED /			GPIO1 can be used as an LED output.
TXD			This signal can be configured as the TXD output of the internal UART. Custom firmware is required to activate this function.

Table 6.1 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE (Table 6.2)	DESCRIPTION
GPIO2 /	36	I/O6	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
RXD			This signal can be configured as input to the RXD of the internal UART. Custom firmware is required to activate this function.
GPIO10 (CRD_PWR)	35	I/O200	Card power drive: 3.3 V (100 mA or 200 mA) This must be the only FET used to power devices. Failure to do this will violate voltage specifications on device pins. If this pin is not being used as a card power pin, this pin may be used either as input, edge sensitive interrupt input, or output (GPIO). Please see Section 8.4.2.3, "A4h-A5h: Smart Media Device Power Configuration," on page 38 for more information.
nRESET	38	IS	RESET input The system uses this active low signal to reset the chip. The active low pulse should be at least 1 µs wide.
TEST	40	I	TEST Input Tie this pin to ground for normal operation.
DIGITAL / POWER / GROUND			
CRFILT	15		VDD Core Regulator Filter Capacitor This pin requires a 1.0 µF (or greater) ± 20% (ESR <0.1Ω) capacitor to VSS.
PLLFILT	46		Phase-locked Loop Regulator Filter Capacitor This pin requires a 1.0 µF (or greater) ± 20% (ESR <0.1Ω) capacitor to VSS.
VDD12	41		1.2 V Power for HSIC pads and buffers
VDD33	5 12 16 25 34 48		3.3 V Power and Regulator Input Please see Chapter 10, "DC Parameters," on page 55 for more information. Pins 16 and 48 each require an external bypass capacitor of 4.7 µF minimum.
VSS	ePad		The ground pad is the only VSS for the device and must be tied to ground with multiple vias.

6.2 Buffer Type Descriptions

Table 6.2 USB4640/USB4640i Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input.
I/O	Input/output.
IPU	Input with weak internal pull-up.
IS	Input with Schmitt trigger.
I/O6	Input/output buffer with 6 mA sink and 6 mA source.
I/OD6PU	Input/open drain output buffer with a 6 mA sink.
O8	Output buffer with an 8 mA sink and an 8 mA source.
O8PD	Output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-down resistor.
O8PU	Output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-up resistor.
I/O8	Input/output buffer with an 8 mA sink and an 8 mA source.
I/O8PD	Input/output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-down resistor.
I/O8PU	Input/output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-up resistor.
O12	Output buffer with a 12 mA sink and a 12 mA source.
I/O12	Input/output buffer with 12 mA sink and 12 mA source.
I/O12PD	Input/output buffer with 12 mA sink and 12 mA source with a weak internal pull-down resistor.
I/O200	Input/output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I/O-U	Analog input/output as defined in the USB 2.0 Specification.
I-R	RBIAS.

6.3 Port Power Control

Port Power control using a USB Power Switch

The USB4640/USB4640i has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled, and the pull-up resistor is enabled creating an open drain output.

If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will detect this event as a low. The open drain output does not interfere. The internal over-current sense filter handles the transient conditions, such as low voltage, while the device is powering up.

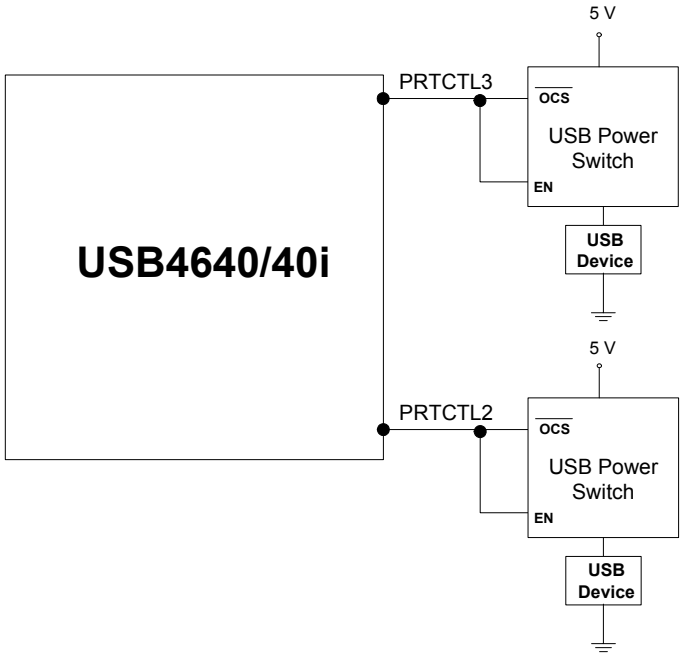


Figure 6.1 Port Power Control with USB Power Switch

Port Power control using a Poly Fuse

When using the USB4640/USB4640i with a poly fuse, an external diode must be used (See Figure 6.2). When disabling port power, the USB4640/USB4640i will drive a '0'. This procedure will have no effect since the external diode will isolate the pin from the load. When port power is enabled, the USB4640/USB4640i output driver is disabled, and the pull-up resistor is enabled which creates an open drain output. This open drain output condition means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to zero volts. The anode of the diode will be at 0.7 volts, and the Schmitt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

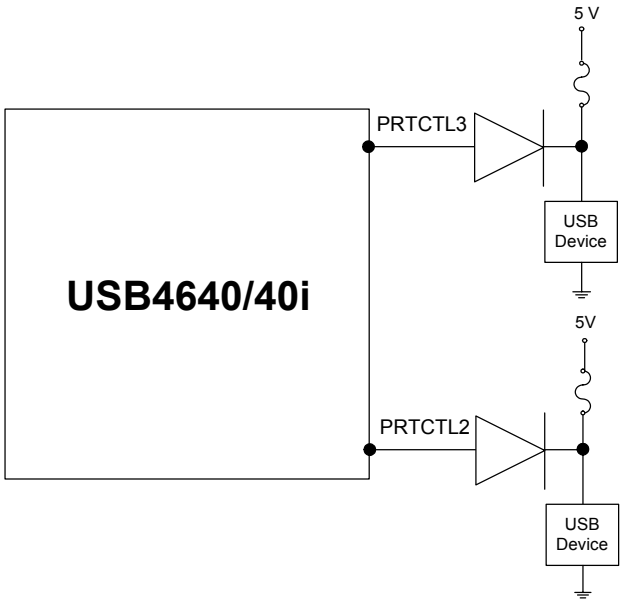


Figure 6.2 Port Power Control with a Single Poly Fuse and Multiple Loads

When using a single poly fuse to power all devices, note that for the ganged situation, all power control pins must be tied together.

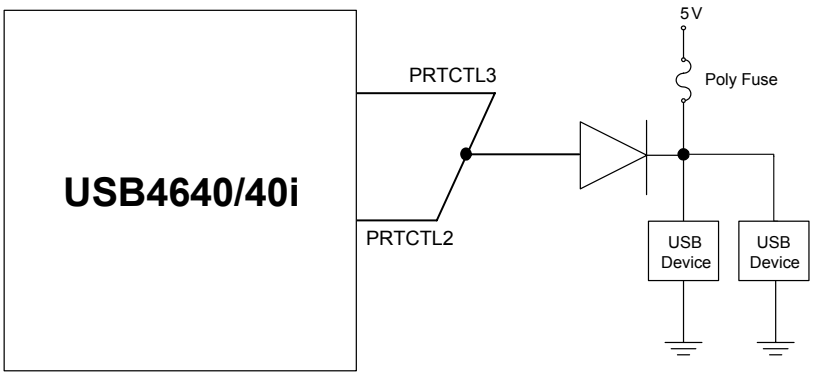


Figure 6.3 Port Power with Ganged Control with Poly Fuse

6.4 ROM BOOT Sequence

After power-on reset, the internal firmware checks for an external SPI flash device that contains a valid signature of "2DFU" (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and code execution begins at address 0x0000 in the external SPI device. Otherwise, code execution continues from the internal ROM.

If there is no SPI ROM detected, the internal firmware then checks for the presence of an I^2C ROM. The firmware looks for the signature 'ATA2' at the offset of FCh-FFh and 'ecf1' at the offset of 17Ch-17Fh in the I^2C ROM. The firmware reads in the I^2C ROM to configure the hardware and software internally. Please refer to Section 8.3.2, "EEPROM Data Descriptor," on page 29 for the details of the configuration options.

The SPI ROM required for the USB4640/USB4640i is a recommended minimum of 1 Mbit and support either 30 MHz or 60 MHz. The frequency used is set using the SPI_SPD_SEL. For 30 MHz operation, this pin must be pulled to ground through a 100 kΩ resistor. For 60 MHz operation, this pin must pulled up through a 100 kΩ resistor.

The SPI_SPD_SEL pin is used to choose the speed of the SPI interface. During nRESET assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When nRESET is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality. The internal pull-down will be disabled.

The firmware can determine the speed of operation on the SPI port by checking the SPI_SPEED in the SPI_CTL register (0x2400 - RESET = 0x02). Both 1- and 2-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMS are also supported.

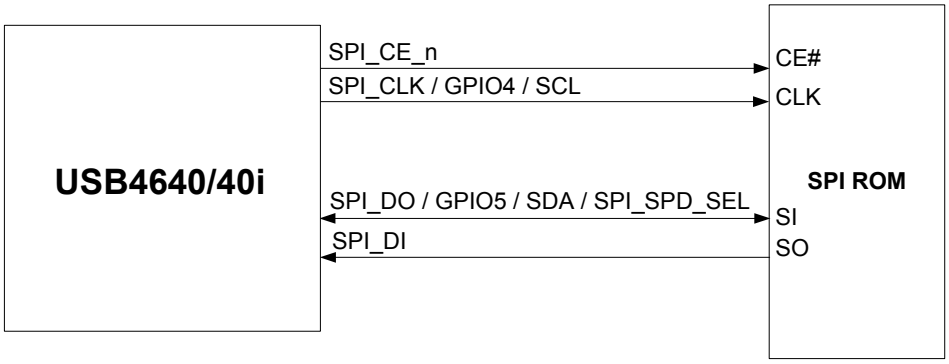


Figure 6.4 SPI ROM Connection

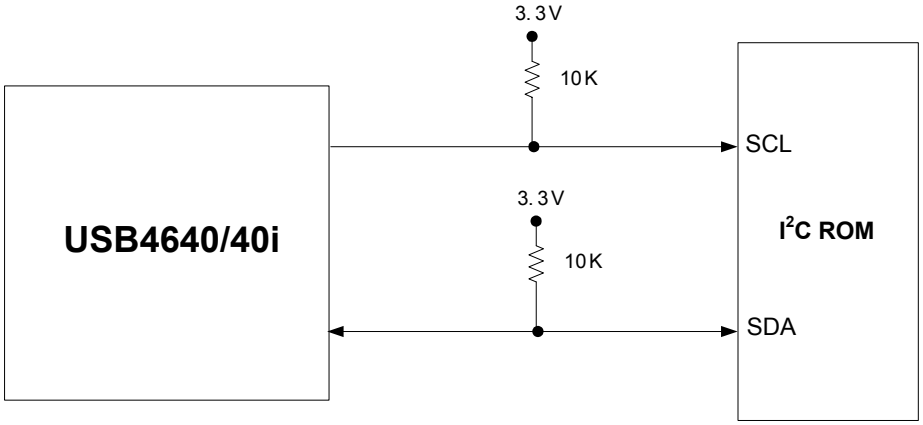


Figure 6.5 I^2C Connection

Chapter 7 Pin Reset States

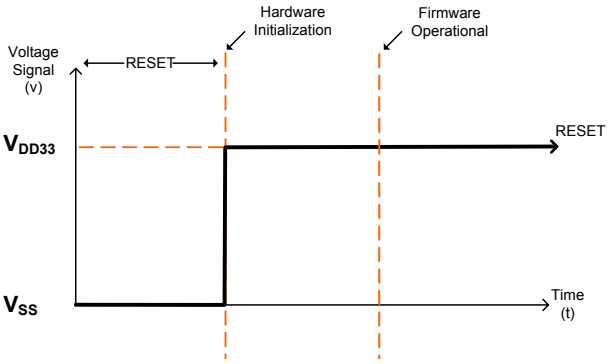


Figure 7.1 Pin Reset States

Table 7.1 Legend for Pin Reset States Table

SYMBOL	DESCRIPTION
0	Output driven low
1	Output driven high
IP	Input enabled
PU	Hardware enables pull-up
PD	Hardware enables pull-down
none	Hardware disables pad
--	Hardware disables function
Z	Hardware disables pad. Both output driver and input buffers are disabled.

7.1 Pin Reset States

Table 7.2 USB4640/USB4640i Reset States Table

		RESET STATE		
PIN	PIN NAME	FUNCTION	INPUT/ OUTPUT	PU/ PD
1	USBDN_DM2	USBDN_DM2	IP	PD
2	USBDN_DP2	USBDN_DP2	IP	PD
3	USBDN_DM3	USBDN_DM3	IP	PD
4	USBDN_DP3	USBDN_DP3	IP	PD
6	PRTCTL2	PRTCTL	0	--
7	PRTCTL3	PRTCTL	0	--

Table 7.2 USB4640/USB4640i Reset States Table (continued)

		RESET STATE		
PIN	PIN NAME	FUNCTION	INPUT/ OUTPUT	PU/ PD
8	SPI_CE_n	SPI_CE_n	1	--
9	SPI_CLK / GPIO4 / SCL	GPIO	0	--
10	SPI_DO / GPIO5 / SDA / SPI_SPD_SEL	GPIO	0	--
11	SPI_DI	SPI_DI	IP	PD
13	GPIO6 / SD_WP / MS_SCLK / xD_D4	GPIO	0	--
14	GPIO15 / SD_nCD	GPIO	IP	PU
17	SD_D1 / MS_D5 / xD_D3	none	Z	--
18	SD_D0 / MS_D4 / xD_D2	none	Z	--
19	SD_D7 / MS_D6 / xD_D1	none	Z	--
20	SD_D6 / MS_D7 / xD_D0	none	Z	--
21	SD_CLK / MS_BS / xD_nWP	none	Z	--
22	xD_nWE	xD_nWE	Z	--
23	SD_D5 / MS_D1 / xD_ALE	none	Z	--
24	SD_CMD / MS_D0 / xD_CLE	none	Z	--
26	xD_nCE	xD_nCE	Z	--
27	xD_nRE	xD_nRE	Z	--
28	xD_nB/R	xD_nB/R	Z	--
29	GPIO14 / xD_nCD	GPIO	IP	PU
30	SD_D4 / MS_D2 / xD_D7	none	Z	--
31	GPIO12 / MS_INS	GPIO	IP	PU
32	SD_D3 / MS_D3 / xD_D6	none	Z	--
33	SD_D2 / xD_D5	none	Z	--
35	GPIO10 (CRD_PWR)	GPIO	Z	--
36	GPIO2 / RXD	GPIO	0	--
37	GPIO1 / LED / TXD	GPIO	0	--
38	nRESET	nRESET	IP	--
39	HSIC_IMP	HSIC_IMP	Z	--
40	TEST	TEST	IP	PD

Table 7.2 USB4640/USB4640i Reset States Table (continued)

		RESET STATE		
PIN	**PIN NAME**	**FUNCTION**	**INPUT/ OUTPUT**	**PU/ PD**
42	HSIC_DAT	HSIC_DAT	IP	--
43	HSIC_STROBE	HSIC_STROBE	IP	--

Chapter 8 Configuration Options

8.1 Hub

SMSC's USB 2.0 hub is fully compliant to the Universal Serial Bus Specification available from the USB Implementer's Forum found at http://www.usb.org (Revision 2.0 April 27, 2000 and the 12/7/2000 and 5/28/2002 Errata). Please reference Chapter 11 (Hub Specification) for general details regarding hub operation and functionality.

For performance reasons, the hub provides 1 transaction translator (TT) that is shared by both downstream ports defined as a single-TT configuration. The TT contains 4 non-periodic buffers.

8.1.1 Hub Configuration Options

The SMSC hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are two principal ways to configure the hub:

- via the internal default settings or
- by settings stored in an external EEPROM or SPI Flash device.

8.1.1.1 Power Switching Polarity

The hub will only support active high power controllers.

8.2 Card Reader

The SMSC USB4640/USB4640i is fully compliant with the following flash media card reader specifications:

- Secure Digital 2.0 / MultiMediaCard 4.2
  -SD 2.0, HS-SD, HC-SD
  -TransFlash™ and reduced form factor media
  -1/4/8 bit MMC 4.2
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  -Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2

8.3 System Configurations

8.3.1 EEPROM/SPI Interface

The USB4640/USB4640i can be configured via a 2-wire (I^2C) EEPROM (512x8) or an external SPI flash device containing the firmware for the USB4640/USB4640i. If an external configuration device does not exist the internal default values will be used. If one of the external devices is used for configuration, the OEM can update the values through the USB interface. The hub will then "attach" to the upstream USB host.

The USBDM tool set is available in the USB264x Hub Card reader combo software release package. To download the software package from SMSC's website, please visit:

https://www2.smsc.com/mkt/CW_SFT_PUB.nsf/Agreements/OBJ+Hub+Card+Reader

to go to the OBJ Hub Card Reader Software Download Agreement. Review the license, and if you agree, check the "I agree" box and then select “Confirm”. You will then be able to download USB264x Hub Card reader combo release package zip file containing the USBDM tool set.

Please note that the following applies to the system values and descriptions when used:

- N/A = Not applicable to this part
- Reserved = For internal use

8.3.2 EEPROM Data Descriptor

Table 8.1 Internal Flash Media Controller Configurations

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
00h	USB_SER_LEN	USB Serial String Descriptor Length	1Ah
01h	USB_SER_TYP	USB Serial String Descriptor Type	03h
02h-19h	USB_SER_NUM	USB Serial Number	"000008264001" (See Note 8.1)
1Ah-1Bh	USB_VID	USB Vendor Identifier	0424
1Ch-1Dh	USB_PID	USB Product Identifier	4040
1Eh	USB_LANG_LEN	USB Language String Descriptor Length	04h
1Fh	USB_LANG_TYP	USB Language String Descriptor Type	03h
20h	USB_LANG_ID_LSB	USB Language Identifier Least Significant Byte	09h (See Note 8.3)
21h	USB_LANG_ID_MSB	USB Language Identifier Most Significant Byte	04h (See Note 8.3)
22h	USB_MFR_STR_LEN	USB Manufacturer String Descriptor Length	10h
23h	USB_MFR_STR_TYP	USB Manufacturer String Descriptor Type	03h
24h-31h	USB_MFR_STR	USB Manufacturer String	“Generic” (See Note 8.1)
32h-5Dh	Reserved	-	00h
5Eh	USB_PRD_STR_LEN	USB Product String Descriptor Length	30h
5Fh	USB_PRD_STR_TYP	USB Product String Descriptor Type	03h
60h-99h	USB_PRD_STR	USB Product String	"Ultra Fast Media Reader" (See Note 8.1)
9Ah	USB_BM_ATT	USB BmAttribute	80h

Table 8.1 Internal Flash Media Controller Configurations (continued)

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
9Bh	USB_MAX_PWR	USB Max Power	30h (96 mA)
9Ch	ATT_LB	Attribute Lo byte	40h (Reverse SD_WP only)
9Dh	ATT_HLB	Attribute Hi Lo byte	80h (Reverse SD2_WP only)
9Eh	ATT_LHB	Attribute Lo Hi byte	00h
9Fh	ATT_HB	Attribute Hi byte	00h
A0h	MS_PWR_LB	Memory Stick Device Power Lo byte	00h
A1h	MS_PWR_HB	Memory Stick Device Power Hi byte	0Ah
A2h-A3h	Not Applicable	-	00h
A4h	SM_PWR_LB	Smart Media Device Power Lo byte	00h (See Note 8.2)
A5h	SM_PWR_HB	Smart Media Device Power Hi byte	0Ah (See Note 8.2)
A6h	SD_PWR_LB	Secure Digital Device Power Lo byte	00h
A7h	SD_PWR_HB	Secure Digital Device Power Hi byte	0Ah
A8h	LED_BLK_INT	LED Blink Interval	02h
A9h	LED_BLK_DUR	LED Blink After Access	28h
AAh - B0h	DEV0_ID_STR	Device 0 Identifier String	N/A
B1h - B7h	DEV1_ID_STR	Device 1 Identifier String	“MS”
B8h - BEh	DEV2_ID_STR	Device 2 Identifier String	“SM” (See Note 8.2)
BFh - C5h	DEV3_ID_STR	Device 3 Identifier String	“SD/MMC”
C6h - CDh	INQ_VEN_STR	Inquiry Vendor String	“Generic”
CEh - D2h	INQ_PRD_STR	Inquiry Product String	82640
D3h	DYN_NUM_LUN	Dynamic Number of LUNs	01h
D4h - D7h	DEV_LUN_MAP	Device to LUN Mapping	FFh, 00h, 00h, 00h
D8h - DAh	Reserved	-	00h, 06h, 0Dh
DBh - DDh	Reserved	-	59h, 56h, 97h

Table 8.2 Hub Controller Configurations

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
DEh	VID_LSB	Vendor ID Least Significant Byte	24h
DFh	VID_MSB	Vendor ID Most Significant Byte	04h
E0h	PID_LSB	Product ID Least Significant Byte	40h
E1h	PID_MSB	Product ID Most Significant Byte	26h
E2h	DID_LSB	Device ID Least Significant Byte	A1h
E3h	DID_MSB	Device ID Most Significant Byte	08h
E4h	CFG_DAT_BYT1	Configuration Data Byte 1	8Bh
E5h	CFG_DAT_BYT2	Configuration Data Byte 2	28h
E6h	CFG_DAT_BYT3	Configuration Data Byte 3	00h
E7h	NR_DEVICE	Non-Removable Devices	02h
E8h	PORT_DIS_SP	Port Disable (Self)	00h
E9h	PORT_DIS_BP	Port Disable (Bus)	00h
EAh	MAX_PWR_SP	Max Power (Self)	01h
EBh	MAX_PWR_BP	Max Power (Bus)	32h
ECh	HC_MAX_C_SP	Hub Controller Max Current (Self)	01h
EDh	HC_MAX_C_BP	Hub Controller Max Current (Bus)	32h
EEh	PWR_ON_TIME	Power-on Time	32h
EFh	BOOST_UP	Boost_Up	00h
F0h	BOOST_3:0	Boost_3:0	00h
F1h	PRT_SWP	Port Swap	00h
F2h	PRTM12	Port Map 12	00h
F3h	PRTM3	Port Map 3	00h

Table 8.3 Other Internal Configurations

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
F4h	Reserved	Reserved	00h
F5h	Reserved	Reserved	66h
F6h	Reserved	Reserved	00h
F7-FAh	Not Applicable	-	N/A
FBh	Not Applicable	-	00h
FCh-FFh	NVSTORE_SIG	Non-Volatile Storage Signature	“ATA2”

8.4 Set bit 7 of bmAttribute to enable the registers in Table 8.4.

Table 8.4 Internal Flash Media Controller Extended Configurations

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
100h - 106h	CLUN0_ID_STR	Combo LUN 0 Identifier String	“COMBO”
107h- 129h	Not Applicable	-	N/A
12Ah-145h	Not applicable	-	00h
146h	Not Applicable	-	01h
147h - 14Bh	Not Applicable	-	01h, FFh, FFh, FFh, FFh
14Ch	Not Applicable	-	0Ah
14Dh-17Bh	Not Applicable	-	00h
17Ch-17Fh	NVSTORE_SIG2	Non-Volatile Storage Signature	“ecf1”

Note 8.1 This value is a UNICODE UTF-16LE encoded string value that meets the USB 2.0 specification (Revision 2.0, 2000). Values in double quotations without this note are ASCII values.

Note 8.2 A value of “SM” will be overridden with “xD” once an xD-Picture Card has been identified.

Note 8.3 For a list of the most current 16-bit language ID’s defined by the USB-IF, please visit http://www.unicode.org or consult *The Unicode Standard, Worldwide Character Encoding*, (Version 4.0), The Unicode Consortium, Addison-Wesley Publishing Company, Reading, Massachusetts.

8.4.1 EEPROM Data Descriptor Register Descriptions

8.4.1.1 00h: USB Serial String Descriptor Length

BYTE	NAME	DESCRIPTION
0	USB_SER_LEN	USB serial string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes).

8.4.1.2 01h: USB Serial String Descriptor Type

BYTE	NAME	DESCRIPTION
1	USB_SER_TYP	USB serial string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

8.4.1.3 02h-19h: USB Serial Number Option

BYTE	NAME	DESCRIPTION
25:2	USB_SER_NUM	Maximum string length is 12 hex digits. Must be unique to each device.

8.4.1.4 1Ah-1Bh: USB Vendor ID Option

BYTE	NAME	DESCRIPTION
1:0	USB_VID	This ID is unique for every vendor. The vendor ID is assigned by the USB Implementer's Forum.

8.4.1.5 1Ch-1Dh: USB Product ID Option

BYTE	NAME	DESCRIPTION
1:0	USB_PID	This ID is unique for every product. The product ID is assigned by the vendor.

8.4.1.6 1Eh: USB Language Identifier Descriptor Length

BYTE	NAME	DESCRIPTION
0	USB_LANG_LEN	USB language ID string descriptor length as defined by Section 9.6.7 "String" of the USB 2.0 Specification (Revision 2.0, 2000). This field is the "bLength" which describes the size of the string descriptor (in bytes).

8.4.1.7 1Fh: USB Language Identifier Descriptor Type

BYTE	NAME	DESCRIPTION
1	USB_LANG_TYP	USB language ID string descriptor type as defined by Section 9.6.7 "String" of the USB 2.0 Specification (Revision 2.0, 2000). This field is the "bDescriptorType" which is a constant value associated with a string descriptor type.

8.4.1.8 20h: USB Language Identifier Least Significant Byte

BYTE	NAME	DESCRIPTION
2	USB_LANG_ID _LSB	English language code = '0409'. See Note 8.3 to reference additional language ID's defined by the USB-IF.

8.4.1.9 21h: USB Language Identifier Most Significant Byte

BYTE	NAME	DESCRIPTION
3	USB_LANG_ID _MSB	English language code = '0409'. See Note 8.3 to reference additional language ID's defined by the USB-IF.

8.4.1.10 22h: USB Manufacturer String Descriptor Length

BYTE	NAME	DESCRIPTION
0	USB_MFR_STR _LEN	USB manufacturer string descriptor length as defined by Section 9.6.7 "String" of the USB 2.0 Specification (Revision 2.0, 2000). This field is the "bLength" which describes the size of the string descriptor (in bytes).

8.4.1.11 23h: USB Manufacturer String Descriptor Type

BYTE	NAME	DESCRIPTION
1	USB_MFR_STR _TYP	USB manufacturer string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

8.4.1.12 24h-31h: USB Manufacturer String Option

BYTE	NAME	DESCRIPTION
15:2	USB_MFR_STR	The maximum string length is 28 characters.

8.4.1.13 32h-5Dh: Reserved

BYTE	NAME	DESCRIPTION
59:16	Reserved	Reserved.

8.4.1.14 5Eh: USB Product String Descriptor Length

BYTE	NAME	DESCRIPTION
0	USB_PRD_STR _LEN	USB product string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes).

8.4.1.15 5Fh: USB Product String Descriptor Type

BYTE	NAME	DESCRIPTION
1	USB_PRD_STR _TYP	USB product string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

8.4.1.16 60h-99h: USB Product String Option

BYTE	NAME	DESCRIPTION
59:2	USB_PRD_STR	This string will be used during the USB enumeration process in the Windows® operating system. Maximum string length is 28 characters.

8.4.1.17 9Ah: USB BmAttribute (1 byte)

BIT	NAME	DESCRIPTION
7:0	USB_BM_ATT	Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA) or bus-powered (limited to 100 mA maximum power prior to being configured by the host controller). When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 Specification is not violated. When configured as a self-powered device, <1 mA of current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. **80 = Bus-powered operation (default)** C0 = Self-powered operation A0 = Bus-powered operation with remote wake-up E0 = Self-powered operation with remote wake-up

8.4.1.18 9Bh: USB MaxPower (1 byte)

BIT	NAME	DESCRIPTION
7:0	USB_MAX_PWR	USB Max Power per the USB 2.0 Specification. Do NOT set this value greater than 100 mA.

8.4.1.19 9Ch-9Fh: Attribute Byte Descriptions

BYTE	BYTE NAME	BIT	DESCRIPTION
0	ATT_LB	3:0	Always reads ‘0’.
		4	Inquire Manufacturer and Product ID Strings ‘1’ - Use the Inquiry Manufacturer and Product ID Strings. ‘0’ (default) - Use the USB Descriptor Manufacturer and Product ID Strings.
		5	Always reads ‘0’.
		6	Reverse SD Card Write Protect Sense ‘1’ (default) - SD cards will be write protected when SW_nWP is high, and writable when SW_nWP is low. ‘0’ - SD cards will be write protected when SW_nWP is low, and writable when SW_nWP is high.
		7	Extended Configuration Enable '1' - This bit must be set to '1' to enable editing, updating, and reading from registers 100h-17Fh. '0' - The internal configuration is loaded. When this bit is not set (and it equals '0'). It will not read from registers 100h-17Fh.
1	ATT_HLB	3:0	Always reads ‘0’.
		4	Activity LED True Polarity ‘1’ - Activity LED to Low True. ‘0’ (default) - Activity LED polarity to High True.
		5	Common Media Insert / Media Activity LED ‘1’ - The activity LED will function as a common media inserted/media access LED. ‘0’ (default) - The activity LED will remain in its idle state until media is accessed.
		6	Always reads ‘0’.
		7	Reverse SD2 Card Write Protect Sense ‘1’ (default) - SD cards in LUN 1 will be write protected when SW_nWP is high, and writable when SW_nWP is low. ‘0’ - SD cards in LUN 1 will be write protected when SW_nWP is low, and writable when SW_nWP is high.

BYTE	BYTE NAME	BIT	DESCRIPTION
2	ATT_LHB	0	Attach on Card Insert / Detach on Card Removal '1' - Attach on Insert is enabled. '0' (default) - Attach on Insert is disabled.
		1	Always reads '0'.
		2	Enable Device Power Configuration '1' - Custom Device Power Configuration stored in the NVSTORE is used. '0' (default) - Default Device Power Configuration is used.
		7:3	Always reads '0'.
3	ATT_HB	6:0	Always reads '0'.
		7	xD Player Mode

8.4.2 A0h-A7h: Device Power Configuration

The USB4640/USB4640i has one internal FET which can be utilized for card power. This section describes the default internal configuration. The settings are stored in NVSTORE and provide the following features:

1. A card can be powered by an external FET or by an internal FET.

2. The power limit can be set to 100 mA or 200 mA (Default) for the internal FET.

Each media uses two bytes to store its device power configuration. Bit 3 selects between internal or external card power FET options. For internal FET card power control, bits 0 through 2 are used to set the power limit. The "Device Power Configuration" bits are ignored unless the "Enable Device Power Configuration" bit is set. See Section 8.4.1.19, "9Ch-9Fh: Attribute Byte Descriptions," on page 36.

8.4.2.1 A0h-A1h: Memory Stick Device Power Configuration

FET	TYPE	BITS	BIT TYPE	DESCRIPTION
0	FET Lo Byte MS_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** MS_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

8.4.2.2 A2h-A3h: Not Applicable

BYTE	NAME	DESCRIPTION
1:0	Not Applicable	Not applicable.

8.4.2.3 A4h-A5h: Smart Media Device Power Configuration

FET	TYPE	BITS	BIT TYPE	DESCRIPTION
0	FET Lo Byte SM_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** SM_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

8.4.2.4 A6h-A7h: Secure Digital Device Power Configuration

FET	TYPE	BITS	BIT TYPE	DESCRIPTION
0	FET Lo Byte SD_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** SD_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

8.4.2.5 A8h: LED Blink Interval

BYTE	NAME	DESCRIPTION
0	LED_BLK_INT	The blink rate is programmable in 50 ms intervals. The high bit (7) indicates an idle state: ‘0’ - Off ‘1’ - On The remaining bits (6:0) are used to determine the blink interval up to a max of 128 x 50 ms.

8.4.2.6 A9h: LED Blink Duration

BYTE	NAME	DESCRIPTION
1	LED_BLK_DUR	LED Blink After Access. This byte is used to designate the number of seconds that the GPIO1 LED will continue to blink after a drive access. Setting this byte to "05" will cause the GPIO 1 LED to blink for 5 seconds after a drive access.

8.4.3 Device ID Strings

These bytes are used to specify the LUN descriptor returned by the device. These bytes are used in combination with the device to LUN mapping bytes in applications where the OEM wishes to reorder and rename the LUNs. If multiple devices are mapped to the same LUN (a COMBO LUN), then the CLUN#_ID_STR will be used to name the COMBO LUN instead of the individual device strings. When applicable, the "SM" value will be overridden with xD once an xD-Picture Card has been identified.

8.4.3.1 AAh-B0h: Device 0 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV0_ID_STR	Not applicable.

8.4.3.2 B1h-B7h: Device 1 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV1_ID_STR	This ID string is associated with the Memory Stick device.

8.4.3.3 B8h-BEh: Device 2 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV2_ID_STR	This ID string is associated with the Smart Media (Note 8.2) device.

8.4.3.4 BFh-C5h: Device 3 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV3_ID_STR	This ID string is associated with the Secure Digital / MultiMediaCard device.

8.4.3.5 C6h-CDh: Inquiry Vendor String

BYTE	NAME	DESCRIPTION
7:0	INQ_VEN_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

8.4.3.6 CEh-D2h: Inquiry Product String

BYTE	NAME	DESCRIPTION
4:0	INQ_PRD_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

8.4.3.7 D3h: Dynamic Number of LUNs

BIT	NAME	DESCRIPTION
7:0	DYN_NUM_LUN	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to "FF", the program assumes that you are using the default value and icons will be configured per the default configuration.

8.4.3.8 D4h-D7h: Device to LUN Mapping

BYTE	NAME	DESCRIPTION
3:0	DEV_LUN_MAP	These registers map a device controller (SD/MMC, SM (Note 8.2), and MS) to a Logical Unit Number (LUN). The device reports the mapped LUNs to the USB host in the USB descriptor during enumeration. The icon installer associates custom icons with the LUNs specified in these fields. Setting a register to "FF" indicates that the device is not mapped. Setting all of the DEV_LUN_MAP registers for all devices to "FF" forces the use of the default mapping configuration. Not all configurations are valid. Valid configurations depend on the hardware, packaging, and OEM board layout. The number of unique LUNs mapped must match the value in the Section 8.4.3.7, "D3h: Dynamic Number of LUNs," on page 40.

8.4.3.9 D8h-DDh: Reserved

BYTE	NAME	DESCRIPTION
2:0	Reserved	Reserved.

8.4.4 Hub Controller Configurations

8.4.4.1 DEh: Vendor ID (LSB)

BIT	BYTE NAME	DESCRIPTION
7:0	VID_LSB	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementer's Forum).

8.4.4.2 DFh: Vendor ID (MSB)

BIT	BYTE NAME	DESCRIPTION
7:0	VID_MSB	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementer's Forum).

8.4.4.3 E0h: Product ID (LSB)

BIT	NAME	DESCRIPTION
7:0	PID_LSB	Least Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product.

8.4.4.4 E1h: Product ID (MSB)

BIT	NAME	DESCRIPTION
7:0	PID_MSB	Most Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product.

8.4.4.5 E2h: Device ID (LSB)

BIT	NAME	DESCRIPTION
7:0	DID_LSB	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD (binary coded decimal) format.

8.4.4.6 E3h: Device ID (MSB)

BIT	NAME	DESCRIPTION
7:0	DID_MSB	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format.

8.4.4.7 E4h: Configuration Data Byte 1 (CFG_DAT_BYT1)

BIT	NAME	DESCRIPTION
7	SELF_BUS_PWR	Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA) or bus-powered (limited to 100 mA maximum power prior to being configured by the host controller). When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated. When configured as a self-powered device, <1 mA of current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. ‘0’ = Bus-powered operation ‘1’ = Self-powered operation
6	Reserved	Reserved
5	HS_DISABLE	Hi-Speed Disable: Disables the capability to attach as either a Hi-/Full-Speed device, and forces attachment as Full-Speed only (i.e. no Hi-Speed support). ‘0’ = Hi-/Full-Speed ‘1’ = Full-Speed-Only (Hi-Speed disabled!)

BIT	NAME	DESCRIPTION
4:3	Reserved	Reserved
2:1	CURRENT_SNS	Over-Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a per port or ganged basis is dependent upon the hardware implementation. ‘00’ = Ganged sensing (all ports together) ‘01’ = Individual (port-by-port) ‘1x’ = Over-current sensing not supported (must only be used with bus-powered configurations!)
0	PORT_PWR	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is dependent upon the hardware implementation. ‘0’ = Ganged switching (all ports together) ‘1’ = Individual port-by-port switching

8.4.4.8 E5h: Configuration Data Byte 2 (CFG_DAT_BYT2)

BIT	NAME	DESCRIPTION
7:6	Reserved	Reserved
5:4	OC_TIMER	OverCurrent Timer: Over-current timer delay. ‘00’ = 50 ns ‘01’ = 100 ns ‘10’ = 200 ns ‘11’ = 400 ns
3	COMPOUND	Compound Device: Allows OEM to indicate that the hub is part of a compound device (per the USB 2.0 Specification). The applicable port(s) must also be defined as having a “non-removable device”. **Note:** When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. ‘0’ = No ‘1’ = Yes, the hub is part of a compound device
2:0	Reserved	Reserved

8.4.4.9 E6h: Configuration Data Byte 3 (CFG_DAT_BYT3)

BIT	NAME	DESCRIPTION
7:4	Reserved	Reserved

BIT	NAME	DESCRIPTION
3	PRTMAP_EN	Port Mapping Enable: Selects the method used by the hub to assign port numbers and disable ports. '0' = Standard Mode. Strap options or the following registers are used to define which ports are enabled, and the ports are mapped as port 'n' on the hub is reported as port 'n' to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host. Register 300Ah: Port disable for self-powered operation (Reset = 0x00). Register 300Bh: Port disable for bus-powered operation (Reset = 0x00). '1' = Port Map mode. The mode enables remapping via the registers defined below. Register 30FBh: Port Map 12 (Reset = 0x00) Register 30FCh: Port Map 3 (Reset = 0x00)
2:0	Reserved	Reserved

8.4.4.10 E7h: Non-Removable Device

BIT	BYTE NAME	DESCRIPTION
7:0	NR_DEVICE	Indicates which port(s) include non-removable devices. '0' = Port is removable '1' = Port is non-removable Informs the host if one of the active ports has a permanent device that is undetachable from the hub. The device must provide its own descriptor data. When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Controls physical port 3 Bit 2= Controls physical port 2 Bit 1= Controls physical port 1 Bit 0= Reserved **Note:** Bit 1 must be set to a '1' by the firmware for proper identification of the card reader as a non-removable device.

8.4.4.11 E8h: Port Disable For Self-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	PORT_DIS_SP	Disables 1 or more ports. '0' = Port is available '1' = Port is disabled During self-powered operation this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a host controller. The ports can be disabled in any order since the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Controls physical port 3 Bit 2= Controls physical port 2 Bit 1= Controls physical port 1 Bit 0= Reserved

8.4.4.12 E9h: Port Disable For Bus-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	PORT_DIS_BP	Disables 1 or more ports. '0' = Port is available '1' = Port is disabled During self-powered operation, this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Controls physical port 3 Bit 2= Controls physical port 2 Bit 1= Controls physical port 1 Bit 0 is Reserved

8.4.4.13 EAh: Max Power For Self-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	MAX_PWR_SP	Value in 2 mA increments that the hub consumes when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. **Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA.

8.4.4.14 EBh: Max Power For Bus-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	MAX_PWR_BP	Value in 2 mA increments that the hub consumes when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.

8.4.4.15 ECh: Hub Controller Max Current For Self-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	HC_MAX_C_SP	Value in 2 mA increments that the hub consumes when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA. A value of 50 (decimal) indicates 100 mA, which is the default value.

8.4.4.16 EDh: Hub Controller Max Current For Bus-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	HC_MAX_C_BP	Value in 2 mA increments that the hub consumes when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. A value of 50 (decimal) would indicate 100 mA, which is the default value.

8.4.4.17 EEh: Power-On Time

BIT	BYTE NAME	DESCRIPTION
7:0	PWR_ON_TIME	The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is adequate on that port. If the host requests the power-on time, the system software uses this value to determine how long to wait before accessing a powered-on port.

8.4.4.18 EFh: Boost_Up

BIT	NAME	DESCRIPTION
7:2	Reserved	Reserved
1:0	BOOST_IOUT	USB electrical signaling drive strength boost bit for the upstream port 'A'. '00' = Normal electrical drive strength = No boost '01' = Elevated electrical drive strength = Low (approximately 4% boost) '10' = Elevated electrical drive strength = Medium (approximately 8% boost) '11' = Elevated electrical drive strength = High (approximately 12% boost) **Note:** "Boost" could result in non-USB compliant parameters. OEM should use a '00' value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.

8.4.4.19 F0h: Boost_3:0

BIT	NAME	DESCRIPTION
7:6	Reserved	Reserved
5:4	BOOST_IOUT_3	Upstream USB electrical signaling drive strength boost bit for downstream port '3'. '00' = Normal electrical drive strength = No boost '01' = Elevated electrical drive strength = Low (approximately 4% boost) '10' = Elevated electrical drive strength = Medium (approximately 8% boost) '11' = Elevated electrical drive strength = High (approximately 12% boost)
3:2	BOOST_IOUT_2	Upstream USB electrical signaling drive strength boost bit for downstream port '2'. '00' = Normal electrical drive strength = No boost '01' = Elevated electrical drive strength = Low (approximately 4% boost) '10' = Elevated electrical drive strength = Medium (approximately 8% boost) '11' = Elevated electrical drive strength = High (approximately 12% boost) **Note:** "Boost" could result in non-USB Compliant parameters. OEM should use a '00' value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.
1:0	Reserved	Always reads '0'.

8.4.4.20 F1h: Port Swap

BIT	BYTE NAME	DESCRIPTION
7:0	PRT_SWP	Swaps the upstream and downstream USB DP and DM pins for ease of board routing to devices and connectors. '0' = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. '1' = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Controls physical port 3 Bit 2= Controls physical port 2 Bit 1= Reserved Bit 0= Controls physical port 0

8.4.4.21 F2h: Port Map 12

<table>
<tr><th>BIT</th><th>BYTE NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7:0</td><td>PRTM12</td><td>PortMap register for ports 1 & 2

When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub reported having.

The host's port number is referred to as “logical port number” and the physical port on the hub is the “physical port number”. When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).

Note: The OEM must ensure that contiguous logical port numbers are used, starting from number ‘1’ up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.

Table 8.5 Port Map Register for Ports 1 & 2
<table>
<tr><td>Bit [7:4]</td><td>‘0000’</td><td>Physical port 2 is disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical port 2 is mapped to Logical port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical port 2 is mapped to Logical port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical port 2 is mapped to Logical port 3</td></tr>
<tr><td></td><td>‘0100’ to ‘1111’</td><td>Illegal; Do not use</td></tr>
<tr><td>Bit [3:0]</td><td>‘0000’</td><td>Physical port 1 is disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical port 1 is mapped to Logical port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical port 1 is mapped to Logical port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical port 1 is mapped to Logical port 3</td></tr>
<tr><td></td><td>‘0100’ to ‘1111’</td><td>Illegal; Do not use</td></tr>
</table></td></tr>
</table>

8.4.4.22 F3h: Port Map 3

BIT	BYTE NAME	DESCRIPTION
7:0	PRTM3	PortMap register for port 3. When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub reported having. The host's port number is referred to as “logical port number” and the physical port on the hub is the “physical port number”. When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host). **Note:** The OEM must ensure that contiguous logical port numbers are used, starting from number ‘1’ up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.

Table 8.6 Port Map Register for Port 3

Bit [7:4]	‘0000’	Reserved
	‘0001’	Reserved
	‘0010’	Reserved
	‘0011’	Reserved
	‘0100’ to ‘1111’	Illegal; Do not use
Bit [3:0]	‘0000’	Physical port 3 is disabled
	‘0001’	Physical port 3 is mapped to Logical port 1
	‘0010’	Physical port 3 is mapped to Logical port 2
	‘0011’	Physical port 3 is mapped to Logical port 3
	‘0100’ to ‘1111’	Illegal; Do not use

8.4.4.23 F4h-F6h: Reserved

BYTE	BYTE NAME	DESCRIPTION
6:0	Reserved	Reserved.

8.4.4.24 F7h-FBh: Not Applicable

BIT	BYTE NAME	DESCRIPTION
7:0	Not Applicable	Not applicable.

8.4.4.25 FCh-FFh: Non-Volatile Storage Signature

BYTE	NAME	DESCRIPTION
3:0	NVSTORE_SIG	This signature is used to verify the validity of the data in the first 256 bytes of the configuration area. The signature must be set to ‘ATA2’ for USB4640/USB4640i.

8.4.5 Internal Flash Media Controller Extended Configurations

Enable Registers 100h - 17Fh by setting bit 7 of bmAttribute.

8.4.5.1 100h-106h: Combo LUN 0 Identifier String

BYTE	NAME	DESCRIPTION
6:0	CLUN0_ID_STR	If the device to LUN mapping bytes have configured this LUN to be a combo LUN, then these strings will be used to identify the LUN rather than the device identifier strings.

8.4.5.2 107h-17Bh: Not Applicable

BYTE	NAME	DESCRIPTION
116:0	Not Applicable	Not Applicable.

8.4.5.3 17Ch -17Fh: Non-Volatile Storage Signature for Extended Configuration

BYTE	NAME	DESCRIPTION
3:0	NVSTORE_SIG2	This signature is used to verify the validity of the data in the upper 256 bytes if a 512 byte EEPROM is used, otherwise this bank is a read-only configuration area. The signature must be set to 'ecf1'.

8.4.6 I^2C EEPROM

The I^2C EEPROM interface implements a subset of the I^2C Master Specification (Please refer to the Philips Semiconductor Standard I^2C-Bus Specification for details on I^2C bus protocols). The device’s I^2C EEPROM interface is designed to attach to a single “dedicated” I^2C EEPROM, and it conforms to the Standard-mode I^2C Specification (100 kbps transfer rate and 7-bit addressing) for protocol and electrical compatibility.

Note: Extensions to the I^2C Specification are not supported. The device acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

8.4.6.1 Implementation Characteristics

The device will only access an EEPROM using the sequential read protocol.

8.4.6.2 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the SPI_DO / GPIO5 / SDA / SPI_SPD_SEL and SPI_CLK / GPIO4 / SCL lines (per SMBus 1.0 Specification and EEPROM manufacturer guidelines) to VDD33 in order to assure proper operation.

8.4.7 In-Circuit EEPROM Programming

The EEPROM can be programmed via automatic test equipment (ATE). Pulling nRESET low tri-states the device's EEPROM interface and allows an external source to program the EEPROM.

8.5 Default Configuration Option

The SMSC device can be configured via its internal default configuration. Please see Section 8.3.2, "EEPROM Data Descriptor" for specific details on how to enable default configuration. Please refer to Table 8.1 for the internal default values that are loaded when this option is selected.

8.6 Reset

There are three different resets that the device experiences. One is a hardware reset from the internal power-on reset (POR) circuit, another reset is via the nRESET pin, and the third is a USB bus reset.

8.6.1 Internal POR Hardware Reset

All reset timing parameters are guaranteed by design.

8.6.2 External Hardware nRESET

A valid hardware reset is defined as assertion of nRESET for a minimum of 1 µs after all power supplies are within operating range. While reset is asserted, the device (and its associated external circuitry) consumes less than 500 µA of current.

Assertion of nRESET (external pin) causes the following:

1. All downstream ports are disabled and PRTCTL power to downstream devices is removed.
2. The PHYs are disabled and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00h).
5. The external crystal oscillator is halted.
6. The PLL is halted.

8.6.2.1 nRESET for EEPROM Configuration

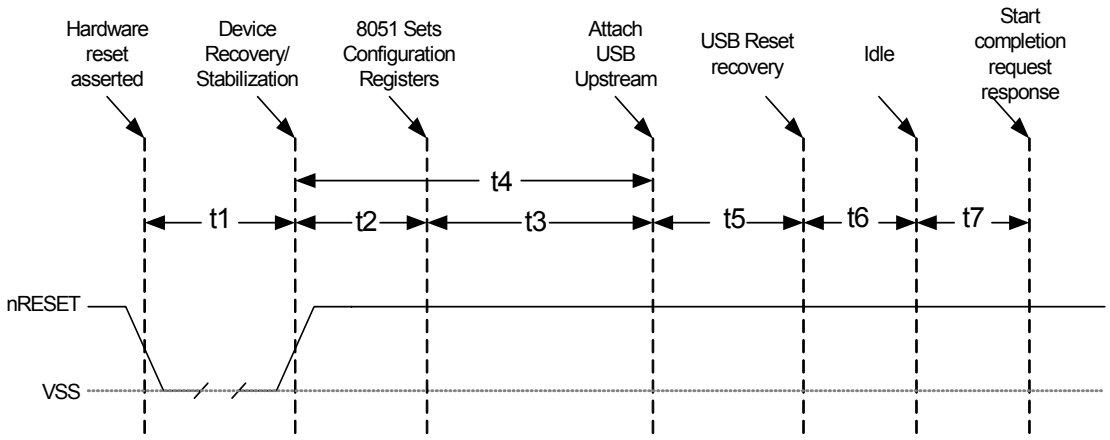


Figure 8.1 nRESET Timing for EEPROM Mode

Table 8.7 nRESET Timing for EEPROM Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nRESET asserted	1			µsec
t2	Device recovery/stabilization			500	µsec
t3	8051 programs device configuration		20	50	msec
t4	USB attach (See **Note**)			100	msec
t5	Host acknowledges attach and signals USB reset	100			msec
t6	USB idle		Undefined		msec
t7	Completion time for requests (with or without data stage)			5	msec

Note: All power supplies must have reached the operating levels mandated in Chapter 10, DC Parameters, prior to (or coincident with) the assertion of nRESET.

8.6.3 USB Bus Reset

In response to the upstream port signaling a reset to the device, the device does the following:

Note: The device does not propagate the upstream USB reset to downstream devices.

1. Sets default address to ‘0’.
2. Sets configuration to: Unconfigured.
3. Negates PRTCTL[3:2] to all downstream ports.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence.

The host then configures the device and the device’s downstream port devices in accordance with the USB 2.0 Specification.

Chapter 9 AC Specifications

9.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

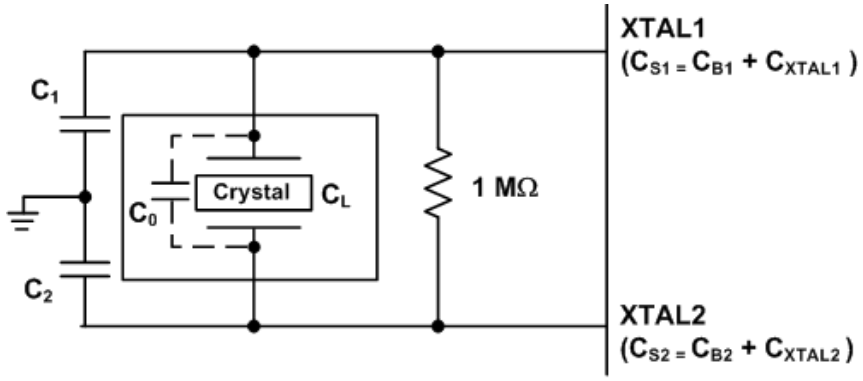


Figure 9.1 Typical Crystal Circuit

Table 9.1 Crystal Circuit Legend

SYMBOL	DESCRIPTION	IN ACCORDANCE WITH
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (See Note 9.1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	SMSC IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	SMSC IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 9.2, "Capacitance Formulas" (See Note 9.2)
C_2		

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 9.2 Capacitance Formulas

Note 9.1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to '0' for use in the calculation of the capacitance formulas in Figure 9.2, "Capacitance Formulas". However, the OEM PCB itself may present a parasitic capacitance between XTAL1 and XTAL2. For an accurate calculation of C_1 and C_2, take the parasitic capacitance between traces XTAL1 and XTAL2 into account.

Note 9.2 Each of these capacitance values is typically approximately 18 pF.

9.2 Ceramic Resonator

24 MHz ± 350 ppm

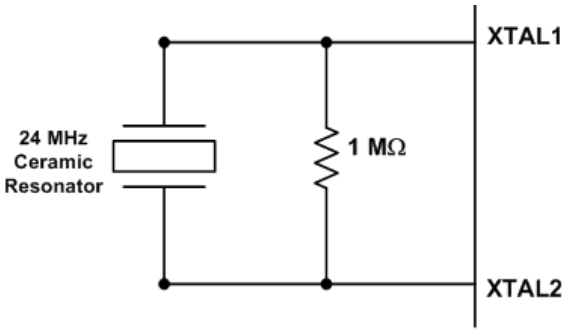


Figure 9.3 Ceramic Resonator Usage with SMSC IC

9.3 External Clock

50% Duty cycle ± 10%, 24 MHz ± 350 ppm, Jitter < 100 ps rms.

The external clock is recommended to conform to the signaling level designated in the JESD76-2 specification on 1.8 V CMOS Logic. XTAL2 should be treated as a no connect.

9.3.1 I^2C EEPROM

Frequency is fixed at 58.6 kHz ± 20%

9.3.2 USB 2.0

The SMSC device conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 Specification. Please refer to the USB 2.0 Specification for more information.

Chapter 10 DC Parameters

10.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_{STOR}	-55	150	°C	
Lead Temperature				°C	Please refer to JEDEC specification J-STD-020D.
3.3 V supply voltage	VDD33	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	(3.3 V supply voltage + 2) ≤ 6	V	
Voltage on GPIO10		-0.5	VDD33 + 0.3	V	When internal power FET operation of these pins are enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63 V indefinitely, without damage to the device as long as VDD33 is less than 3.63 V and T_A is less than 70°C.
Voltage on any signal pin		-0.5	VDD33 + 0.3	V	
Voltage on XTAL1		-0.5	3.6	V	
Voltage on XTAL2		-0.5	2.0	V	

Note: Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies the absolute maximum ratings must not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, a clamp circuit should be used.

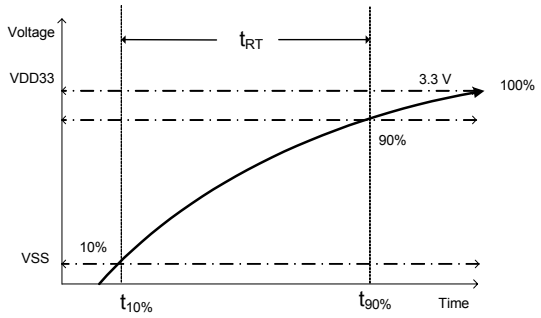


Figure 10.1 Supply Rise Time Model

10.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Commercial USB4640 Operating Temperature	T_A	0	70	°C	Ambient temperature in still air.
Industrial USB4640i Operating Temperature	T_A	-40	85	°C	Ambient temperature in still air.
3.3 V supply voltage	VDD33	3.0	3.6	V	A 3.3 V regulator with an output tolerance of 1% must be used if the output of the internal power FET's must support a 5% tolerance.
3.3 V supply rise time	t_{RT}	0	400	µs	(Figure 10.1)
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal pin		-0.3	VDD33	V	
Voltage on XTAL1		-0.3	2.0	V	
Voltage on XTAL2		-0.3	2.0	V	

10.3 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis	V_{HYSI}		420		mV	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to VDD33
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = VDD33
I/O6, I/OD6PU Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6 mA @ VDD33 = 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -6 mA @ VDD33 = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to VDD33 (Note 10.1)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
O8, O8PD, 08PU, I/O8, I/O8PD, and I/O8PU Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ VDD33 = 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -8 mA @ VDD33 = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to VDD33 (Note 10.1)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O12, I/O12, and I/O12PD Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ VDD33 = 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12 mA @ VDD33 = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to VDD33 (Note 10.1)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U						Note 10.2
I-R						Note 10.3
I/O200 Integrated Power FET for GPIO10						
High Output Current	I_{OUT}	200			mA	$Vdrop_{FET}$ = 0.46 V
Low Output Current (Note 10.4)	I_{OUT}	100			mA	$Vdrop_{FET}$ = 0.23 V
On Resistance (Note 10.4)	R_{DSON}			2.1	Ω	I_{FET} = 70 mA
Output Voltage Rise Time	t_{DSON}			800	µs	C_{LOAD} = 10 µF
Integrated Power FET Set to 100 mA						
Output Current (Note 10.4)	I_{OUT}	100			mA	$Vdrop_{FET}$ = 0.22 V
Short Circuit Current Limit	I_{SC}			140	mA	$Vout_{FET}$ = 0 V
On Resistance (Note 10.4)	R_{DSON}			2.1	Ω	I_{FET} = 70 mA
Output Voltage Rise Time	t_{DSON}			800	µs	C_{LOAD} = 10 µF
Integrated Power FET Set to 200 mA						
Output Current (Note 10.4)	I_{OUT}	200			mA	$Vdrop_{FET}$ = 0.46 V
Short Circuit Current Limit	I_{SC}			181	mA	$Vout_{FET}$ = 0 V
On Resistance (Note 10.4)	R_{DSON}			2.1	Ω	I_{FET} = 70 mA
Output Voltage Rise Time	t_{DSON}			800	µs	C_{LOAD} = 10 µF

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Supply Current Unconfigured						Note 10.6
Hi-Speed Host						
USB4640 USB4640i	$I_{CCINTHS}$ $I_{CCINTHS}$		TBD TBD	TBD TBD	mA mA	
Full Speed Host						
USB4640 USB4640i	$I_{CCINITFS}$ $I_{CCINITFS}$		TBD TBD	TBD TBD	mA mA	
Supply Current Configured Hi-Speed Host, 1 downstream port						Note 10.6
USB4640 USB4640i	I_{HCH1} I_{HCH1}		TBD TBD	TBD TBD	mA mA	
Supply Current Configured Hi-Speed Host, each additional downstream port						
USB4640 USB4640i			TBD TBD	TBD TBD	mA mA	
Supply Current Configured Full-Speed Host, 1 downstream port						
USB4640 USB4640i	I_{FCC1} I_{FCC1}		TBD TBD	TBD TBD	mA mA	
Supply Current Configured Full-Speed Host, each additional downstream port						
USB4640 USB4640i			TBD TBD	TBD TBD	mA mA	
HSIC_DAT, HSIC_STROBE Driver Impedance	I_D		TBD	TBD	Ω	Note 10.5
Supply Current Active	I_{CC}		TBD	TBD	mA	Note 10.6
Supply Current Suspend	I_{CSBY}		TBD	TBD	µA	
Supply Current Reset	I_{RST}		TBD	TBD	µA	

Note 10.1 Output leakage is measured with the current pins in high impedance.

Note 10.2 See the USB 2.0 Specification, Chapter 7, for USB DC electrical characteristics

Note 10.3 RBIAS is a 3.3 V tolerant analog pin.

Note 10.4 Output current range is controlled by program software. The software disables the FET during short circuit condition.

Note 10.5 Please refer to the USB 2.0 supplement “High-Speed Inter-Chip USB Electrical Specification Revision 1.0 as of September 23, 2007” which can be obtained from http://www.usb.org/developers/docs/docs.

Note 10.6 Typical and maximum values were characterized using the following temperature ranges:
The USB4640 supports the commercial temperature range of 0°C to +70°C
The USB4640i supports the industrial temperature range of -40°C to +85°C

10.4 Capacitance

T_A = 25°C; fc = 1 MHz; VDD33= 3.3 V

Table 10.1 Pin Capacitance

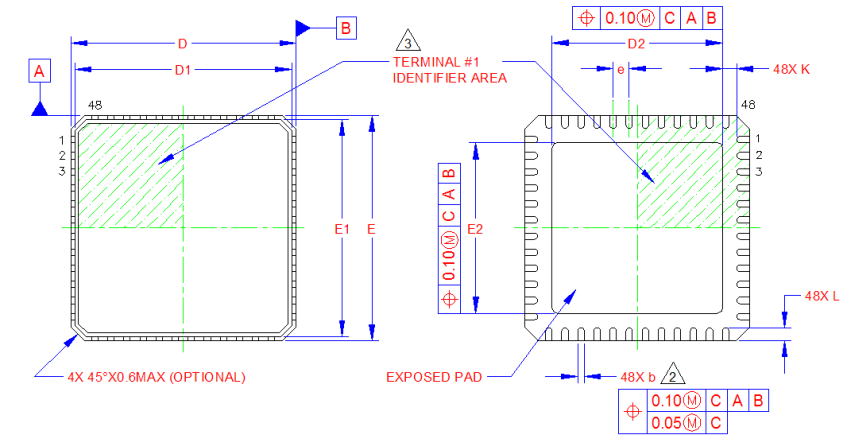
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins (except USB pins and pins under test) are tied to AC ground.
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

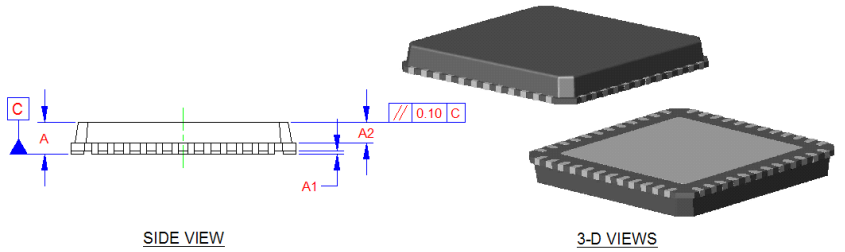
Chapter 11 GPIO Usage

Table 11.1 USB4640/USB4640i GPIO Usage

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED / TxD	LED indicator / Serial port transmit line
GPIO2	H	RxD	Serial port receive line
GPIO4	H	SCL	Serial EEPROM clock
GPIO5	H	SDA	Serial EEPROM data
GPIO6	L	SD_WP	Secure Digital card write protect assertion
GPIO10	L	CRD_PWR_CTRL	Card power control
GPIO12	L	MS_nCD	Memory Stick card detect
GPIO14	L	xD_nCD	xD-Picture card detect
GPIO15	L	SD_nCD	Secure Digital card detect

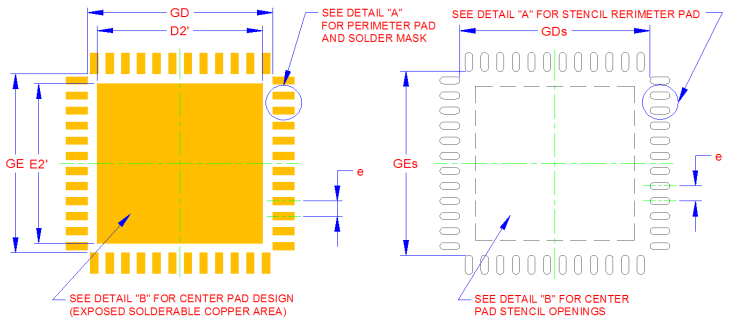
Chapter 12 Package Specifications





COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	0.85	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	-	-	0.90	-	MOLD CAP THICKNESS
D/E	6.85	7.00	7.15	-	X/Y BODY SIZE
D1/E1	6.55	6.75	6.95	-	X/Y MOLD CAP SIZE
D2/E2	5.20	5.30	5.40	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.35	-	-	-	CENTER PAD TO PIN CLEARANCE
e	0.50 BSC			-	TERMINAL PITCH

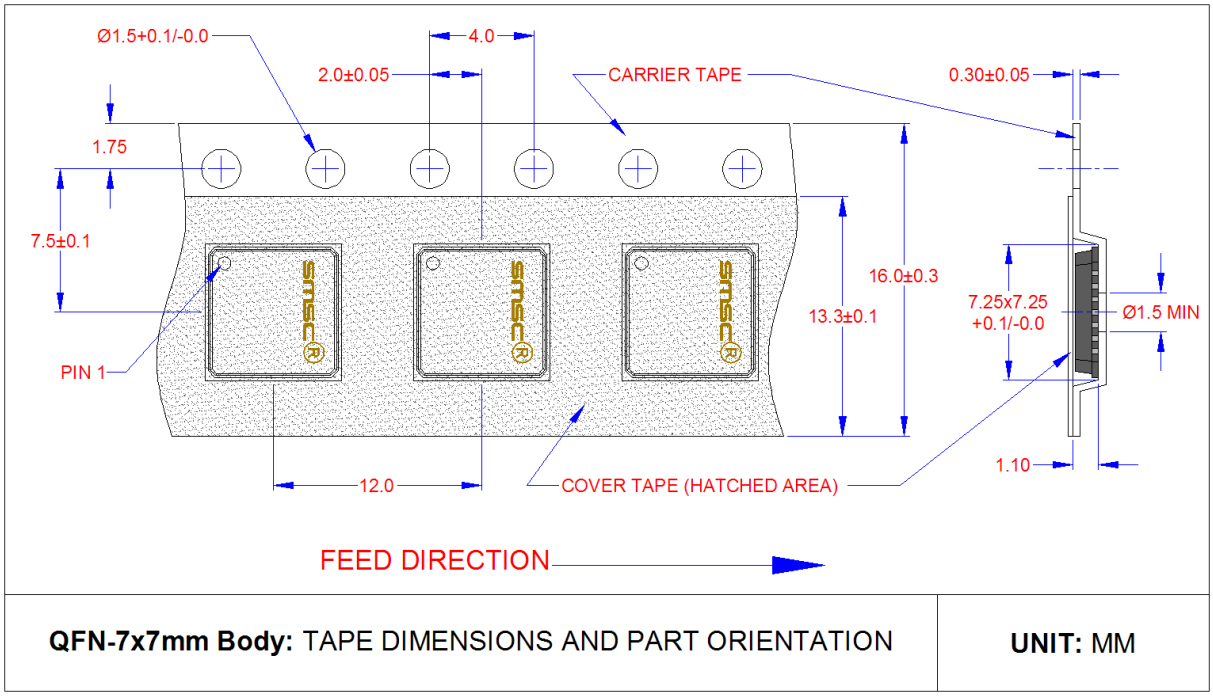
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.00	-	6.10
GDs/GEs	6.05	-	-
D2'/E2'	-	5.30	5.30
Pad: X	-	0.28	0.28
Stencil: Xs	-	0.23	0.25
Pad: Y	-	0.69	0.69
Stencil: Ys	-	0.62	0.64
e		0.50	

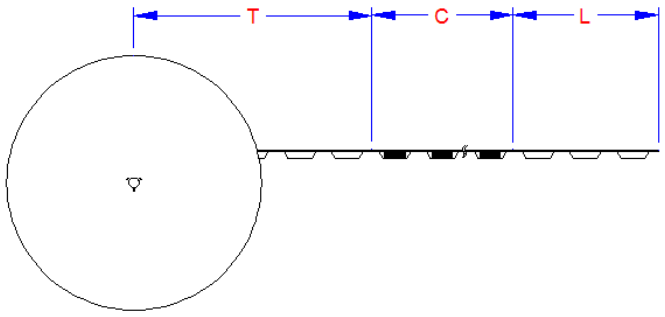
Figure 12.1 USB4640/USB4640i 48-Pin QFN

12.1 Tape and Reel Specifications



QFN-7x7mm Body: TAPE DIMENSIONS AND PART ORIENTATION	**UNIT:** MM

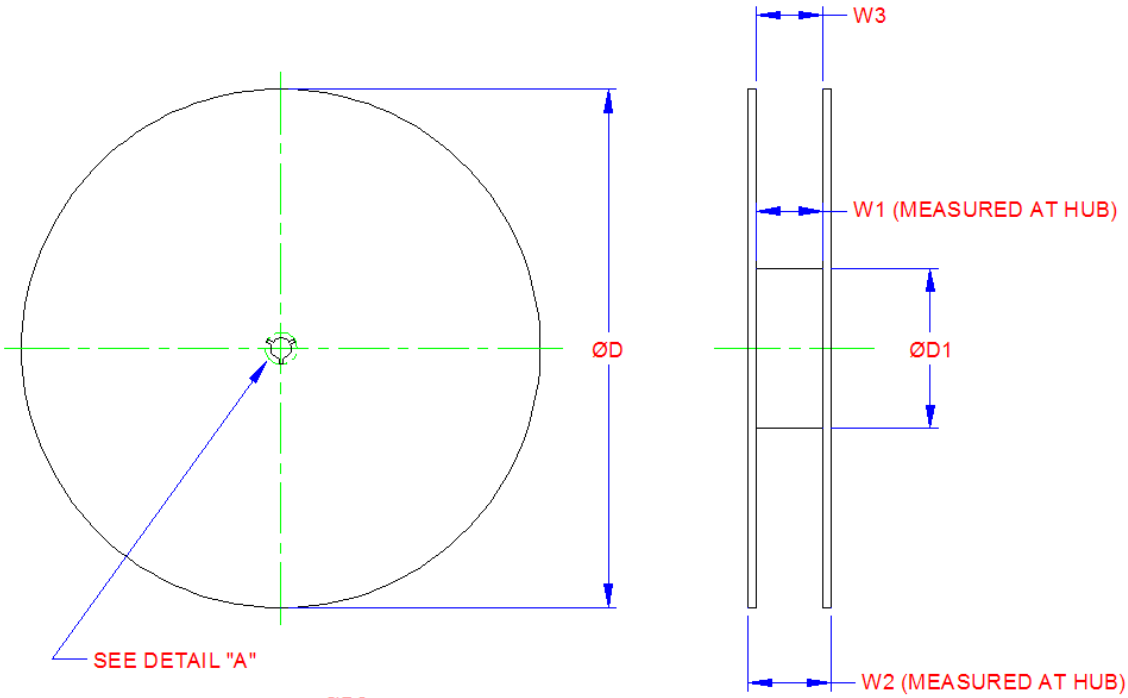
TAPE LENGTH & PART QUANTITY

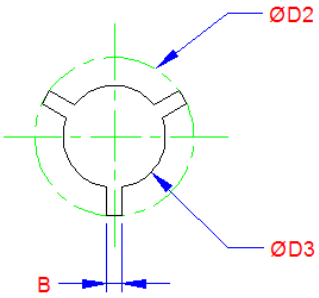


TAPE SECTIONS		
SECTION	SYM	SIZE
TRAILER	T	14 pockets (MIN)
COMPONENT	C	3000 components
LEADER	L	34 pockets (MIN)

Figure 12.2 48-Pin Package Tape Specifications

REEL PHYSICAL DIMENSIONS





DETAIL "A"

REEL DIMs for 16mm CARRIER TAPE			
PART	FEATURE	SYM	SIZE (mm)
FLANGE	DIAMETER	D	330 (+0.25/-4.00)
	SPACE between FLANGES	W1	16.4 (+2.0/-0.0)
	OVERALL WITH	W2	22.4 (MAX)
	MIN SPACE "W1" AT FLANGE EDGE	W3	16.3 (MIN)
HUB	OUTER DIAMETER	D1	102 REF
	KEY SLIT DIAMETER	D2	20.2 (MIN)
	ARBOR HOLE DIAMETER	D3	13.0 (+0.5/-0.2)
	KEY SLIT WIDTH	B	2.0 (±0.5)

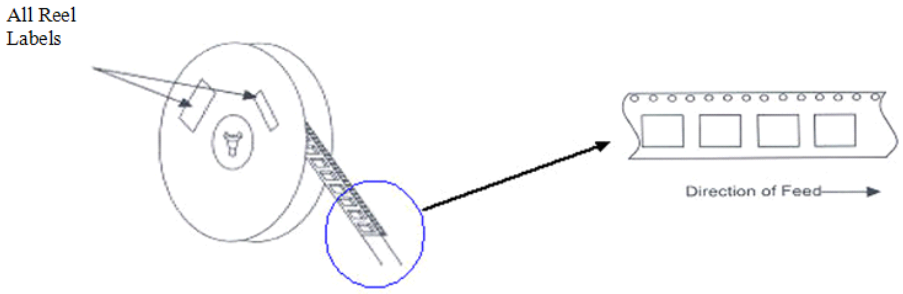


Figure 12.3 48-Pin Package Reel Specifications