

**UNISONIC TECHNOLOGIES CO., LTD** 

USB4S012

Preliminary

# 4-CHANNEL ESD SOLUTION FOR USB-HS/USB OTG/USB CHARGER INTERFACE

### DESCRIPTION

The UTC **USB4S012** is a fo ur-channel ele ctrostatic disch arge (ESD) solution for USB charger or USB on-the-g o (OTG) interface. In many cell phone applications, the USB connector is the de facto communication port for external communications like high-speed data transfer, audio signal, charging, car-kit, etc. In order to support different interfaces, the USB port needs to handle different voltage levels. For example, some chargers require the V <sub>BUS</sub> port of the USB connector to handle in excess of the n ormal V<sub>BUS</sub> voltage per USB specificat ions. The UTC **USB4S012** offers combina tions of two different clamp voltages to match the voltage toler ances of the different signal interfaces using the common USB connector.

The UTC **USB4S012** conforms to IEC61000-4-2 (Level 4) ESD. The device is offered in sp ace-saving pack ages with flow-through pin mapping.

#### FEATURES

- \* Integrated ESD Clamps for D+, D–, VBUS, and ID Pins to Provide Single-Chip ESD Protection for USB High Speed, USB-OTG, and USB Charger Interface
- \* IEC 61000-4-2 (Level 4) System Level ESD Compliance Measured at the D+, D–, and ID Pins – ±10-kV IEC 61000-4-2 Contact Discharge
- ±10-kV IEC 61000-4-2 Air-Gap Discharge
- \* 3 Amps Peak Pulse Current (8/20 $\mu s$  Pulse) for  $V_{BUS}$  and D+, D–, and ID Lines
- \* Special Snap Back Technology Allows High-voltage Tolerance During Normal Operation while Reducing the Clamp Voltage during System Level ESD Stress

- \* USB Signal Pins (D+, D–, ID)
- 0.8-pF Line Capacitance
- Tolerates 6V Signal
- \* V<sub>BUS</sub> Line (V<sub>BUS</sub>)
- 11-pF Line Capacitance
- Tolerates 20V Signal
- \* Flow-Through Pin Mapping for the High-Speed Lines Ensures Zero Additional Skew Due to Board Layout While Placing the ESD Protection Chip Near the Connector
- \* Supports Data Rates in Excess of 480Mbps
- \* Industri al T emperature Ra nge: 40°C~85°C

#### ORDERING INFORMATION

Ordering	Deekees Deekir		
Lead Free	ead Free Halogen Free		ig
USB4S012L-AG6-R USB4S	0 12G-AG6-R	SOT-26	Tape Reel

USB4S012 <u>L-AG6-R</u>			
(1)Packing Type	(1) R: Tape Reel		
(2)Package Type	(2) AG6 : SOT-26		
(3)Halogen Free	(3) L: Lead Free, G: Halogen Free		



### MARKING INFORMATION

PACKAGE	MARKING		
SOT-26	$\begin{array}{c} 6 & 5 & 4 \\ \hline 0 & 12 \\ \bullet & \\ \hline & \\ \hline & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\$		

#### ■ PIN CONFIGURATION



### ■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V <sub>BUS</sub>	ESD clamp for high-voltage tolerant VBUS line(s)
2	NC	Not internally connected
3	GND	Ground
4	ID	Provides ESD protection to the high-speed differential data lines
5	D-	Provides ESD protection to the high-speed differential data lines
6	D+	Provides ESD protection to the high-speed differential data lines

### BLOCK DIAGRAM





QW-R215-010.a

## Preliminary

#### ■ ABSOLUTE MAXIMUM RATING over operating free-air temperature range (unless otherwise noted)

PARAMETER SYMBOL		RATINGS	UNIT
V <sub>BUS</sub> Voltage Tolerance	V <sub>BUS</sub> pin	-0.3~20	V
IO Voltage Tolerance	D+, D–, I <sub>D</sub> pins	-0.3~6	V
IEC 61000-4-2 Contact Discharge	D+, D–, ID	±10	kV
IEC 61000-4-2 Air-Gap Discharge	D+, D–, ID	±10	kV
IEC 61000-4-2 Contact Discharge	V <sub>BUS</sub> pin	±10	kV
IEC 61000-4-2 Air-Gap Discharge	V <sub>BUS</sub> pin	±9	kV
Peak pulse power (tp = 8/20 μs)	D+, D–, ID, V <sub>BUS</sub> pins	60 W	
Peak pulse current (tp = 8/20 μs)	D+, D–, ID, V <sub>BUS</sub> pins	3	А
Storage Temperature Range	T <sub>STG</sub> -65∼	125	°C
Operating Free-Air Temperature Range	T <sub>A</sub> -40~	85	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

#### ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER SYMBOL		-	TEST CONDITIONS		TYP	MAX	UNIT
V <sub>BUS</sub> Operating Current	I <sub>VBUS</sub>	V <sub>BUS</sub> =5V	D+ D– ID pins open				μA
		V <sub>BUS</sub> =19V			0.1	0.5	
IO Port Current	I <sub>IO</sub>	V <sub>IO</sub> =2.5V, V <sub>BUS</sub> =5V	D+, D–, ID pins		0.1	0.5	μA
Diode Forward Voltage	VD	I <sub>IO</sub> =8mA	D+, D–, ID pins (lower clamp diode)	0.6 0.	8 0.95		V
V <sub>BUS</sub> Pin Capacitance	CVBUS	V <sub>BUS</sub> =5V			11	15	pF
IO Capacitance	CIO	V <sub>IO</sub> =2.5V	D+, D–, ID pins (DRY package)		0.8	1	pF
Dynamic Resistance	R <sub>dyn</sub> —	I <sub>IO</sub> =1.5A	D+, D–, ID, and V <sub>BUS</sub> pins, including central clamp dioded during positive ESD pulse		1.2		0
		I <sub>IO</sub> =1A	D+, D–, ID, and V <sub>BUS</sub> pins, including central clamp diode during negative ESD pulse		1		Ω
Breakdown Voltage	V	1 - 1 - 1 0	D+, D–, ID pins	6	9		Ň
	VBR	IIO=IIIIA	V <sub>BUS</sub> pin(s)	20	24		v



# TYPICAL APPLICATION CIRCUIT



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