USBULC6-2F3

IPAD™

Dual ultra low capacitance protection for high speed USB

Main application

- Hi-Speed USB port in wireless handsets (up to 480 Mb/s according to USB 2.0 High Speed Specification)

Features

- Ultra low diode capacitance (1.2 pF max)
- Two data lines (D+ and D-) protected against 15 kV ESD
- Breakdown Voltage V_{BR} = 6.0 V min
- Flip-Chip 400 µm pitch, lead-free
- Very low leakage current
- Very small PCB area
- RoHS compliant

Description

The USBULC6-2F3 is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces.

Its ultra low line capacitance secures a high level of signal integrity without compromizing the protection of downstream sensitive chips against the most stringently characterized ESD strikes.

Benefits

- Minimized impact on rise and fall times for maximum data integrity
- Low PCB space occupation
- Higher reliability offered by monolithic integration

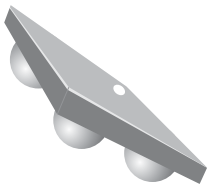
Complies with the following standards:

IEC 61000-4-2: 15 kV (air discharge)

8 kV (contact discharge)

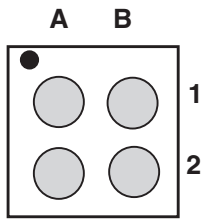
MIL STD 883G - Method 3015.7

25 kV (Human body model)

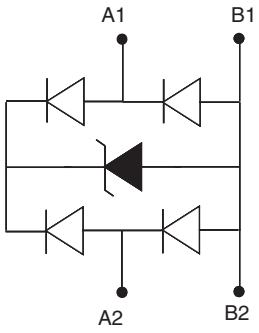


Flip-Chip
(4 Bumps)

Pin configuration (bump side)



Configuration



Note: B1 and B2 bumps must be grounded on the PCB together

Order code

Part Number	Marking
USBULC6-2F3	EH

TM: IPAD is a trademark of STMicroelectronics

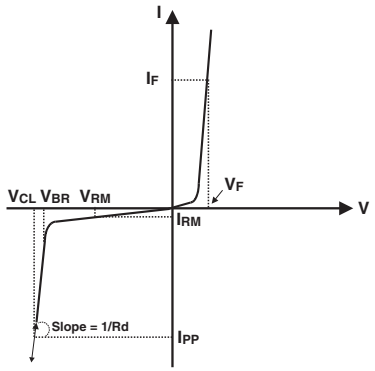
1 Characteristics

Table 1. Absolute Maximum Ratings (T_{amb} = 25° C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge	15 8	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)	60	W
T_j	Maximum junction temperature	125	° C
T_{op}	Operating temperature range	-30 to + 85	° C
T_{stg}	Storage temperature range	-55 to +150	° C

Table 2. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6		9	V
I_{RM}	V_{RM} = 3 V			100	nA
R_d	Exponential wave form 8/20 µs, I_{pp} = 1 to 5 A		1.6		Ω
αT	I_R = 1 mA			5	10^{-4}/° C
C_{line}	V_{LINE} = 0 V, V_{OSC} = 30 mV, F = 1 MHz			1.2	pF

Figure 1. Application diagram

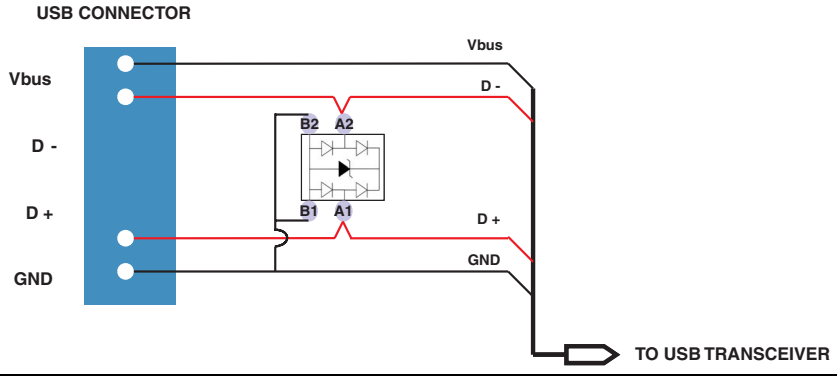


Figure 2. Eye diagram, board only (according to USB High Speed)

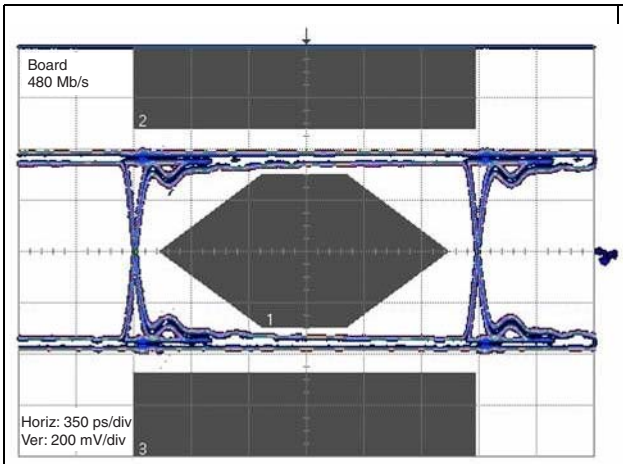


Figure 3. Eye diagram, board with USBULC6-2F3 (according to USB 2.0 High Speed)

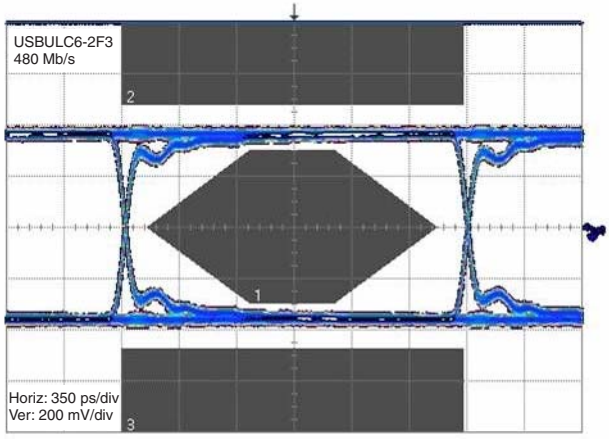


Figure 4. ESD response to IEC 61000-4-2 (+15 kV air discharge)

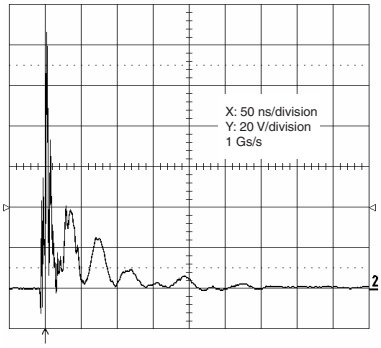


Figure 5. ESD response to IEC 61000-4-2 (-15 kV air discharge

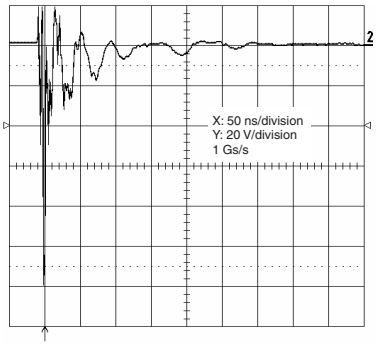


Figure 6. Junction capacitance versus frequency (typical values)

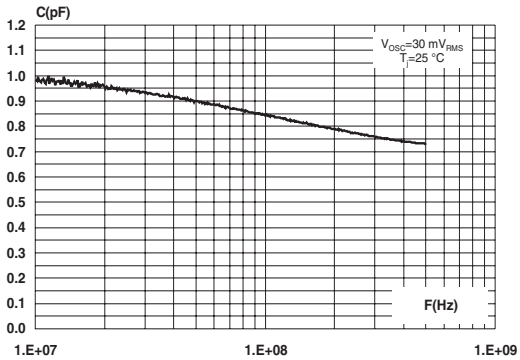


Figure 7. Analog crosstalk measurements

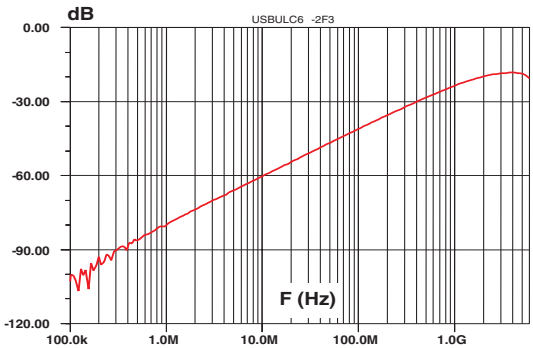


Figure 8. S21 (dB) attenuation measurements

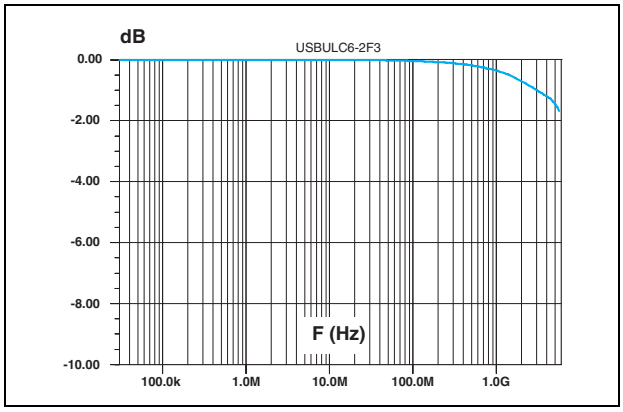


Figure 9. Digital crosstalk

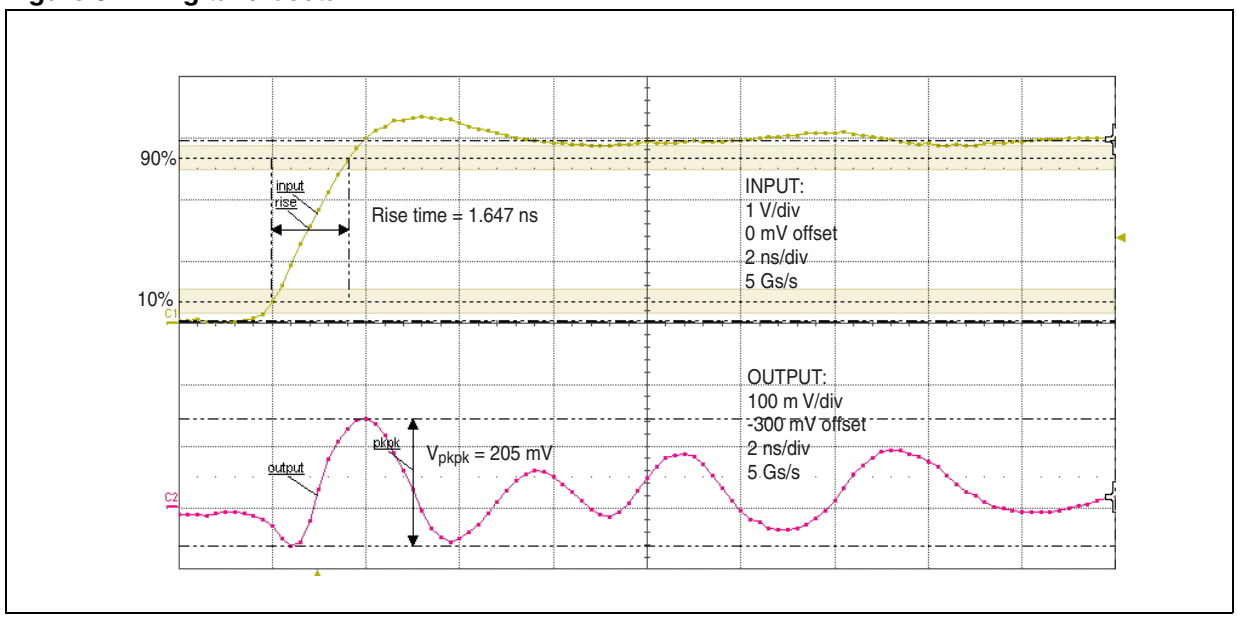


Figure 10. Relative variation of peak pulse power versus initial junction temperature

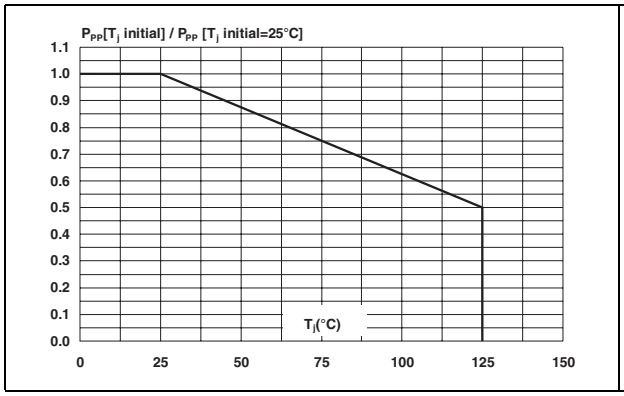


Figure 11. Peak pulse power versus exponential pulse duration

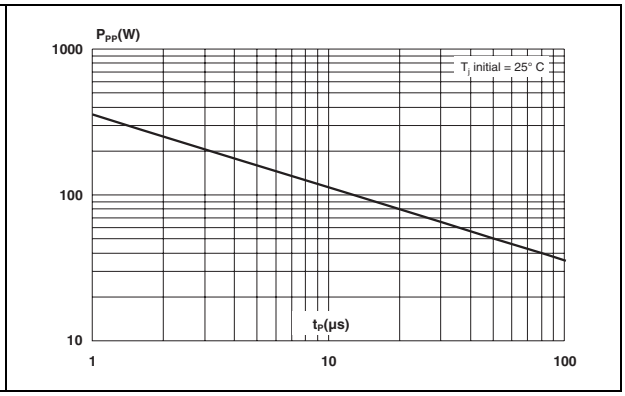


Figure 12. Clamping voltage versus peak pulse current (typical values, exponential waveform)

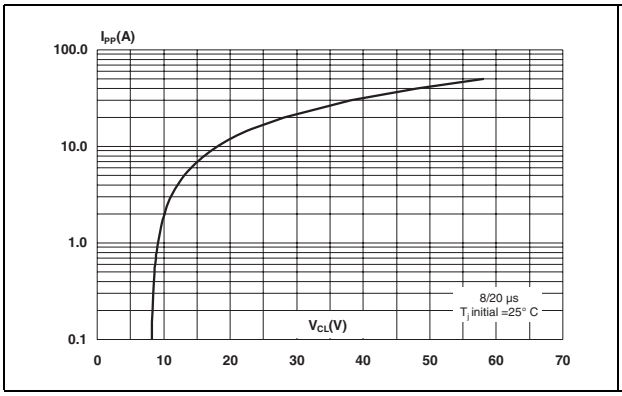
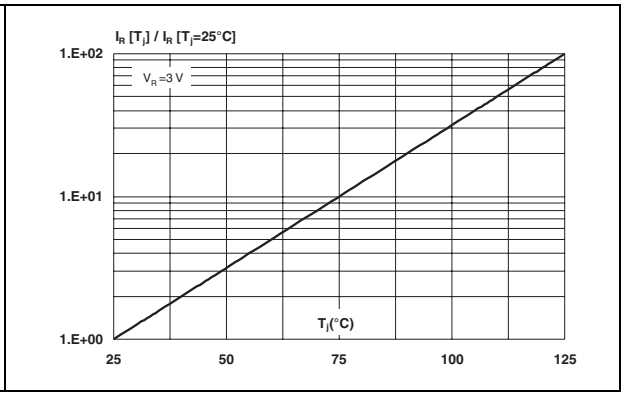


Figure 13. Relative variation of leakage current versus junction temperature (typical values)



2 Ordering information scheme

USB ULC 6 - 2 F3

USB protection

Ultra Low Capacitance

Breakdown voltage
6 = 6 V_{MIN}

Number of lines
2 = 2 lines

Package
F = Flip-Chip
3: Lead free, Pitch = 400 µm, Bump = 255 µm

3 Package information

Figure 14. Flip-Chip dimensions

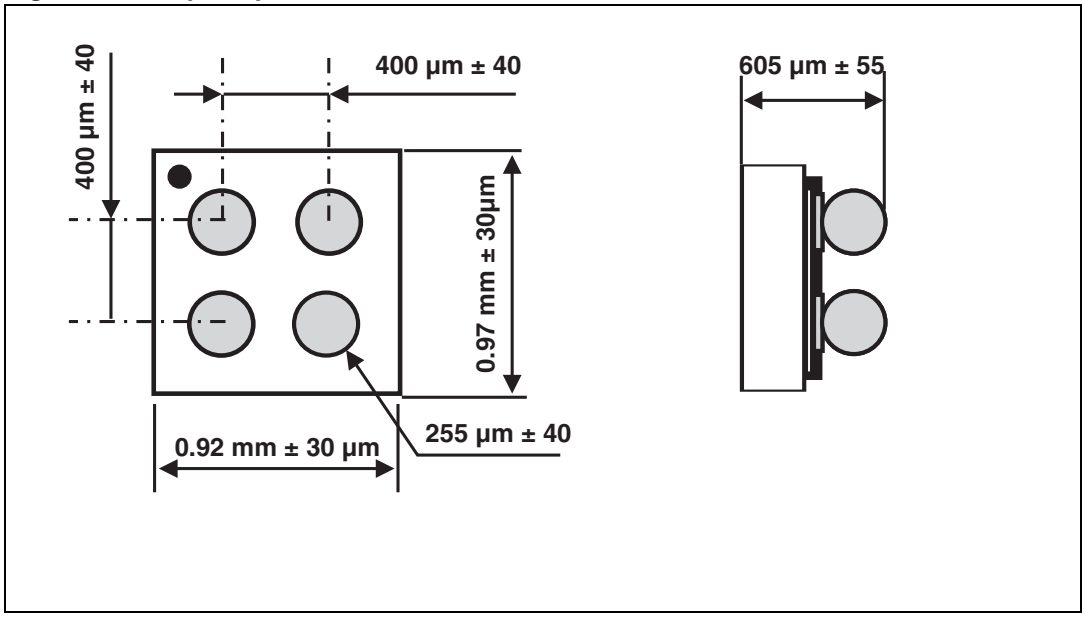


Figure 15. Foot print recommendations

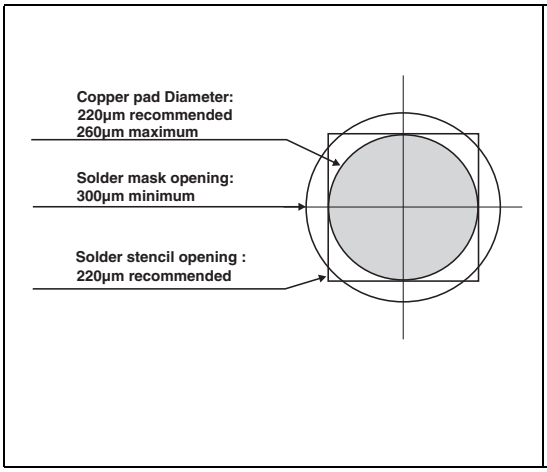


Figure 16. Marking

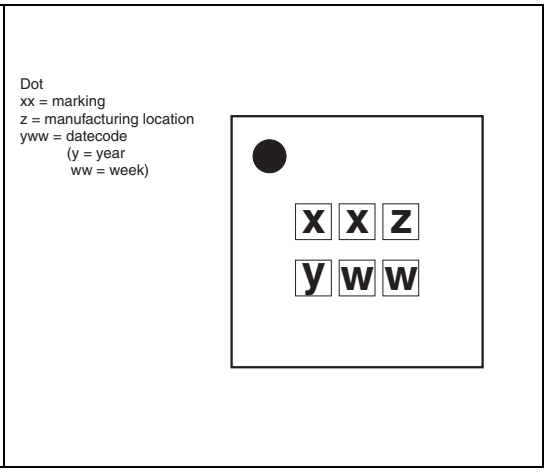
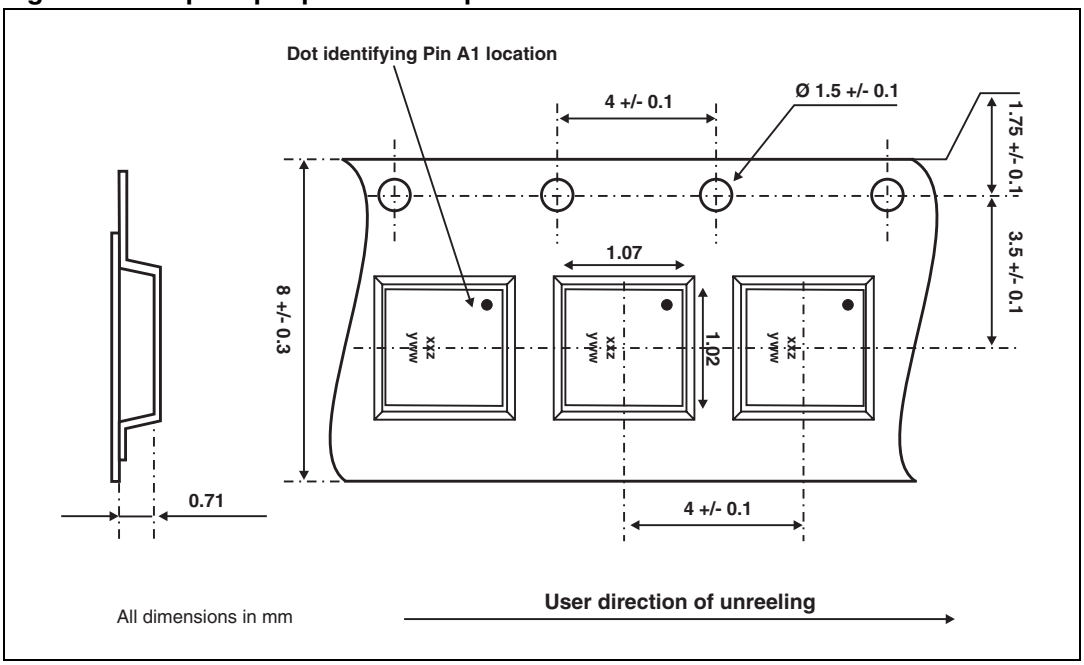


Figure 17. Flip-Chip tape and reel specifications



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note: More information is available in the application notes:
AN2348: "400 µm Flip-Chip: Package description and recommendations for use"
AN1751: "EMI Filters: Recommendations and measurements"

4 Ordering information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
USBULC6-2F3	EH	Flip-Chip	1.16 mg	5000	Tape and reel (7")

5 Revision history

Date	Revision	Changes
15-Dec-2006	1	Initial release

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