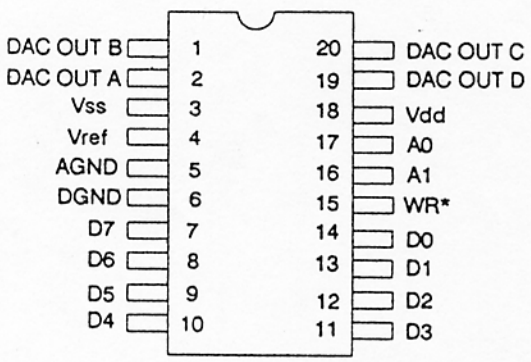
FEATURES

- Four 8 bit voltage output DACs
- Microprocessor peripheral
- TTL /CMOS compatible
- Single (5—15V) supply
- 3us settling time (typical)

DESCRIPTION

The USC1841 contains four 8 bit Digital to Analog Converters (DAC), with output amplifiers and digital interface logic and storage for each DAC. Full specified performance is achieved without trim. The chip contains 8 bit latches for each of the four DACs. Data transfer is over a common 8 bit bus into the four ports/latches. Lines A0 and A1 determine which port is loaded when WR* goes low. Each DAC has an output buffer capable of driving 5mA. Performance is guaranteed for input reference voltages from 2 to 12 V. The USC1841 has been designed to operate with a single power supply. This product is a functional replacement for Analog Devices part number AD 7226.

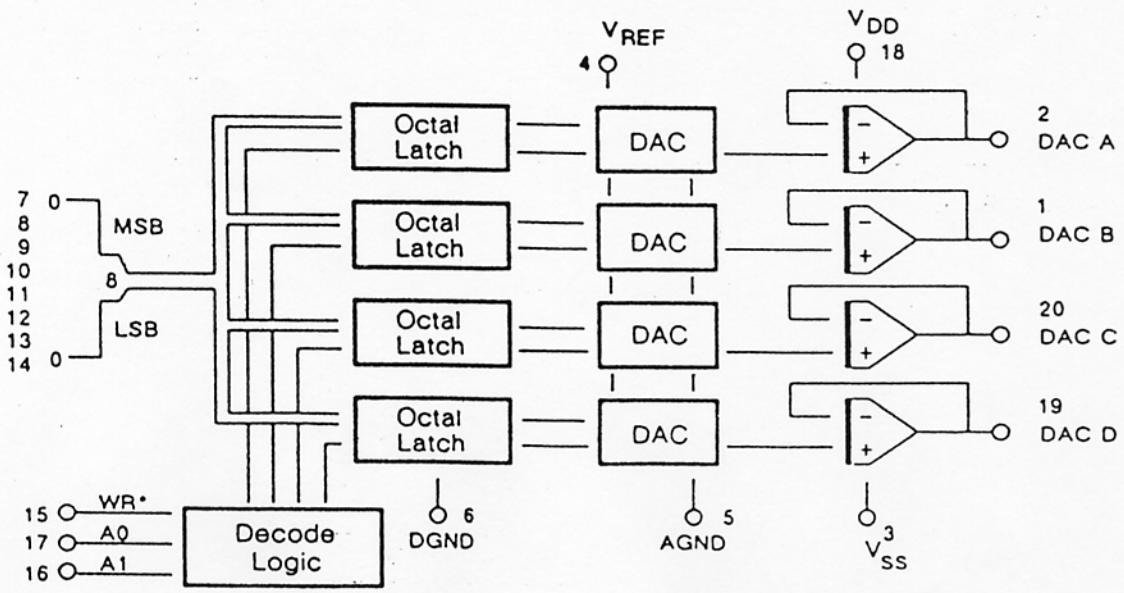
PIN CONFIGURATION



APPLICATIONS

- Automatic test equipment
- Industrial measurement
- Scientific instruments
- Industrial control
- Communications
- Broadcast equipment
- Energy control
- Automotive

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (Vss-V_{DGND})	18V
Logic Input Voltage	V_{DGND}-0.3V, V_{DD} + 0.3V
V_{REF}	Vss, V_{DD}
I_{DD} Supply	20 mA max
Temperature Range	
Storage	−65°C to + 150°C
Operating	−25°C to + 85°C (industrial)
	−55°C to + 125°C (military)

DC ELECTRICAL CHARACTERISTICS

T_A = −55°C; V_{DD} = 5 to 15V; V_{REF} = 2 to 12V; A_{GND} = D_{GND} = 0V.

PARAMETER	MIN	MAX	UNITS
Resolution	8	8	Bits
Total Unadjusted Error		+/-1	LSB
Differential Nonlinearity		+/-1/2	LSB
Reference Input :			
Resistance	4		KOhm
Capacitance		300	pf
Digital Inputs :			
V_{IL}		0.8	V
V_{IH}	2.4		V
Leakage		1.0	uA (V_{IN} = 0V or V_{DD})
Capacitance		8	pf
Coding			Binary
Output Swing	0	V_{DD}-3	V
Load Resistance	2		KOhm
Digital Crosstalk		50	nv—secs
Current Drain (I_{DD})		4	mA (unloaded outputs)

BUS INTERFACE CONTROL

Selection of the desired DAC is controlled by address lines A0 and A1 as shown by the truth table (Table 1). Data from the 8 bit wide input port will be transferred to the latches of the selected port while WR* is low. Changes on the data bus during the low period of WR* be reflected on the output. Data is latched on the rising edge of the WR*

TRUTH TABLE

A1	A0	DAC
0	0	A
0	1	B
1	0	C
1	1	D

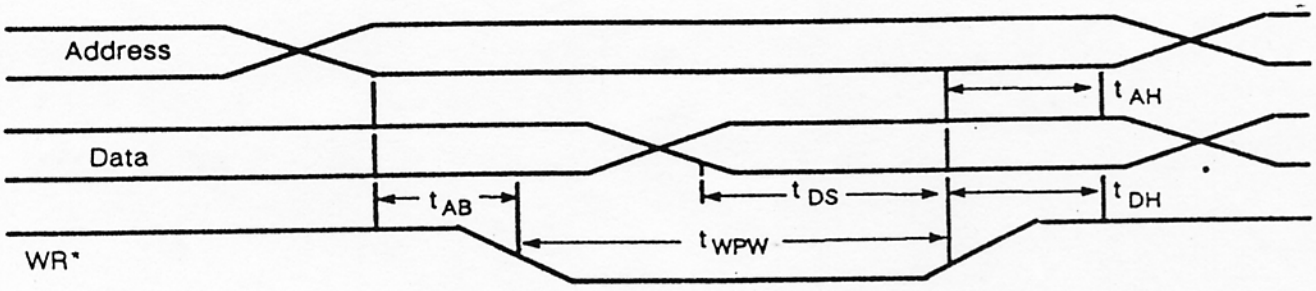
Table 1

AC ELECTRICAL CHARACTERISTICS

T_A = −55°C to + 125°C; V_{DD} = 15V; V_{REF} = 10V; A_{GND} = D_{GND} = 0V

PARAMETER	MIN	MAX	UNITS
Slew Rate	6		V/us (with 15pf load)
Setting Time		7	us to 1/2 LSB
Address — Write Set -up t_{AB}		7	ns
Data — Write Set-up t_{DS}		92	ns
Write Pulse Width twpw		125	ns
Address — Write Hold t_{AH}		7	ns

TIMING DIAGRAM



Data Bus timing
FIGURE 1

CIRCUIT INFORMATION

DIGITAL SECTION

The digital inputs to the USC1841 are compatible to both TTL and CMOS logic levels. Protection of the inputs is accomplished by internal diode clamping circuits. Timing of the input signals is shown in Figure 1. The address should be stable before the WR* signal is activated to insure that the other three DACs are not disturbed. "Flow through" operation can be accomplished on the active DAC.

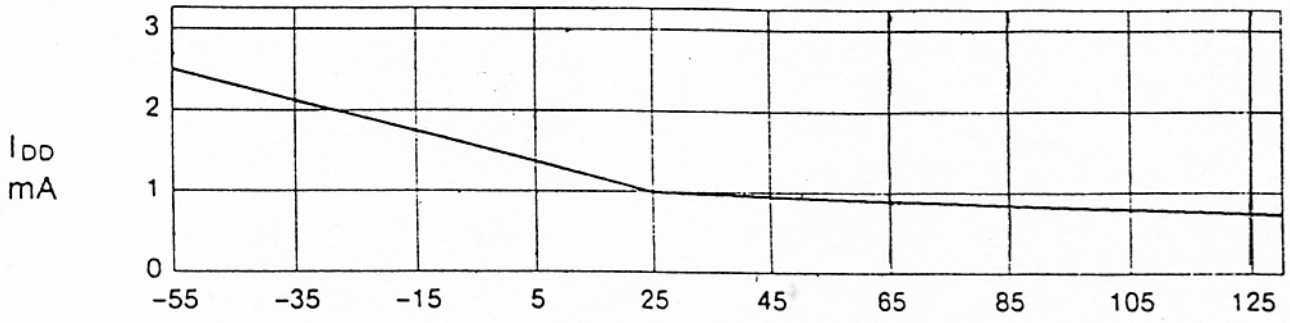
D/A CONVERSION

The four DACs each contain a 256- step resistive ladder made up of poly resistors with a nominal 100 ohm resistance per step. This provides a full monotonic range from V_{REF} to A_{GND}. The appropriate tap of the ladder is selected through a 1/256 decoder by the latched digital information. The load on the reference is not switched, hence the reference load impedance will not change with the code. The load will be the parallel combination of the four ladders.

The tapped voltage from the reference string selected by the decoder is placed into a unity gain non-inverting CMOS buffer amplifier. This produces a digitally programmed voltage source where V_{OUT} (A-D) = DL (A-D) × V_{REF}. DL (A-D) is the digital latched data for the appropriate channels. The buffer amplifier has been designed to drive atleast 5mA into a 2K load. A slew enhancement circuit has been added to assist in changing the output to its new level quickly. This means that the output will slew very rapidly toward the selected value and then settle into the final value without overshoot.

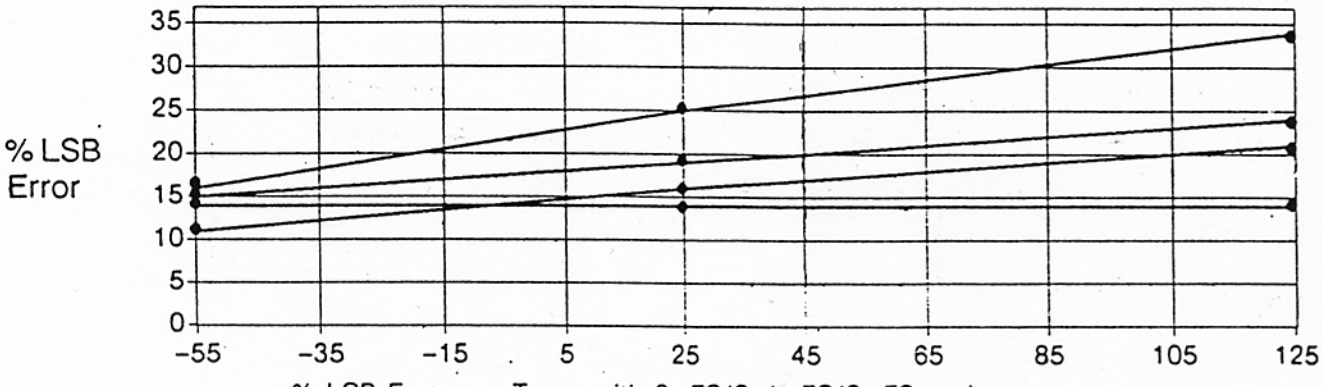
V_{DD} for the chip can be used over the 5 to 15V range. The V_{REF} must range with V_{DD} to maintain atleast a 3V margin from V_{REF} max to V_{DD} min. This produces a V_{REF} range of 2 to 12V.

DEVICE CHARACTERISTICS OVER TEMPERATURE



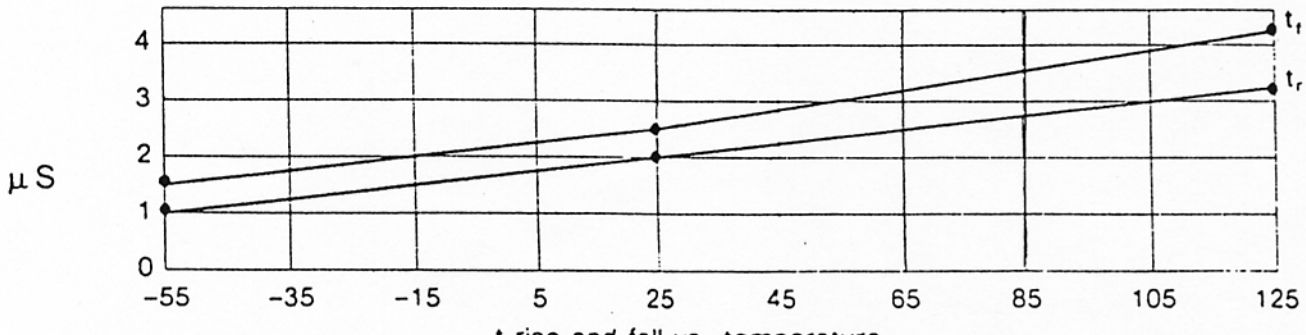
IDD Current vs. Temp
100 KHz clock V_{DD} = 15v V_{REF} = 10v

FIGURE 2



% LSB Error vs. Temp with 0, FS/2-1, FS/2, FS codes

FIGURE 3

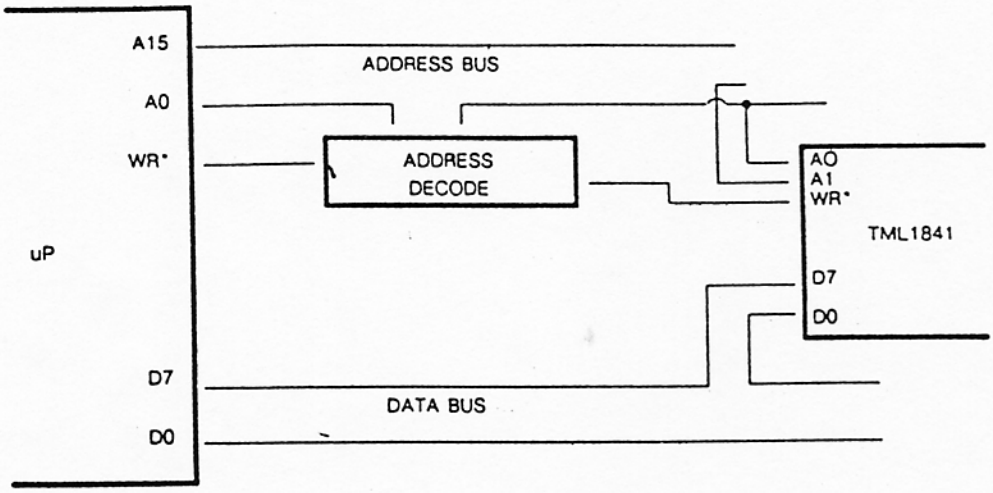


t rise and fall vs. temperature

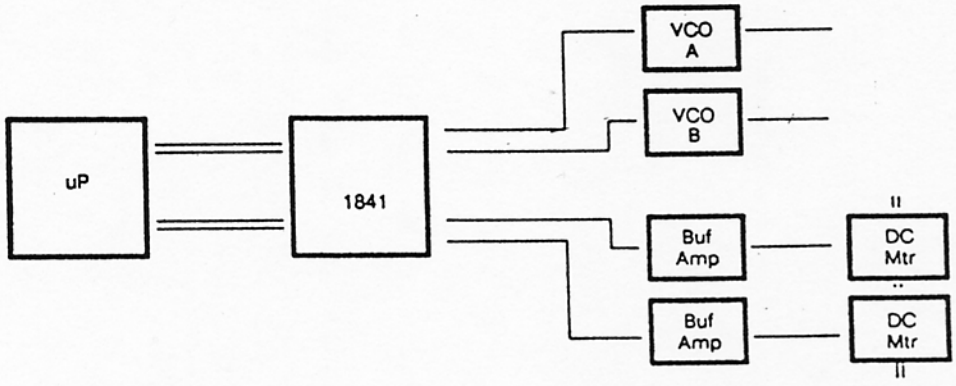
FIGURE 4

The typical operation over temperature is shown in Figures 2,3, and 4 for I_{DD} current, output error (expressed in terms of % LSB), and output rise and fall times.

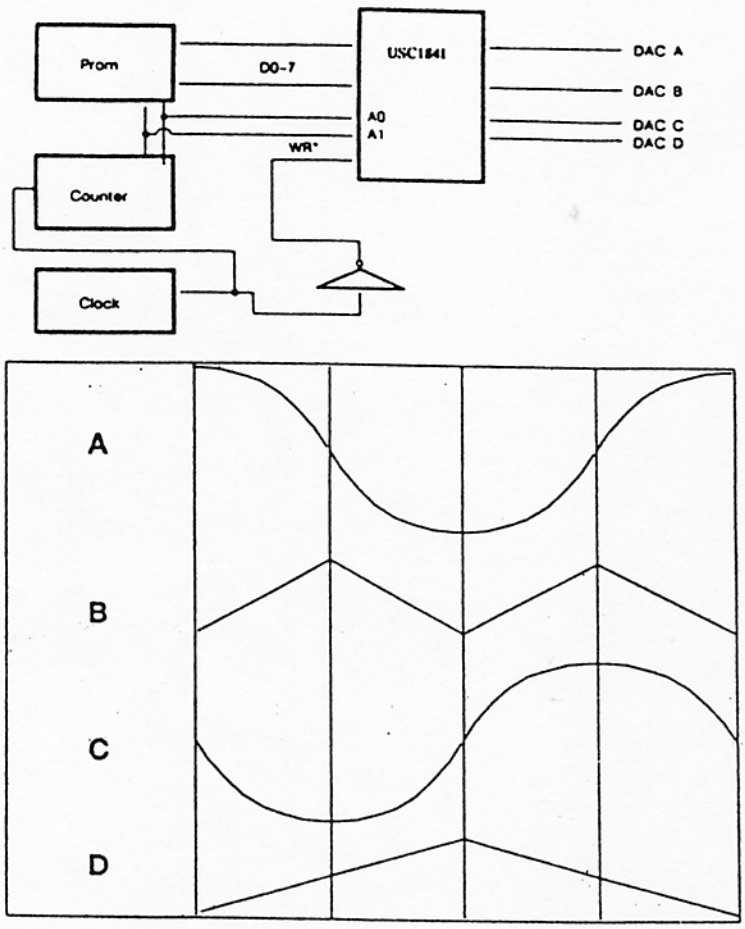
MICROPROCESSOR INTERFACE



MICROPROCESSOR TO USC1841 INTERFACE



The USC1841 can be controlled by a microprocessor and used to set the frequency on VCOs or the speed of motors. This example shows the unit controlling two independent VCOs plus a pair of DC motors with the use of buffer amplifiers. While this doesn't indicate feedback for either setup, it could easily be incorporated into the processor's input area.



Application of a four-channel function generator. Four independent output functions can be programmed into the PROM on an interlace basis. This permits the data to be sequenced at a variable rate controlled by the clock. The rapid settling time of the USC1841 allows this to be a very high speed function. Similar "electronic cams" can be generated for a variety of repetitive tasks. Various square wave signals could also be generated from the counter, but would not necessarily be full amplitude.

ORDERING INFORMATION

USC1841—BI—P20	Industrial Plastic
USC1841—BI—C20	Industrial Cerdip (—25°C to + 85°C)
USC1841—BM—C20	Military Cerdip (—55°C to + 125°C)