USG170N03 Preliminary POWER MOSFET

85A, 30V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

■ DESCRIPTION

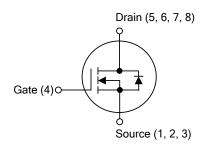
The UTC **USG170N03** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{\text{DS(ON)}}$ characteristic by high cell density trench technology.

The UTC **USG170N03** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

■ FEATURES

- * $R_{DS(ON)} \le 2.64 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_{D}=30\text{A}$ $R_{DS(ON)} \le 4.1 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_{D}=25\text{A}$
- * Optimized for high speed switching, Logic level
- * Enhanced Body diode dv/dt capability
- * Enhanced Avalanche Ruggednessy

■ SYMBOL



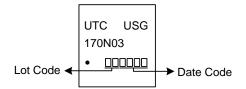
ORDERING INFORMATION

	Ordering Number		Doolsogo	Pin Assignment							Daaldaa	
	Lead Free	Halogen Free	Package	1	2	3	4	5	6	7	8	Packing
	USG170N03L-K08-5060-R	USG170N03G-K08-5060-R	DFN5060-8	S	S	S	G	D	D	D	D	Tape Reel
Ī	Note: Pin Assignment: G: Gate D: Drain S: Source											

USG170N03G-K08-5060-R
(1)Packing Type
(2)Package Type
(3)Green Package
(3) G: Halogen Free and Lead Free, L: Lead Free

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■ MARKING



■ **ABSOLUTE MAXIMUM RATING** (T_C=25°C, unless otherwise specified)

PARAM	ETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Dunin Commont	Continuous	I _D	85	Α
Drain Current	Pulsed (Note 2)	I _{DM}	170	Α
Avalanche Energy (Note 3) Single Pulsed (Note 3)		E _{AS}	32	mJ
Power Dissipation		P _D	65	W
Junction Temperature		TJ	+150	°C
Storage Temperature Range		T _{STG}	-20 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 3. L=0.1mH, I_{AS} =25.4A, V_{DD} =30V, R_G = 25 Ω , Starting T_J = 25 $^{\circ}$ C
- 4. $I_{SD} \le 20A$, $di/dt \le 200A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 25$ °C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT		
Junction to Ambient	θ_{JA}	55	°C/W		
Junction to Case	θ_{JC}	1.9	°C/W		

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

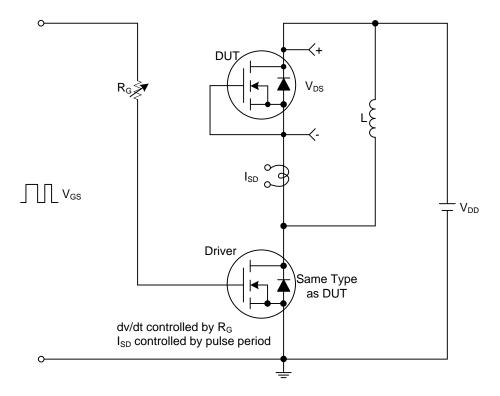
■ **ELECTRICAL CHARACTERISTICS** (T_J =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT			
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	30			V	
Drain-Source Leakage Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V			1	μΑ	
Cata Sauraa Laakaga Currant	Forward		V_{GS} =+20V, V_{DS} =0V			+100	nΑ
Gate-Source Leakage Current	Reverse	I _{GSS}	V_{GS} =-20V, V_{DS} =0V			-100	nΑ
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_{D}=1$ mA	1.2		2.2	V	
Static Drain-Source On-State Resista	R _{DS(ON)}	$V_{GS}=10V$, $I_D=30A$		2.2	2.64	mΩ	
Static Drain-Source On-State Resista		V_{GS} =4.5V, I_D =25A		3.1	4.1	mΩ	
DYNAMIC PARAMETERS							
Input Capacitance	C _{ISS}			2600		pF	
Output Capacitance	Coss	V_{GS} =0V, V_{DS} =25V, f=1.0MHz		980		pF	
Reverse Transfer Capacitance	C_{RSS}			65		pF	
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_{G}	\\ -24\\ \\ -4.5\\ -95.\		24		nC
Gate to Source Charge	Q_{GS}	V_{DS} =24V, V_{GS} =4.5V, I_{D} =85A I_{G} =1mA (Note 1, 2)		5.2		nC	
Gate to Drain Charge	Q_GD	IG=IIIIA (Note 1, 2)		8.5		nC	
Turn-on Delay Time (Note 1)		$t_{D(ON)}$			12		ns
Rise Time	t_R	V_{DS} =15V, V_{GS} =10V, I_{D} =85A,		18		ns	
Turn-off Delay Time	t _{D(OFF)}	$R_G = 3.3\Omega$ (Note 1, 2)		30		ns	
Fall-Time	t_{F}			20		ns	
SOURCE- DRAIN DIODE RATINGS	AND CH	ARACTERIST	rics				
Maximum Body-Diode Continuous C	Is				85	Α	
Maximum Body-Diode Pulsed Currer	I _{SM}				170	Α	
Drain-Source Diode Forward Voltage	(Note 1)	V_{SD}	I _S =85A, V _{GS} =0V			1.4	V

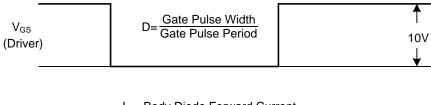
Notes: 1. Pulse Test : Pulse width ≤ 300 µs, Duty cycle ≤ 2 %.

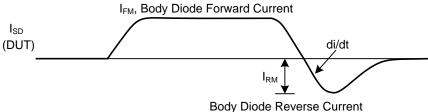
2. Essentially independent of operating temperature.

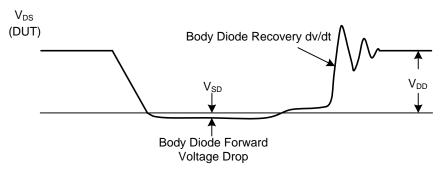
■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit



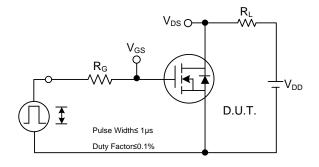


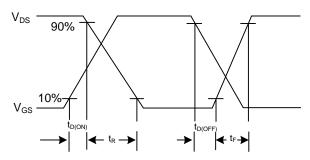


Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

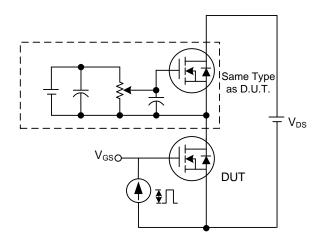
■ TEST CIRCUITS AND WAVEFORMS

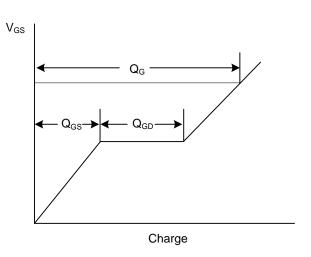




Switching Test Circuit

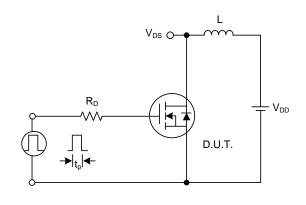
Switching Waveforms

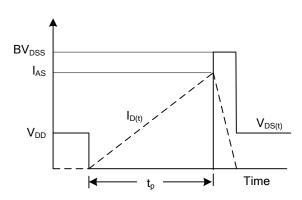




Gate Charge Test Circuit

Gate Charge Waveform





Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

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