



USGR028N85

Preliminary

POWER MOSFET

200A, 85V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

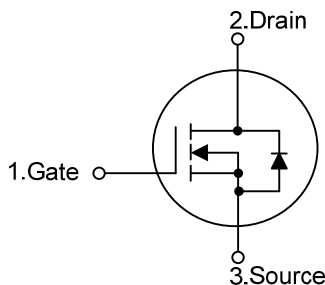
DESCRIPTION

The UTC **USGR028N85** is a uses Super Trench II technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

FEATURES

- * $R_{DS(ON)} \leq 2.8 \text{ m}\Omega @ V_{GS}=10V, I_D=50A$
- * Excellent gate charge
- * Very low on-resistance $R_{DS(ON)}$
- * High switching speed
- * Low reverse transfer capacitance

SYMBOL

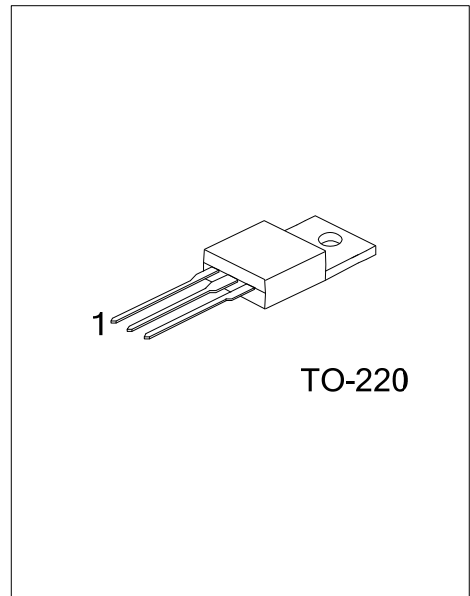


ORDERING INFORMATION

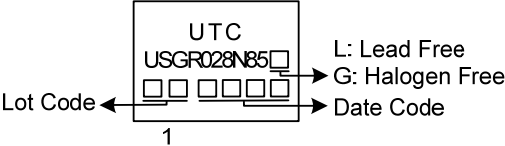
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
USGR028N85L-TA3-T	USGR028N85G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

USGR028N85G-TA3-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) TA3: TO-220
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	85	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	200	A
	Pulsed (Note 2)	I_{DM}	400	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	300	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.9	V/ns
Power Dissipation		P_D	180	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-20 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=77.5\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case		θ_{JC}	0.69 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

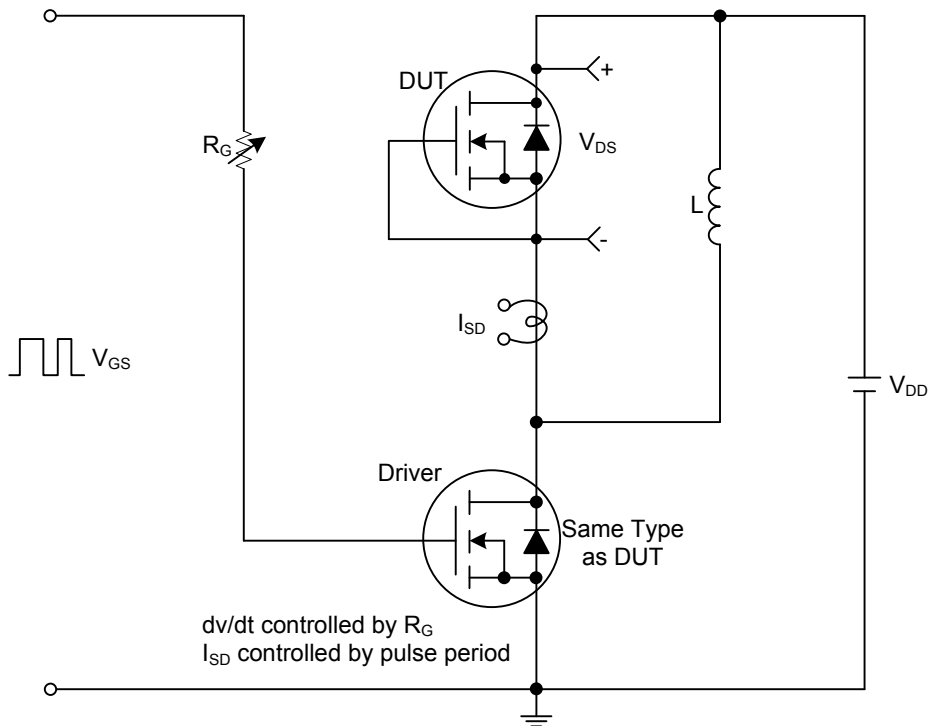
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	85			V	
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=85\text{V}$, $V_{GS}=0\text{V}$			1	μA	
Gate-Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA	
	Reverse		$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA	
ON CHARACTERISTICS								
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V	
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=50\text{A}$		2.5	2.8	m Ω	
DYNAMIC PARAMETERS								
Input Capacitance		C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		6310		pF	
Output Capacitance		C_{OSS}				3110		pF
Reverse Transfer Capacitance		C_{RSS}				300		pF
SWITCHING PARAMETERS								
Total Gate Charge (Note 1)		Q_G	$V_{DS}=68\text{V}$, $V_{GS}=10\text{V}$, $I_D=200\text{A}$, (Note 1, 2)		120		nC	
Gate to Source Charge		Q_{GS}				29		nC
Gate to Drain Charge		Q_{GD}				35		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	$V_{DD}=40\text{V}$, $V_{GS}=10\text{V}$, $I_D=200\text{A}$, $R_G=3.3\Omega$ (Note 1, 2)		20		ns	
Rise Time		t_R				25		ns
Turn-off Delay Time		$t_{D(OFF)}$				74		ns
Fall-Time		t_F				35		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS								
Maximum Body-Diode Continuous Current		I_S				200	A	
Maximum Body-Diode Pulsed Current		I_{SM}				400	A	
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	$I_S=200\text{A}$, $V_{GS}=0\text{V}$			1.4	V	
Reverse Recovery Time (Note 1)		t_{rr}	$I_S=30\text{A}$, $V_{GS}=0\text{V}$,			64	nS	
Reverse Recovery Charge		Q_{rr}	$di/dt = 100\text{A}/\mu\text{s}$			120	nC	

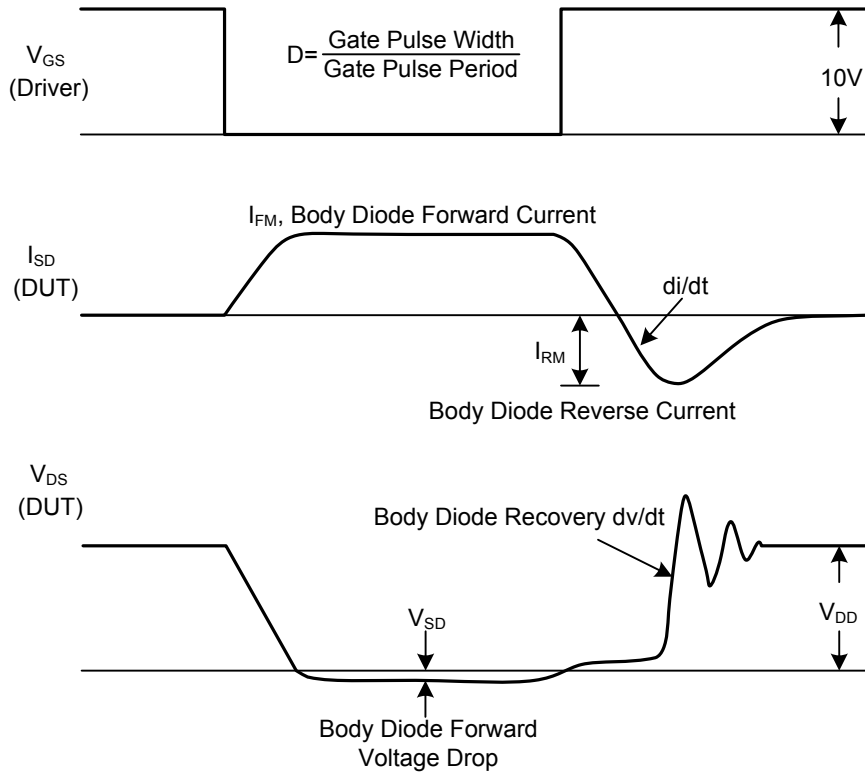
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



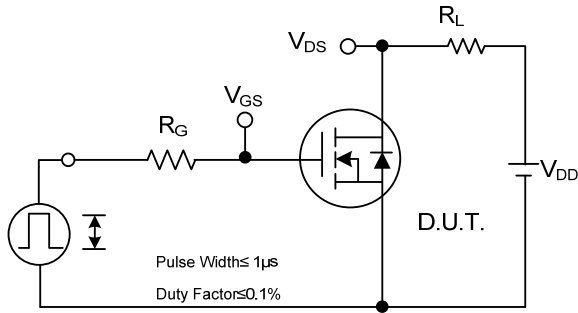
Peak Diode Recovery dv/dt Test Circuit



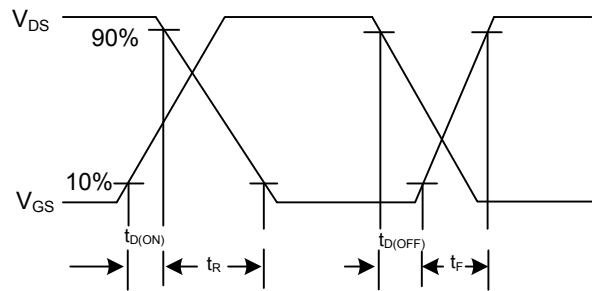
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

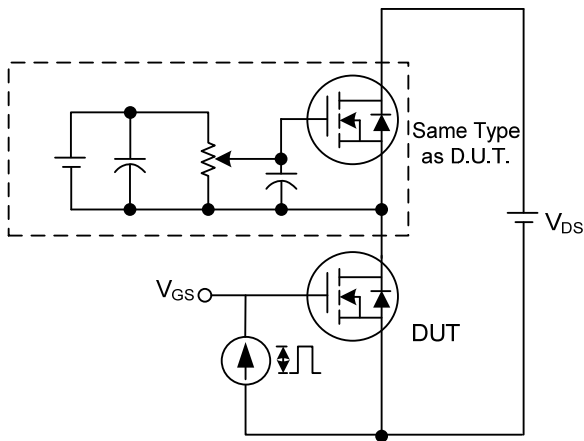
■ TEST CIRCUITS AND WAVEFORMS



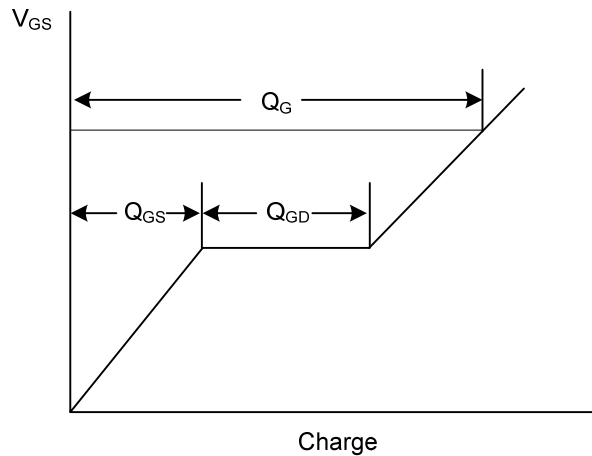
Switching Test Circuit



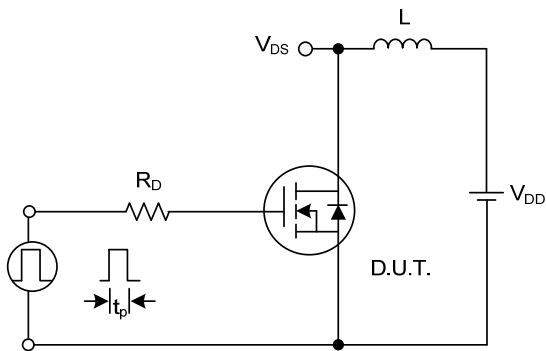
Switching Waveforms



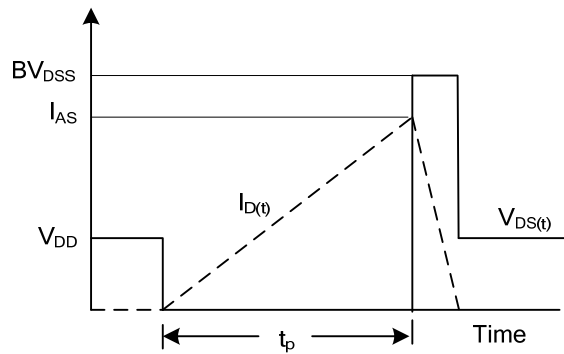
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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