



UT2N20

POWER MOSFET

2.0A, 200V N-CHANNEL POWER MOSFET

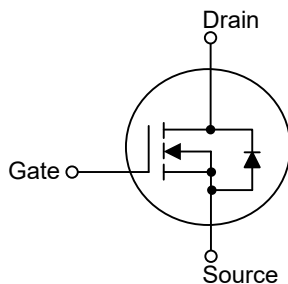
DESCRIPTION

The UTC **UT2N20** is a high voltage power MOSFET combines advanced trench MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics. This power MOSFET is usually used in high speed switching applications of switching power supplies and adaptors.

FEATURES

- * $R_{DS(ON)} \leq 625 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=1.0\text{A}$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness

SYMBOL

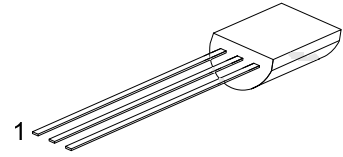


ORDERING INFORMATION

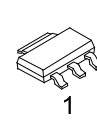
Ordering Number		Package	Pin Assignment						Packing
Lead Free	Halogen Free		1	2	3	4	5	6	
UT2N20L-AA3-R	UT2N20G-AA3-R	SOT-223	G	D	S	-	-	-	Tape Reel
UT2N20L-AG6-R	UT2N20G-AG6-R	SOT-26	D	D	G	S	D	D	Tape Reel
UT2N20L-T92-B	UT2N20G-T92-B	TO-92	G	D	S	-	-	-	Tape Box
UT2N20L-T92-K	UT2N20G-T92-K	TO-92	G	D	S	-	-	-	Bulk
UT2N20L-T92-C-B	UT2N20G-T92-C-B	TO-92	S	G	D	-	-	-	Tape Box
UT2N20L-T92-C-K	UT2N20G-T92-C-K	TO-92	S	G	D	-	-	-	Bulk

Note: Pin Assignment: D: Drain G: Gate S: Source

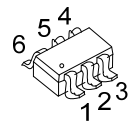
UT2N20G-T92-C-B	(1)Packing Type (2)Pin Assignment (3)Package Type (4)Green Package	(1) B: Tape Box, K: Bulk, R: Tape Reel (2) refer to Pin Assignment (for TO-92) (3) AA3: SOT-223, AG6: SOT-26, T92: TO-92 (4) G: Halogen Free and Lead Free, L: Lead Free
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TO-92

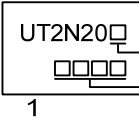
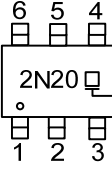
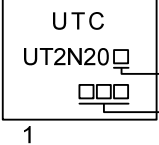


SOT-223



SOT-26

■ MARKING

PACKAGE	MARKING
SOT-223	 L: Lead Free G: Halogen Free Date Code
SOT-26	 L: Lead Free G: Halogen Free
TO-92	 L: Lead Free G: Halogen Free Date Code

■ **ABSOLUTE MAXIMUM RATING** ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	2	A
	Pulsed	I_{DM}	4	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	3.7	V/ns
Power Dissipation	SOT-223	P_D	2.2	W
	SOT-26		1.5	W
	TO-92		2	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
 3. $I_{SD} \leq 2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-223	θ_{JA}	140	$^{\circ}\text{C}/\text{W}$
	SOT-26		240	$^{\circ}\text{C}/\text{W}$
	TO-92		160	$^{\circ}\text{C}/\text{W}$
Junction to Case	SOT-223	θ_{JC}	56.8	$^{\circ}\text{C}/\text{W}$
	SOT-26		83	$^{\circ}\text{C}/\text{W}$
	TO-92		62.5	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

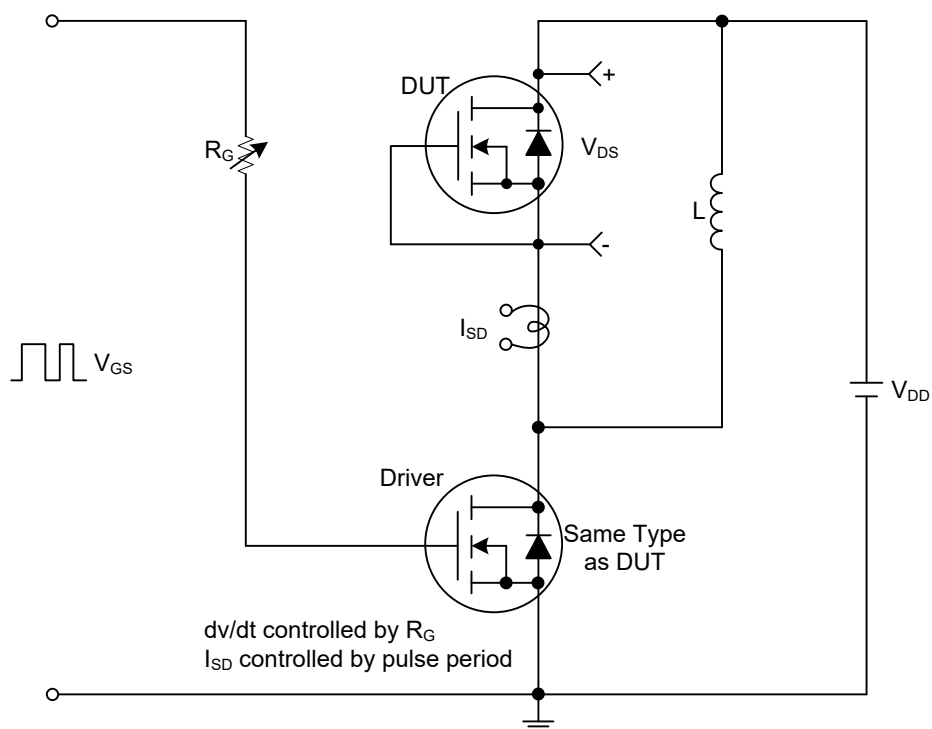
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	200			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =200V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		3.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.0A			625	mΩ
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1MHz		404.8		pF
Output Capacitance		C _{OSS}			32.1		pF
Reverse Transfer Capacitance		C _{RSS}			17.2		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =160V, V _{GS} =10V, I _D =2.0A I _G =1mA (Note 1, 2)		16.1		nC
Gate to Source Charge		Q _{GS}			4.3		nC
Gate to Drain Charge		Q _{GD}			3.5		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =2.0A, R _G =25Ω (Note 1, 2)		17.6		ns
Rise Time		t _R			15.2		ns
Turn-off Delay Time		t _{D(OFF)}			41.6		ns
Fall-Time		t _F			22		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				2	A
Maximum Body-Diode Pulsed Current		I _{SM}				4	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =2.0A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _S =2.0A, V _{GS} =0V,		72		ns
Reverse Recovery Charge		Q _{rr}	dI _F /dI=100A/μs		0.1		μC

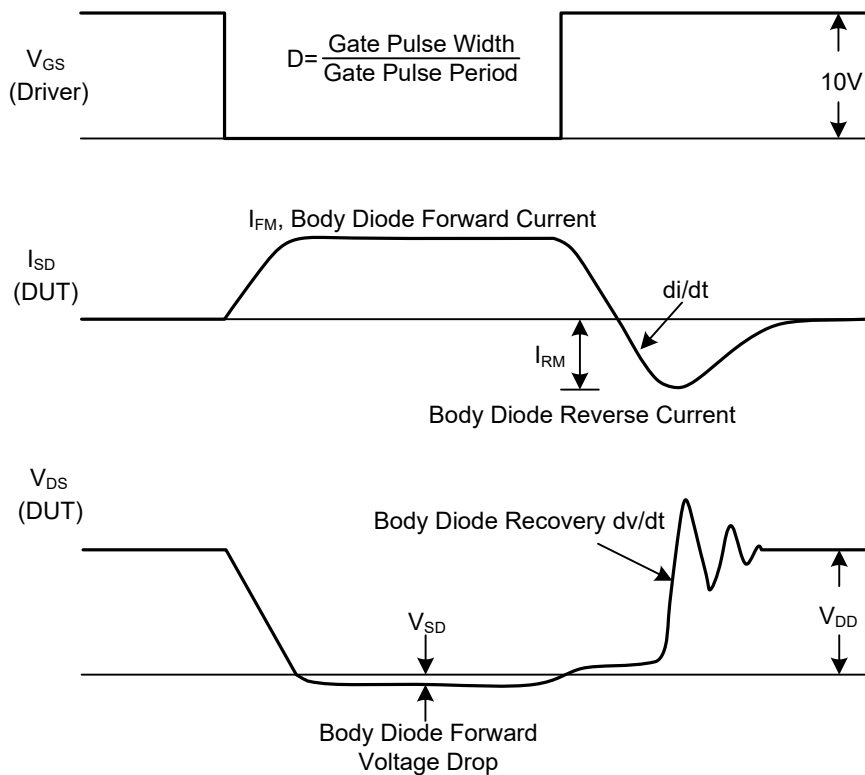
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



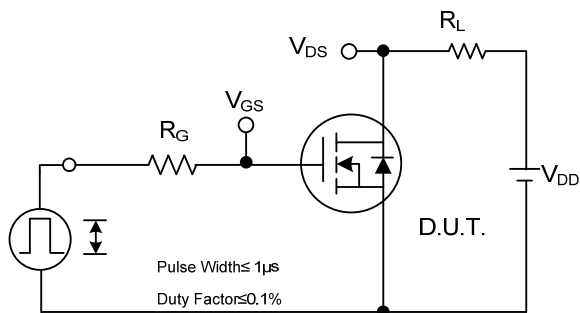
Peak Diode Recovery dv/dt Test Circuit



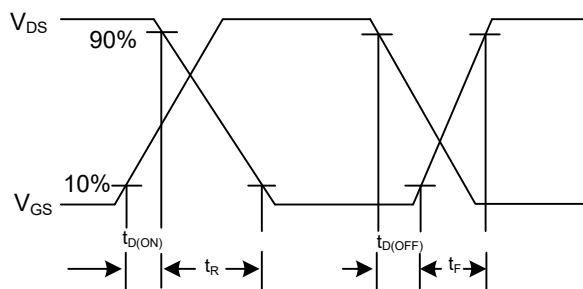
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

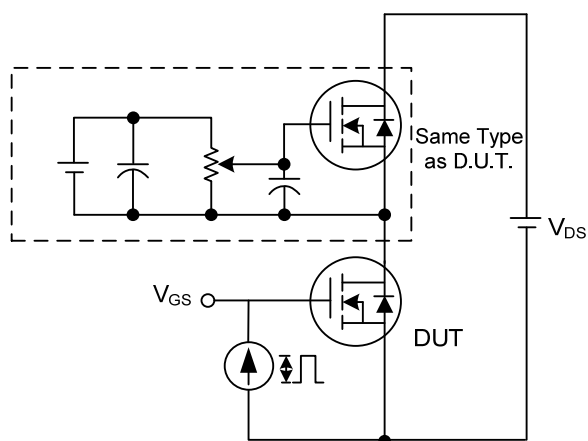
■ TEST CIRCUITS AND WAVEFORMS



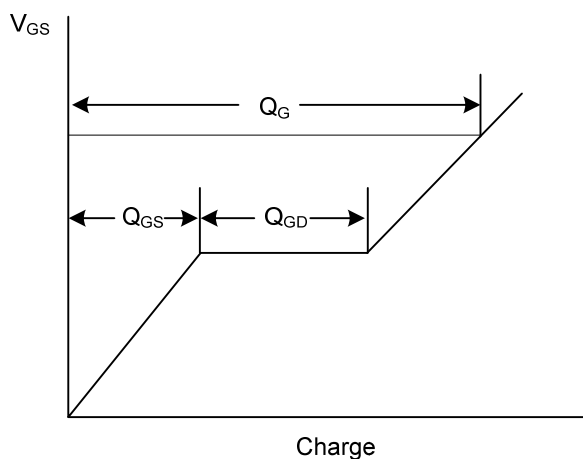
Switching Test Circuit



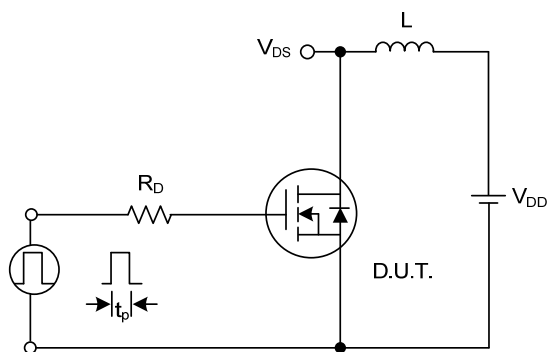
Switching Waveforms



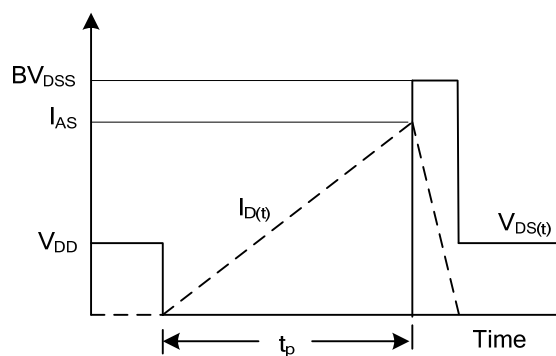
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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