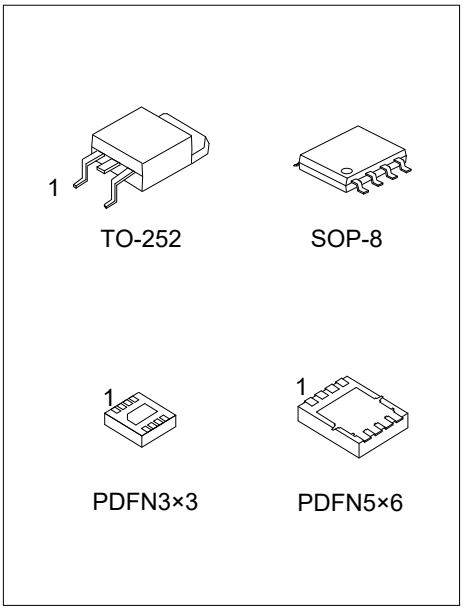
UT40N04

Power MOSFET

N-CHANNEL LOGIC LEVEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR



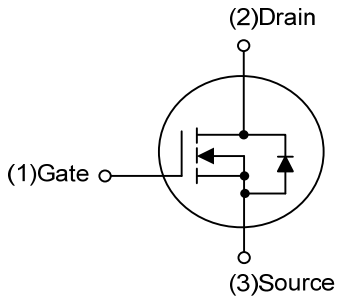
■ DESCRIPTION

The UTC **UT40N04** is an N-channel enhancement mode FET using advanced technology to provide fast switching speed, ruggedized device design, low on-resistance and cost-effectiveness.

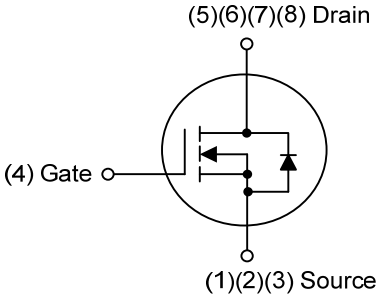
■ FEATURES

* Low on-Resistance
* Fast Switching Speed

■ SYMBOL



TO-252



SOP-8/PDFN3×3/PDFN5×6

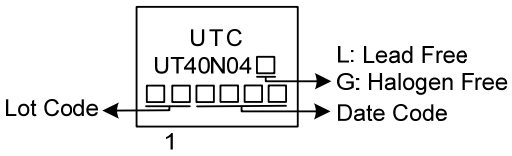
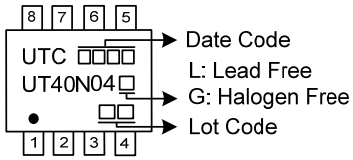
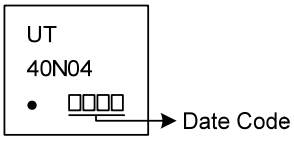
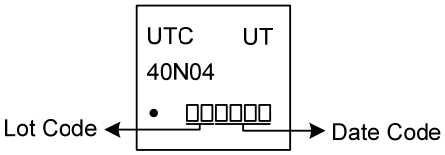
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT40N04L-TN3-R	UT40N04G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT40N04L-S08-R	UT40N04G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT40N04L-P3030-R	UT40N04G-P3030-R	PDFN3×3	S	S	S	G	D	D	D	D	Tape Reel
UT40N04L-P5060-R	UT40N04G-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT40N04G-TN3-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) TN3: TO-252, S08: SOP-8, P3030: PDFN3×3 P5060: PDFN5×6 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

TO-252	SOP-8
	
PDFN3×3	**PDFN5×6**
	

■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, Unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	TO-252 PDFN5×6 PDFN3×3	I_D	40	A
	SOP-8		12	A
Pulsed Drain Current (Note 1)		I_{DM}	80	A
Avalanche Energy		E_{AS}	16.9	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.8	V/ns
Power Dissipation	TO-252	P_D	40	W
	SOP-8		3.5	W
	PDFN3×3		30	W
	PDFN5×6		35	W
Operating Junction Temperature		T_J	-55 ~ +150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L=0.1mH, I_{AS}=18.4A, V_{DD}=20V, R_G=25 Ω, Starting T_J = 25°C
4. I_{SD} ≤ 30A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA (NOTE 2)

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	50	°C/W
	SOP-8		125	°C/W
	PDFN3×3		75	°C/W
	PDFN5×6		65	°C/W
Junction to Case	TO-252	θ_{JC}	3.125	°C/W
	SOP-8		35.7	°C/W
	PDFN3×3		4.17	°C/W
	PDFN5×6		3.57	°C/W

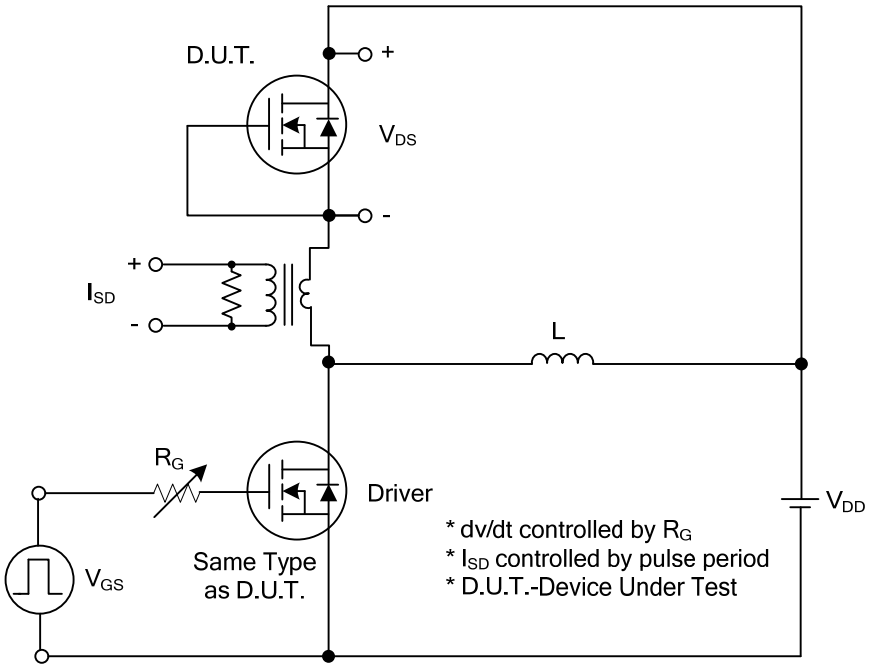
Notes: 1. Independent of Operating Temperature.
2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

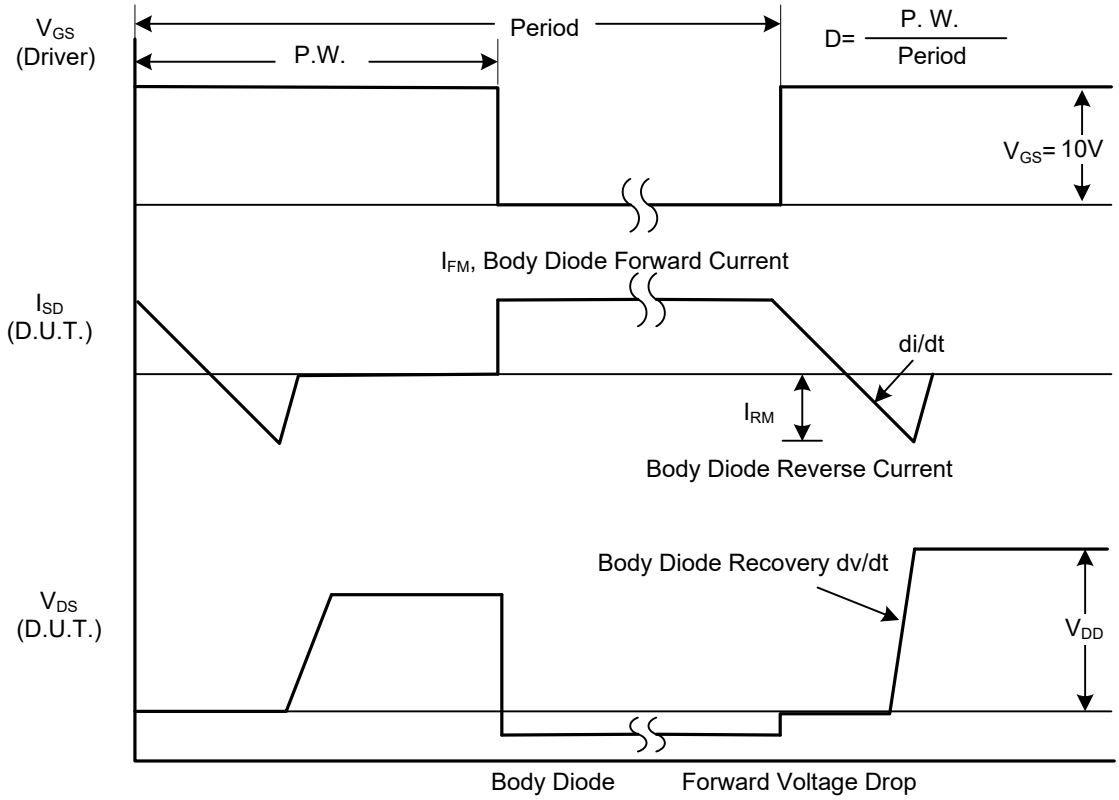
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	40			V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V			10	μA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.0		3.0	V
Static Drain-Source On-State Resistance (Note 1)	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A			12	mΩ
		V_{GS}=4.5V, I_D=10A			16	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		1230		pF
Output Capacitance	C_{OSS}			144		pF
Reverse Transfer Capacitance	C_{RSS}			122		pF
SWITCHING PARAMETERS (Note 2)						
Total Gate Charge	Q_G	V_{DS}=20V, V_{GS}=10V, I_D=40A, I_G=1mA (Note1,2)		34.5		nC
Gate to Source Charge	Q_{GS}			5.3		nC
Gate to Drain Charge	Q_{GD}			8.4		nC
Turn-ON Delay Time	$t_{D(ON)}$	V_{DS}=20V, V_{GS}=10V, I_D=40A, R_G=3Ω (Note1,2)		7		ns
Rise Time	t_R			17		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			30		ns
Fall-Time	t_F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				40	A
Maximum Pulsed Drain-Source Diode Forward Current(Note 1)	I_{SM}				80	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	I_F=40A, V_{GS}=0V			1.3	V

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle≤2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

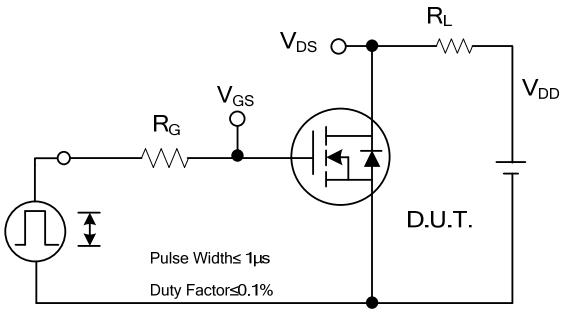


Peak Diode Recovery dv/dt Test Circuit

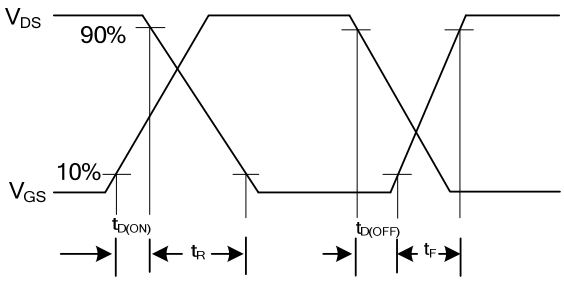


Peak Diode Recovery dv/dt Waveforms

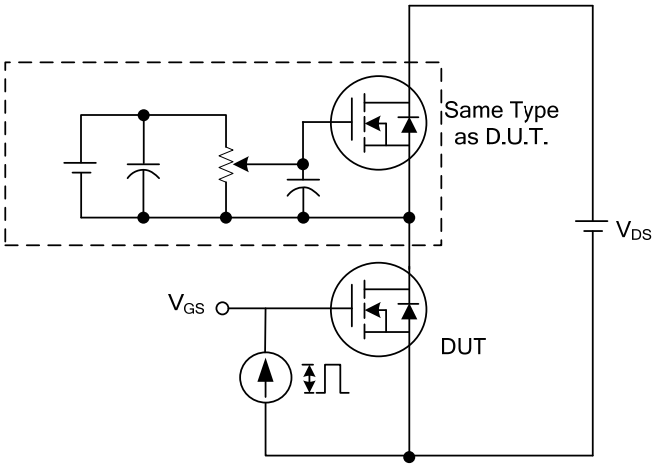
■ TEST CIRCUITS AND WAVEFORMS



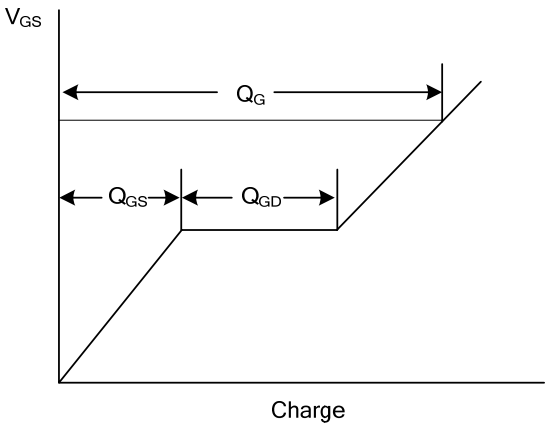
Switching Test Circuit



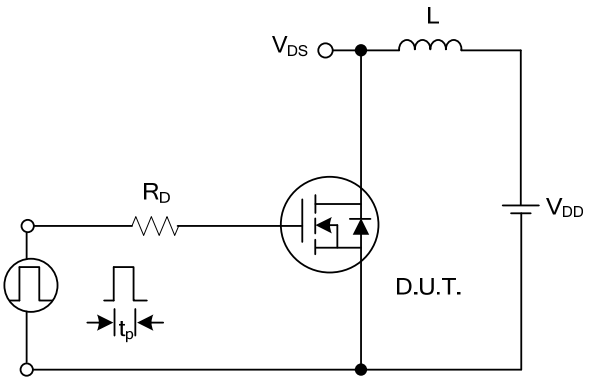
Switching Waveforms



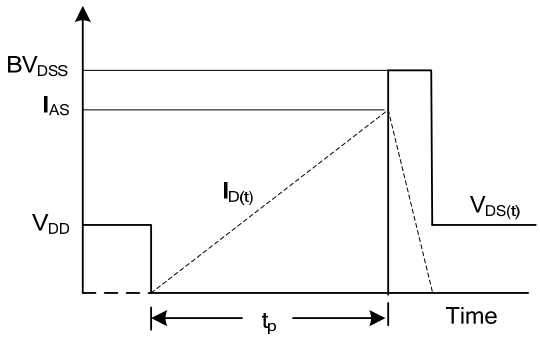
Gate Charge Test Circuit



Gate Charge Waveform

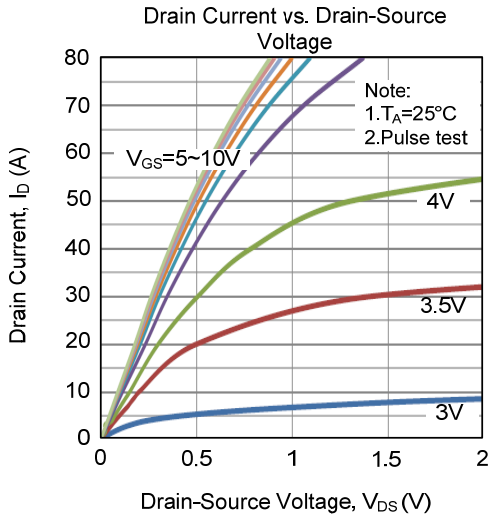


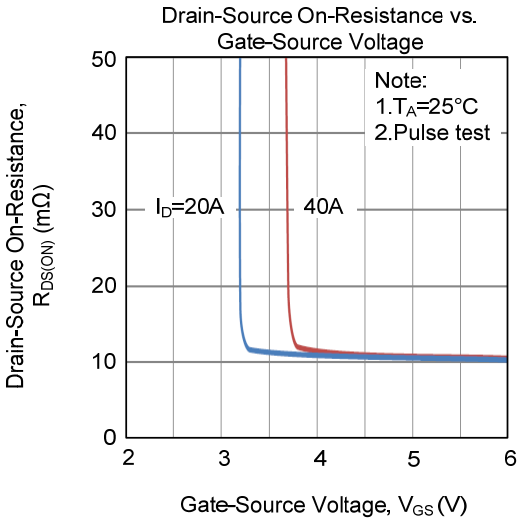
Unclamped Inductive Switching Test Circuit

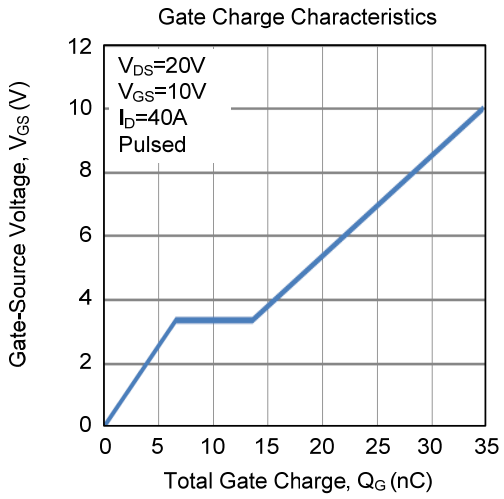


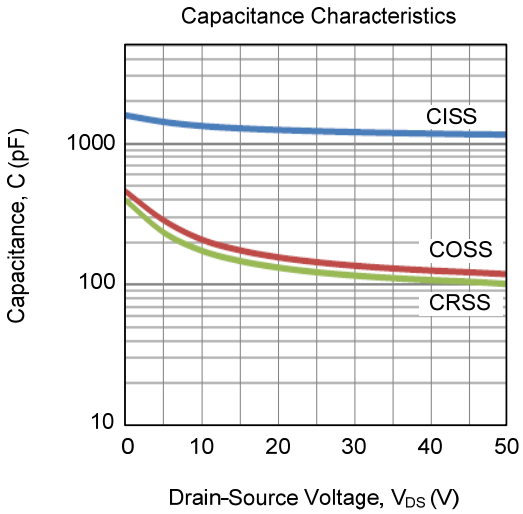
Unclamped Inductive Switching Waveforms

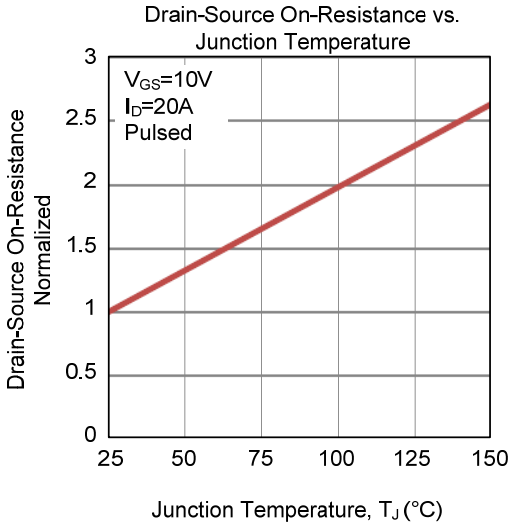
■ TYPICAL CHARACTERISTICS

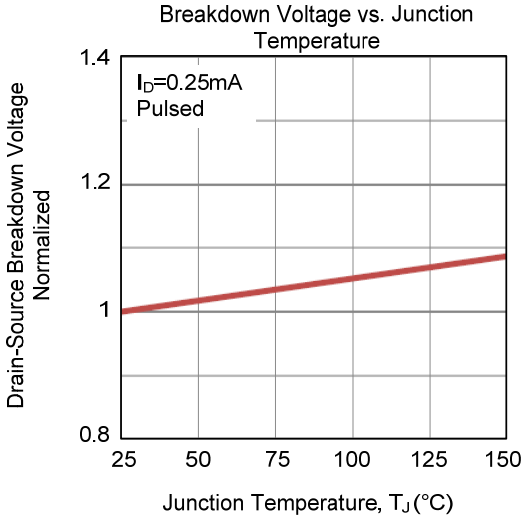






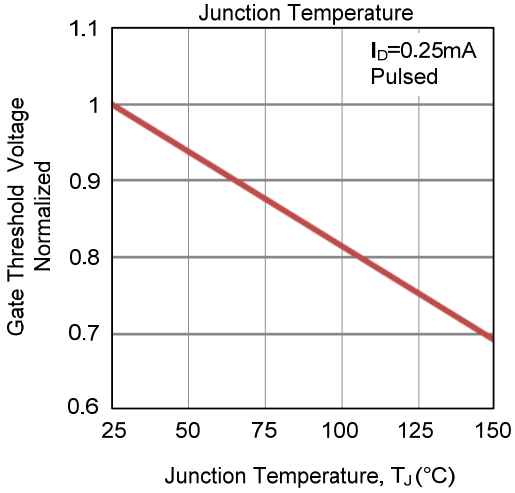




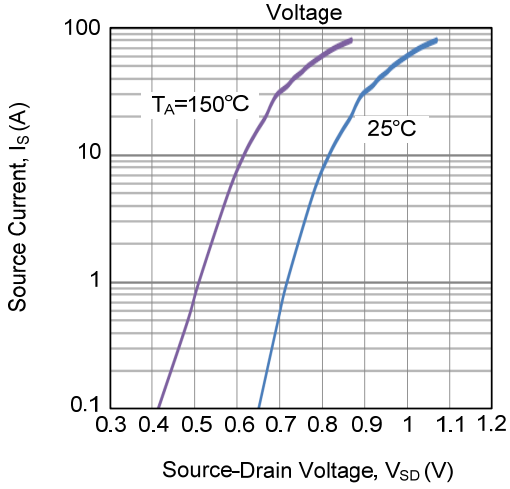


■ TYPICAL CHARACTERISTICS (Cont.)

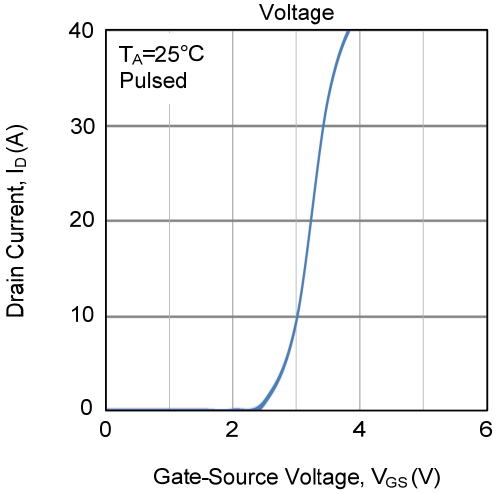
Gate Threshold Voltage vs. Junction Temperature



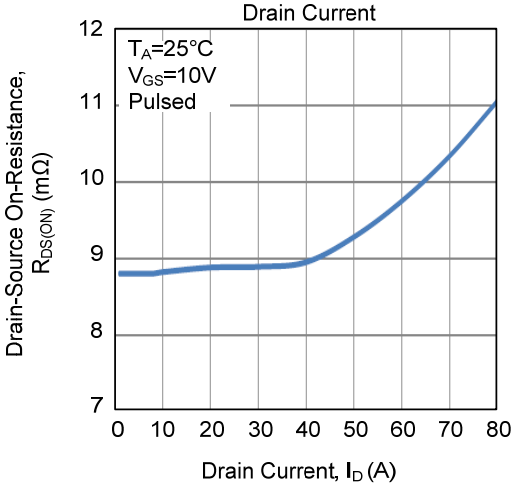
Source Current vs. Source-Drain Voltage



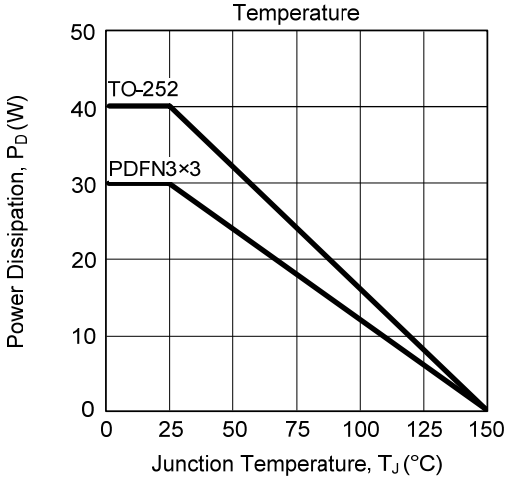
Drain Current vs. Gate-Source Voltage



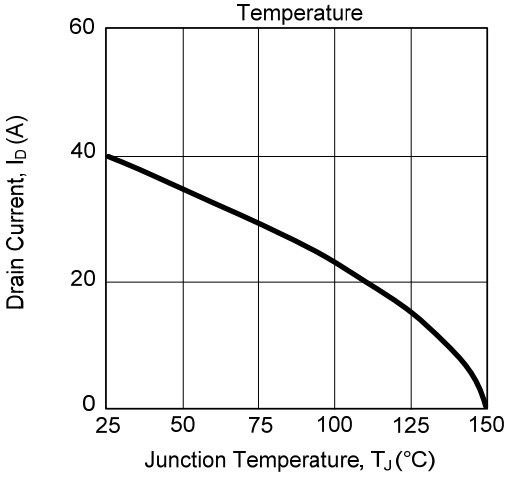
Drain-Source On-Resistance vs. Drain Current



Power Dissipation vs. Junction Temperature



Drain Current vs. Junction Temperature



■ TYPICAL CHARACTERISTICS (Cont.)