



## UT4422

Power MOSFET

### N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

#### DESCRIPTION

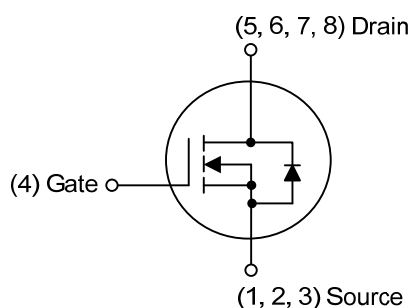
The UTC **UT4422** is a N-channel MOSFET, it uses UTC's advanced technology to provide the customers with a minimum on state resistance and high switching speed.

The UTC **UT4422** is suitable for load switch and battery protection applications.

#### FEATURES

- \*  $R_{DS(ON)} \leq 15 \text{ m}\Omega$  @  $V_{GS} = 10\text{V}$ ,  $I_D = 8.0\text{A}$
- \*  $R_{DS(ON)} \leq 24 \text{ m}\Omega$  @  $V_{GS} = 4.5\text{V}$ ,  $I_D = 8.0\text{A}$
- \* Low Capacitance
- \* Low Gate Charge
- \* Fast Switching Capability
- \* Avalanche Energy Specified

#### SYMBOL

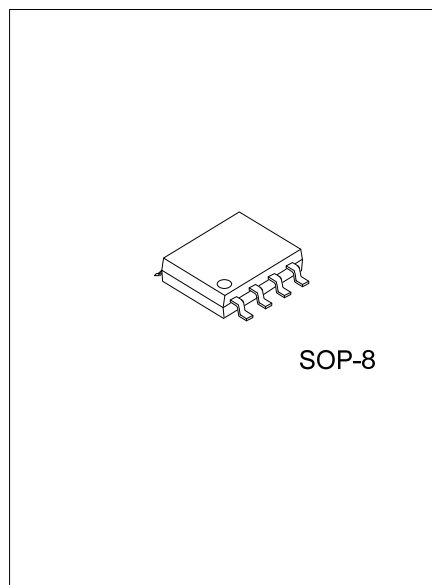


#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT4422L-S08-R	UT4422G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

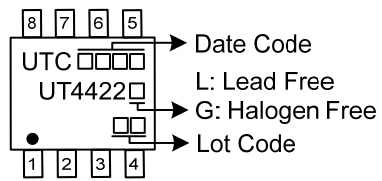
Note: Pin Assignment: G: Gate D: Drain S: Source

UT4422G-S08-R	(1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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SOP-8

## ■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	$I_D$	11	A
Pulsed Drain Current	$I_{DM}$	50	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	7
Power Dissipation	$P_D$	1.5	W
Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L = 0.1\text{mH}$ ,  $I_{AS} = 11.6\text{A}$ ,  $V_{DD} = 20\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	90	$^\circ\text{C/W}$
Junction to Case	$\theta_{JC}$	83.3 (Note)	$^\circ\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

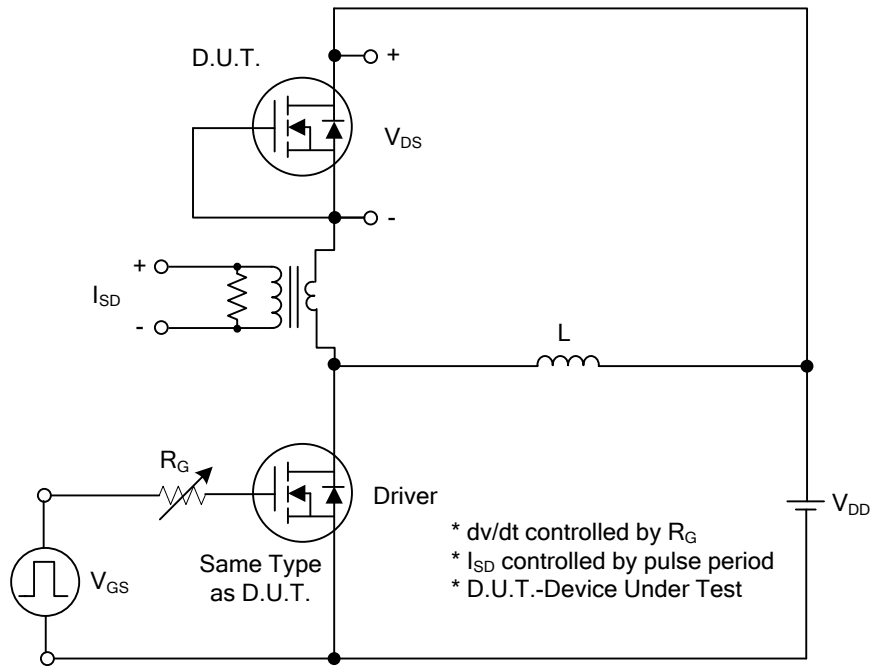
■ ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		3.0	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =8.0A			15	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8.0A			24	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		850		pF
Output Capacitance	C <sub>OSS</sub>			201		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			168		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =10V, I <sub>D</sub> =11A		29		nC
Gate Source Charge	Q <sub>GS</sub>			4		nC
Gate Drain Charge	Q <sub>GD</sub>			8		nC
Turn-ON Delay Time	t <sub>D(ON)</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =11A, R <sub>G</sub> =3.0Ω (Note 1, 2)		6		ns
Turn-ON Rise Time	t <sub>R</sub>			18		ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>			22		ns
Turn-OFF Fall-Time	t <sub>F</sub>			21		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =11A, V <sub>GS</sub> =0V			1.4	V

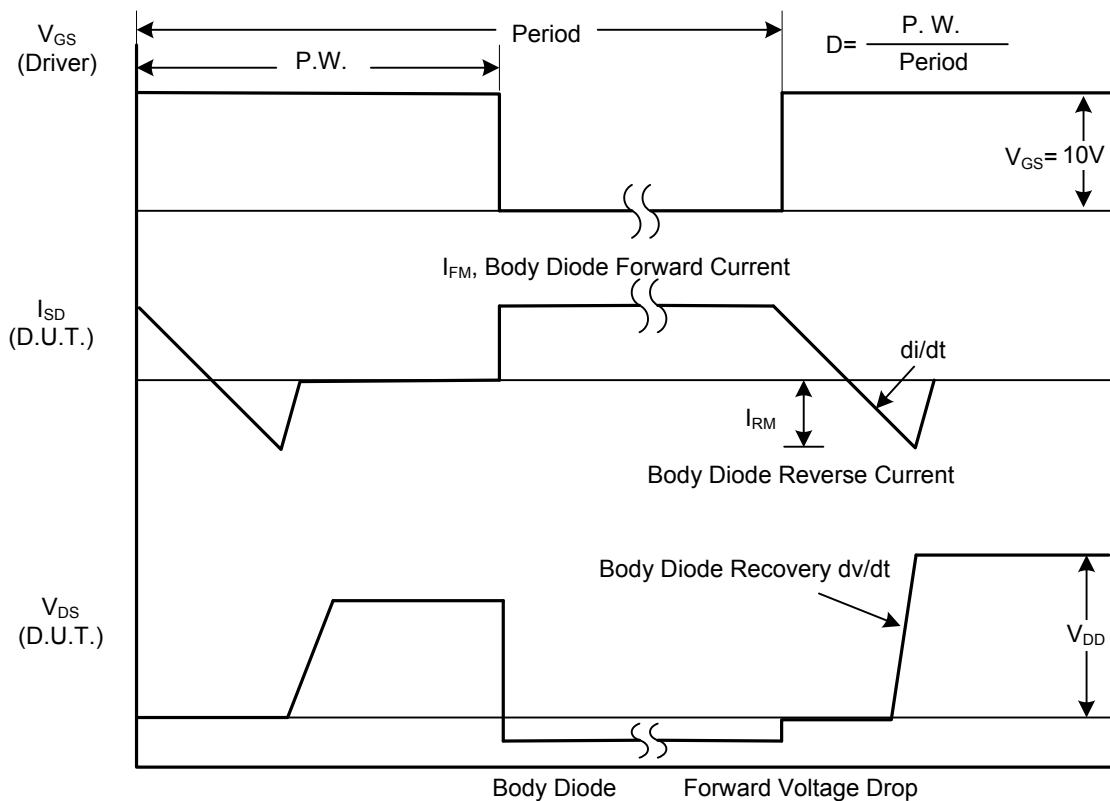
Notes: 1. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

## ■ TEST CIRCUITS AND WAVEFORMS

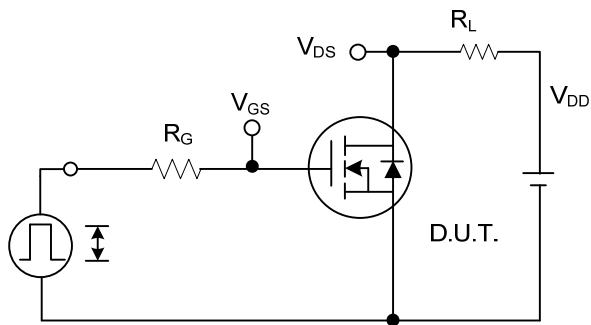


**Peak Diode Recovery dv/dt Test Circuit**

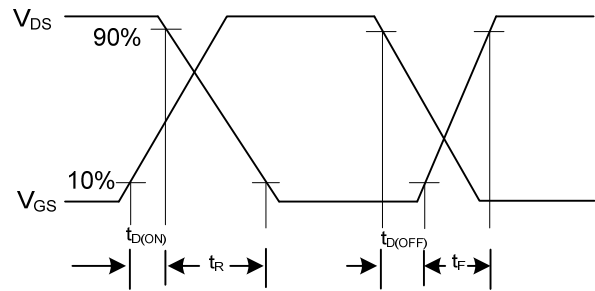


**Peak Diode Recovery dv/dt Waveforms**

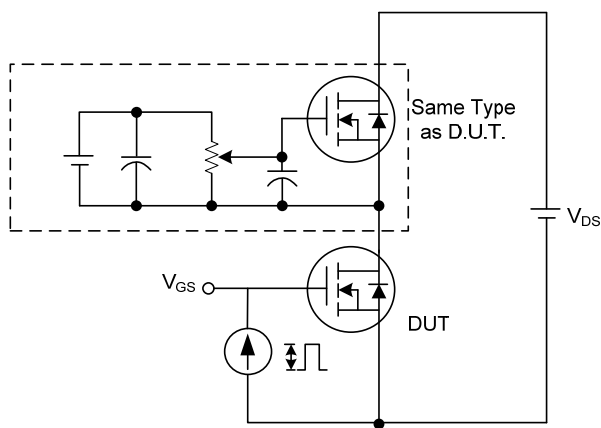
## ■ TEST CIRCUITS AND WAVEFORMS



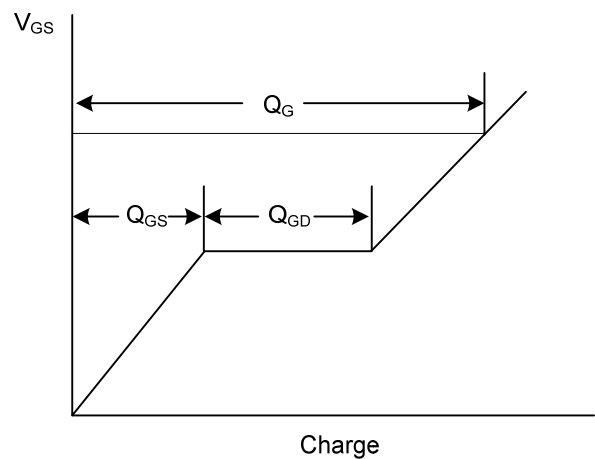
Switching Test Circuit



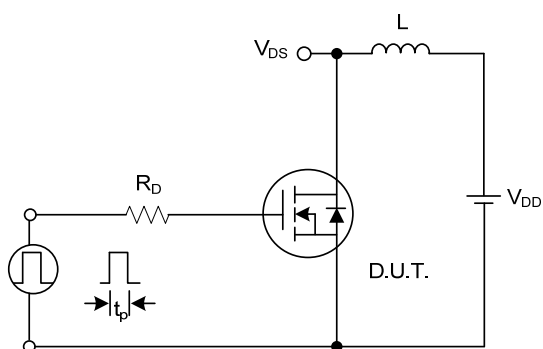
Switching Waveforms



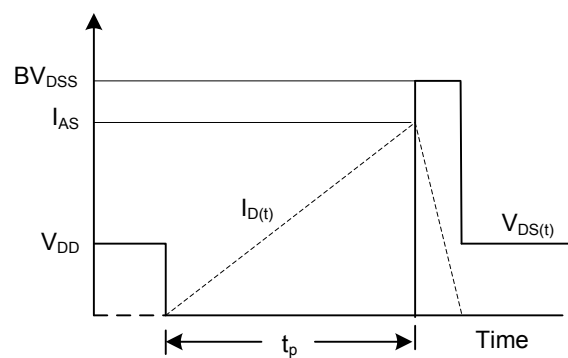
Gate Charge Test Circuit



Gate Charge Waveform

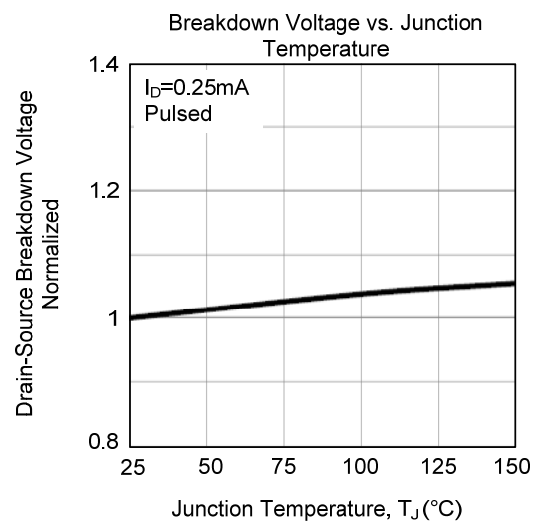
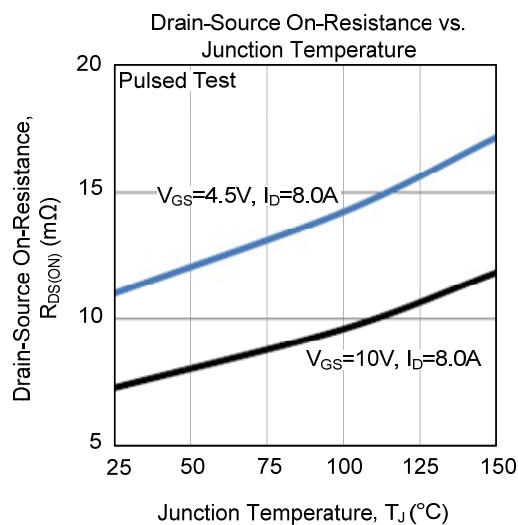
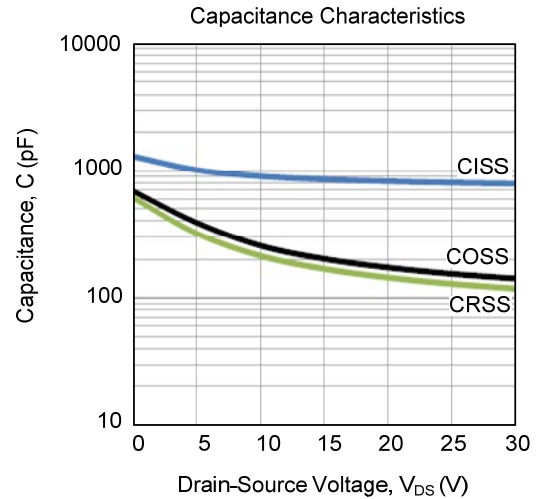
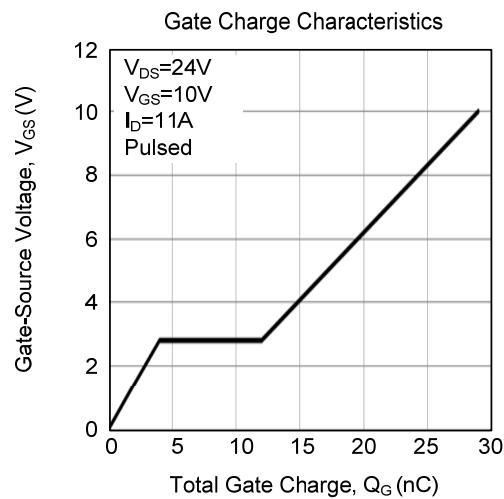
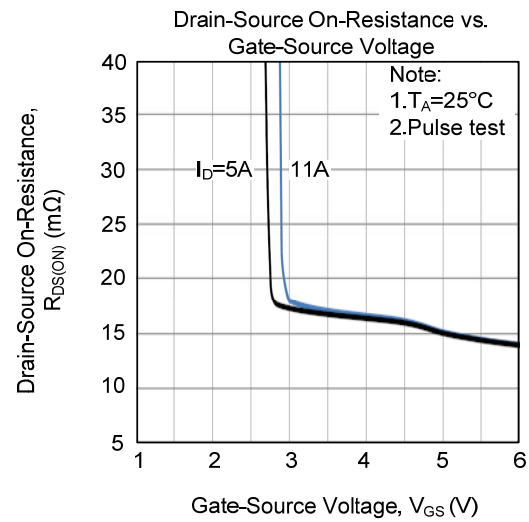
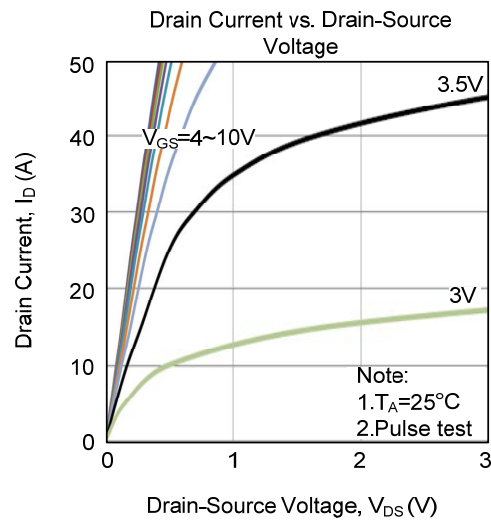


Unclamped Inductive Switching Test Circuit

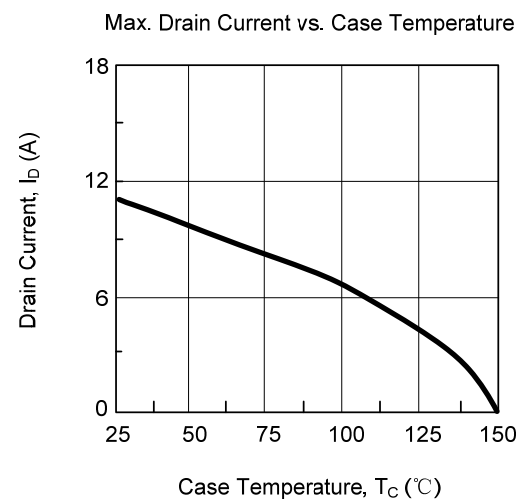
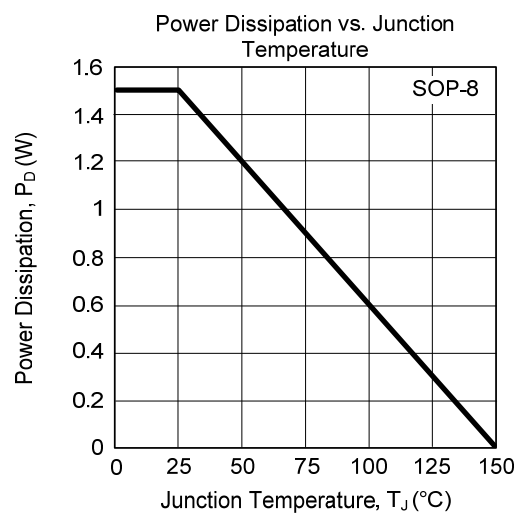
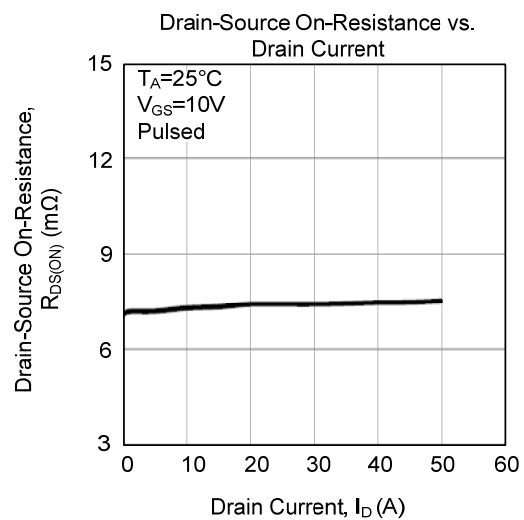
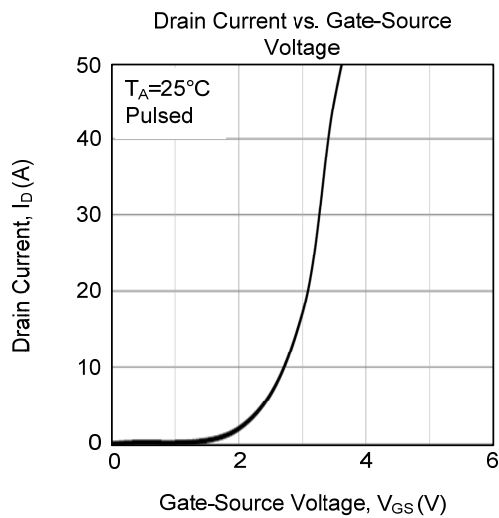
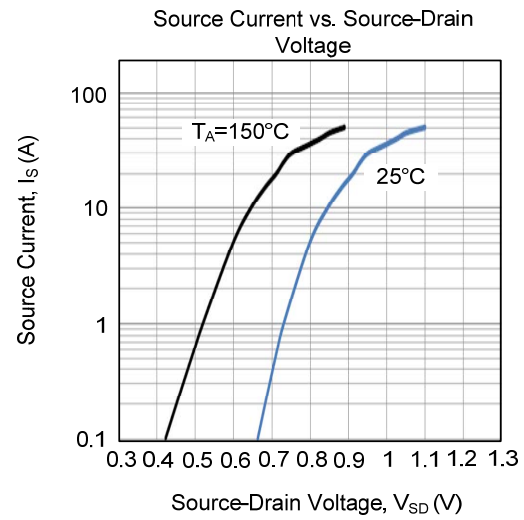
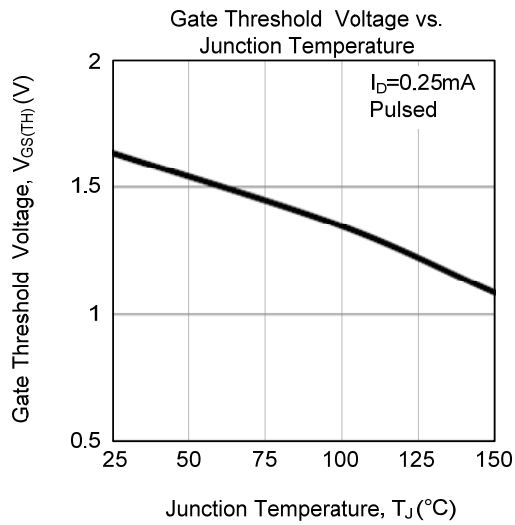


Unclamped Inductive Switching Waveforms

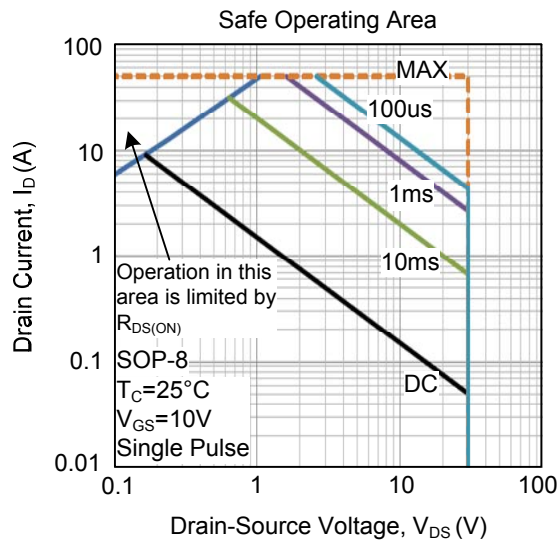
# TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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