UT54ACS193E

Synchronous 4-Bit Up-Down Dual Clock Counter
July 2013
www.aeroflex.com/Logic
Datasheet

A passion for performance.

FEATURES

- Look-ahead circuitry enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- 0.6μm CRH CMOS process
  - Latchup immune
- High speed
- Low power consumption
- Wide power supply operating range of 3.0V to 5.5V
- Available QML Q or V processes
- 16-lead flatpack
- UT54ACS193E - SMD 5962-96566

DESCRIPTION

The UT54ACS193E is a synchronous 4-bit, reversible up-down binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed. Synchronous operation eliminates the output counting spikes normally associated with asynchronous counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count input (Up or Down). The direction of the counting is determined by which count input is pulsed while the other count input is high.

The counter is fully programmable. The outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the count pulses. Asynchronous loading allows the counter to be used as modulo-N divider by simply modifying the count length with the preset inputs.

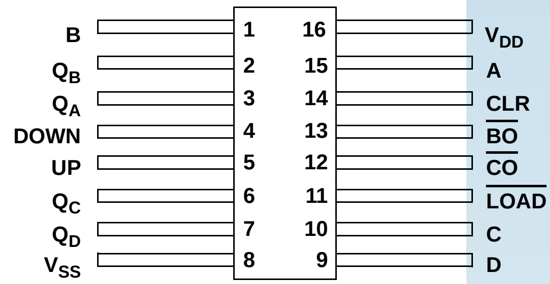
A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

The counter is designed for efficient cascading without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero and the down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum and the up input is low.

The device is characterized over full HiRel temperature range of -55°C to +125°C.

PINOUT

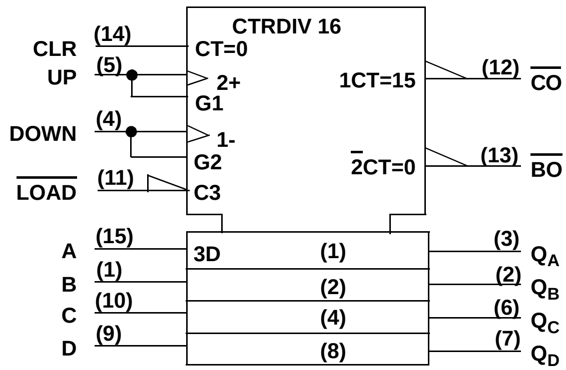
16-Lead Flatpack
TopView



FUNCTION TABLE

FUNCTION	CLOCK UP	CLOCK DOWN	CLR	$\overline{LOAD}$
Count Up	↑	H	L	H
Count Down	H	↑	L	H
Reset	X	X	H	X
Load Preset Input	X	X	L	L

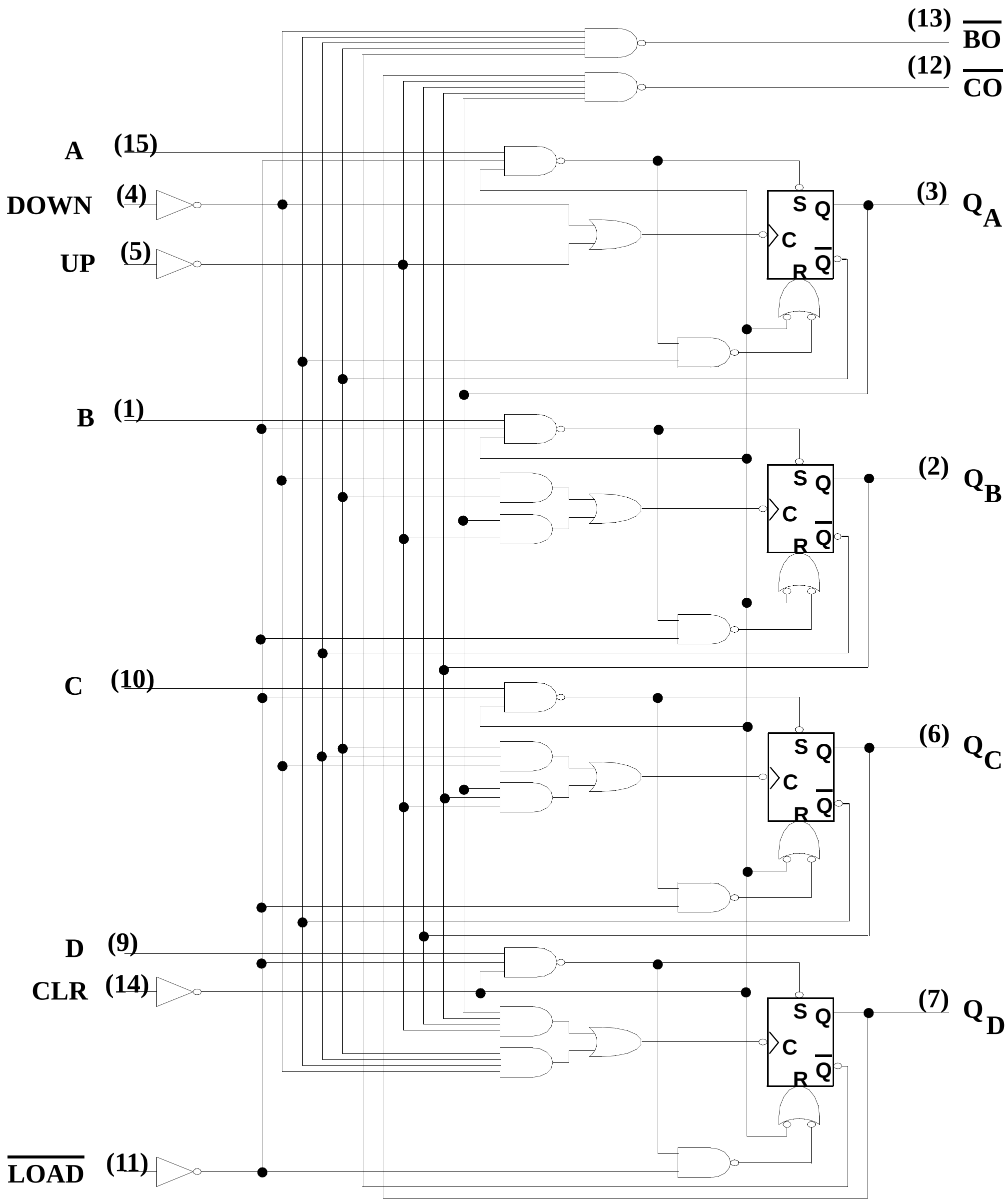
LOGIC SYMBOL



Note:

1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	108	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15	°C/W
I_I	DC input current	±10	mA
P_D [2]	Maximum package power dissipation permitted @ Tc = +125°C	3.3	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Per MIL-STD-883, method 1012.1, Section 3.4.1, $P_D = (T_{j(max)} - T_{c(max)}) / \Theta_{jc}$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	°C

DC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS193E[7]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[6]; -55°C < T_C < +125°C)

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage [1]	V_{DD} from 3.0V to 5.5V		0.3 V_{DD}	V
V_{IH}	High-level input voltage [1]	V_{DD} from 3.0V to 5.5V	0.7 V_{DD}		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage [3]	I_{OL} = 100µA V_{DD} from 3.0V to 5.5V		0.25	V
V_{OH}	High-level output voltage [3]	I_{OH} = -100µA V_{DD} from 3.0V to 5.5V	V_{DD} -0.25		V
I_{OS1}	Short-circuit output current [2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 4.5V to 5.5V	-200	200	mA
I_{OS2}	Short-circuit output current [2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 3.0V to 3.6V	-100	100	mA
I_{OL1}	Low level output current[9] (sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 4.5V to 5.5V	8		mA
I_{OL2}	Low level output current[9] (sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 3.0V to 3.6V	6		mA
I_{OH1}	High level output current[9] (source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 4.5V to 5.5V	-8		mA
I_{OH2}	High level output current[9] (source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 3.0V to 3.6V	-6		mA
P_{total1}	Power dissipation [8, 9]	C_L = 50pF V_{DD} = 4.5V to 5.5V		1.4	mW/ MHz
P_{total2}	Power dissipation [8, 9]	C_L = 50pF V_{DD} = 3.0V to 3.6V		0.6	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS} V_{DD} from 3.0V to 5.5V		10	µA

C_{IN}	Input capacitance [5]	f = 1MHz V_{DD} = 0V		15	pF
C_{OUT}	Output capacitance [5]	f = 1MHz V_{DD} = 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$(min) + 20%, - 0%; $V_{IL} = V_{IL}$(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rs maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose ≤ 1E6 rads(Si) per MIL-STD-883 Method 1019.
8. Power dissipation specified per switching output.
9. Guaranteed by characterization, but not tested.

AC ELECTRICAL CHARACTERISTICS FOR UT54ACS193E[2]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V [1], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	V_{DD}	MINIMUM	MAXIMUM	UNIT
t_{PLH1}	UP to Q_n	C_L = 50pF	3.0V to 3.6V	3	25	ns
			4.5V to 5.5V	3	15	
t_{PHL1}	UP to Q_n	C_L = 50pF	3.0V to 3.6V	4	27	ns
			4.5V to 5.5V	3	16	
t_{PLH2}	UP to $\overline{CO}$	C_L = 50pF	3.0V to 3.6V	2	17	ns
			4.5V to 5.5V	2	10	
t_{PHL2}	UP to $\overline{CO}$	C_L = 50pF	3.0V to 3.6V	2	20	ns
			4.5V to 5.5V	2	11	
t_{PLH3}	DOWN to $\overline{BO}$	C_L = 50pF	3.0V to 3.6V	2	17	ns
			4.5V to 5.5V	2	10	
t_{PHL3}	DOWN to $\overline{BO}$	C_L = 50pF	3.0V to 3.6V	2	20	ns
			4.5V to 5.5V	2	11	
t_{PLH4}	DOWN to Q_n	C_L = 50pF	3.0V to 3.6V	3	27	ns
			4.5V to 5.5V	3	15	
t_{PHL4}	DOWN to Q_n	C_L = 50pF	3.0V to 3.6V	4	27	ns
			4.5V to 5.5V	3	16	
t_{PLH5}	$\overline{LOAD}$ to Q_n	C_L = 50pF	3.0V to 3.6V	4	27	ns
			4.5V to 5.5V	3	16	
t_{PHL5}	$\overline{LOAD}$ to Q_n	C_L = 50pF	3.0V to 3.6V	4	26	ns
			4.5V to 5.5V	3	16	
t_{PHL6}	CLR to Q_n	C_L = 50pF	3.0V to 3.6V	4	25	ns
			4.5V to 5.5V	3	15	
f_{MAX}[3]	Maximum clock frequency	C_L = 50pF	3.0V to 3.6V		80	MHz
			4.5V to 5.5V		120	
t_{SU1}	$\overline{LOAD}$ inactive setup time before UP or DOWN ↑	C_L = 50pF	3.0V to 3.6V	1		ns
			4.5V to 5.5V	1		
t_{SU2}	CLR inactive setup time before UP or DOWN ↑	C_L = 50pF	3.0V to 3.6V	1		ns
			4.5V to 5.5V	1		

t_{SU3}	A, B, C, D setup time before $\overline{\text{LOAD}}$↑	C_L = 50pF	3.0V to 3.6V	4		ns
			4.5V to 5.5V	3		
t_{H1}	UP high hold time after DOWN ↑	C_L = 50pF	3.0V to 3.6V	5		ns
			4.5V to 5.5V	3		
t_{H2}	DOWN high hold time after UP ↑	C_L = 50pF	3.0V to 3.6V	6		ns
			4.5V to 5.5V	4		
t_{H3}	A, B, C, D hold time after $\overline{\text{LOAD}}$↑	C_L = 50pF	3.0V to 3.6V	0		ns
			4.5V to 5.5V	0		
t_W	Minimum pulse width UP high or low DOWN high or low $\overline{\text{LOAD}}$ low CLR high	C_L = 50pF	3.0V to 3.6V	8		ns
			4.5V to 5.5V	6		

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si) per MIL-STD-883 Method 1019 Condition A and section 3.11.2.
3. Maximum clock frequency f_{MAX} is the max rate at which the device will count up or down at the given voltage. However, the user must wait the appropriate UP-to-Qn or Down-to-Qn propagation delay time in order to observe the current counter value.

Packaging

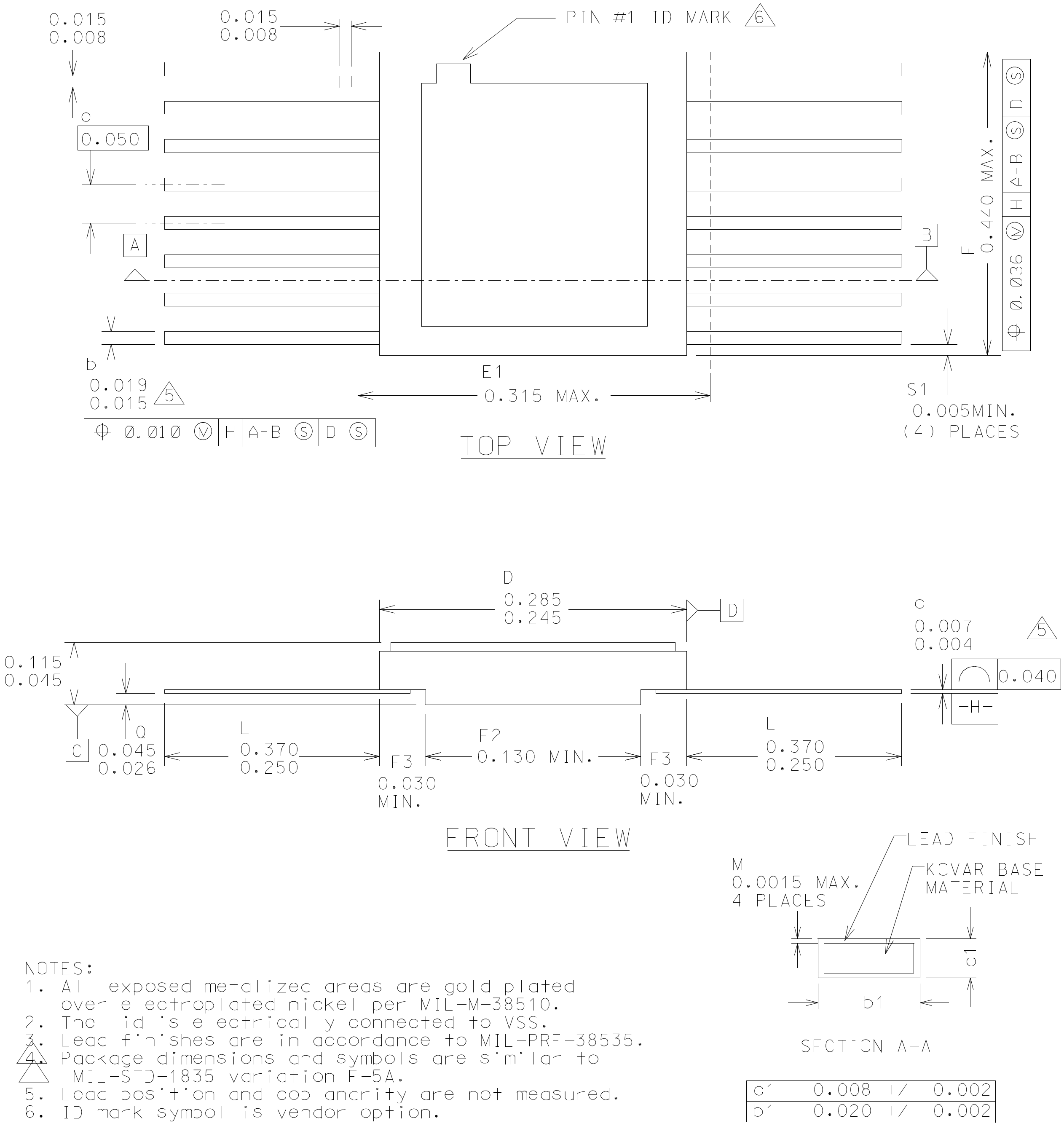


Figure 1. 16-Lead Flatpack

Ordering Information: UT54ACS193E: SMD

5962 * *** ** * * ***

Lead Finish: (Notes 1 to 2)
A = Solder
C = Gold
X = Optional

Package Type:
X = 16-lead ceramic bottom-brazed dual-in-line Flatpack

Class Designator:
Q = QML Class Q
V = QML Class V

Device Type:
02 = 1 rad(Si)/sec
03 = 50 to 300 rads(Si)/sec

Drawing Number:
96566 = UT54ACS193E

Total Dose: (Note 3 and 4)
R = 1E5 rads(Si)
F = 3E5 rads(Si)
G = 5E5 rads(Si)
H = 1E6 rads(Si)

Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML to Reduced HiRel

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