

# UT54ACTQ16244

RadHard CMOS 16-bit Buffer/Line Driver, TTL Inputs, and Three-State Outputs  
 Datasheet

May 16, 2012

www.aeroflex.com/radhard



## FEATURES

- ❑ 16 non-inverting buffers with three-state outputs
- ❑ Guaranteed simultaneously switching noise level and dynamic threshold performance
- ❑ Separate control logic for each byte and nibble
- ❑ 0.6µm Commercial RadHard™ CMOS
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune
- ❑ High speed, low power consumption
- ❑ Output source/sink 24mA
- ❑ Standard Microcircuit Drawing 5962-06243
  - QML compliant part
- ❑ Package:
  - 48-lead flatpack, 25 mil pitch (.390 x .640)

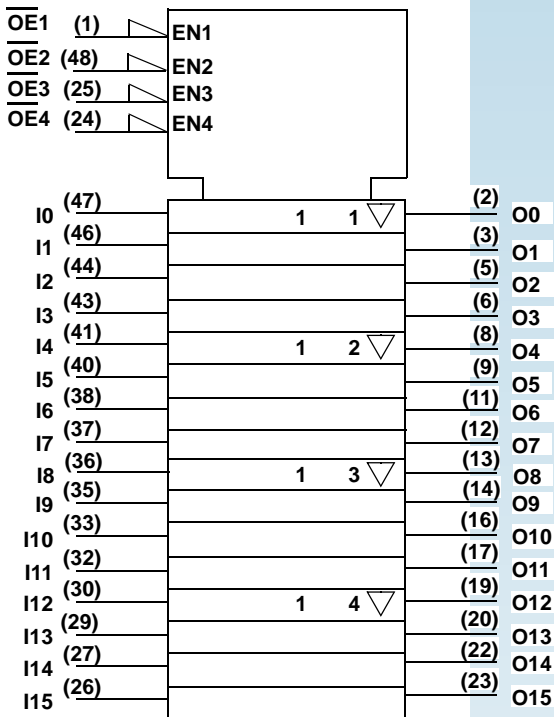
## DESCRIPTION

The 16-bit wide UT54ACTQ16244 buffer/line driver is built using Aeroflex's Commercial RadHard™ epitaxial CMOS technology and is ideal for space applications. This high speed, low power UT54ACTQ16244 buffer/line driver is designed to improve the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The UT54ACTQ16244 can be used as four 4-bit (nibble) buffers, two 8-bit (byte) buffers, or one 16-bit buffer. The device provides true outputs and symmetrical  $\overline{OE}$  (active-low) output-enable inputs. The device is nibble controlled with each nibble functioning identically, but independent of each other. The control pins can be shorted together to obtain full 16-bit operation.

## PIN DESCRIPTION

Pin Names	Description
$\overline{OE}n$	Output Enable Input (Active Low)
I0-I15	Inputs
O0-O15	Outputs

## LOGIC SYMBOL



## FUNCTION TABLE

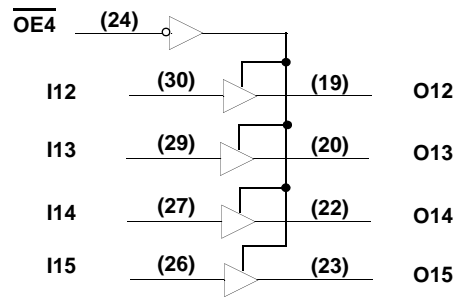
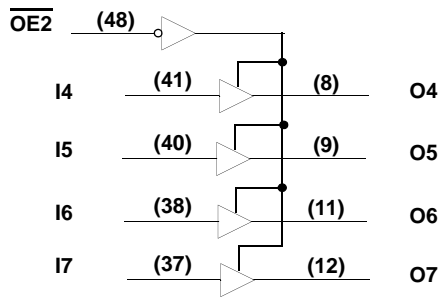
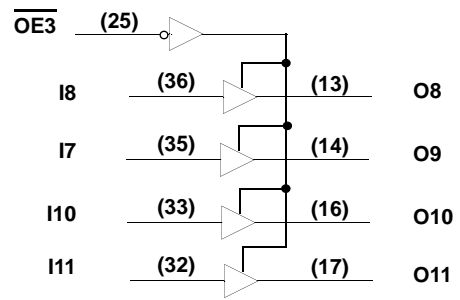
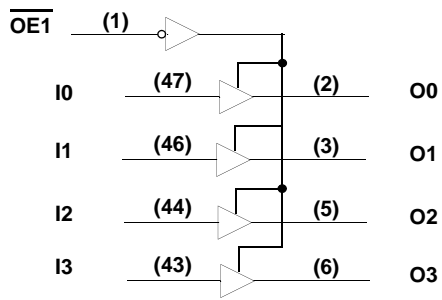
ENABLE $\overline{OE}1, \overline{OE}2,$ $\overline{OE}3, \overline{OE}4$	Inputs I0-I3, I4-I7, I8-I11, I12-I15	Outputs O0-O3, O4-O7, O8-O11, O12-O15
L	L	L
L	H	H
H	X	Z

# PINOUTS

## 48-Lead Flatpack Top View

$\overline{OE1}$	1	48	$\overline{OE2}$
O0	2	47	I0
O1	3	46	I1
V <sub>SS</sub>	4	45	V <sub>SS</sub>
O2	5	44	I2
O3	6	43	I3
V <sub>DD</sub>	7	42	V <sub>DD</sub>
O4	8	41	I4
O5	9	40	I5
V <sub>SS</sub>	10	39	V <sub>SS</sub>
O6	11	38	I6
O7	12	37	I7
O8	13	36	I8
O9	14	35	I9
V <sub>SS</sub>	15	34	V <sub>SS</sub>
O10	16	33	I10
O11	17	32	I11
V <sub>DD</sub>	18	31	V <sub>DD</sub>
O12	19	30	I12
O13	20	29	I13
V <sub>SS</sub>	21	28	V <sub>SS</sub>
O14	22	27	I14
O15	23	26	I15
$\overline{OE4}$	24	25	$\overline{OE3}$

# LOGIC DIAGRAM



## RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rad(Si)
SEL Immune	>108	MeV-cm <sup>2</sup> /mg
SEU Onset Let	N/A <sup>3</sup>	MeV-cm <sup>2</sup> /mg
Neutron Fluence <sup>2</sup>	1.0E14	n/cm <sup>2</sup>

**Notes:**

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent of CMOS technology.
3. This device contains no memory storage elements which can be upset.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
V <sub>I/O</sub>	Voltage any pin during operation	-.3 to V <sub>DD</sub> +.3	V
V <sub>DD</sub>	Supply voltage	-0.3 to 6.0	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub>	Maximum power dissipation	310	mW

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	4.5 to 5.5	V
V <sub>IN</sub>	Input voltage any pin	0 to V <sub>DD</sub>	V
T <sub>C</sub>	Temperature range	-55 to + 125	°C
t <sub>INRISE</sub> t <sub>INFALL</sub>	Maximize input rise or fall time (V <sub>IN</sub> transitioning between V <sub>IL</sub> (max) and V <sub>IH</sub> (min))	20	ns

## DC ELECTRICAL CHARACTERISTICS <sup>1</sup>

(-55°C < T<sub>C</sub> < +125°C)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V <sub>IL</sub>	Low level input voltage <sup>2</sup>	V <sub>DD</sub> from 4.5 to 5.5V			0.8	V
V <sub>IH</sub>	High level input voltage <sup>2</sup>	V <sub>DD</sub> from 4.5 to 5.5V		2.0		V
I <sub>IN</sub>	Input leakage current <sup>3</sup>	V <sub>DD</sub> from 4.5V to 5.5V V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		-1	1	μA
I <sub>OZ</sub>	Three-state output leakage current <sup>3</sup>	V <sub>DD</sub> from 4.5V to 5.5V V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		-10	10	μA
I <sub>OS</sub>	Short-circuit output current <sup>4, 5</sup>	V <sub>O</sub> = V <sub>DD</sub> or V <sub>SS</sub> V <sub>DD</sub> from 4.5V to 5.5V		-600	600	mA
V <sub>OL1</sub>	Low-level output voltage <sup>3, 6</sup>	I <sub>OL</sub> = 24mA I <sub>OL</sub> = 24mA I <sub>OL</sub> = 100μA V <sub>DD</sub> = 4.5V to 5.5V V <sub>IN</sub> = 0.8V to 2.0V	-55°C, 25°C		0.36	V
			+125°C		0.5	
			-55°C, 25°C, +125°C		0.2	
V <sub>OL2</sub>	Low-level output voltage <sup>3, 6, 7</sup>	I <sub>OL</sub> = 50mA V <sub>IN</sub> = 2.0V or 0.8V V <sub>DD</sub> = 5.5V V <sub>IN</sub> = 0.8V to 2.0V	-55°C, 25°C		0.8	V
			+125°C		1.0	
V <sub>OH1</sub>	High-level output voltage <sup>3, 6</sup>	I <sub>OH</sub> = -24mA I <sub>OH</sub> = -24mA I <sub>OH</sub> = -100μA V <sub>DD</sub> = 4.5V to 5.5V V <sub>IN</sub> = 0.8V to 2.0V	-55°C, 25°C	V <sub>DD</sub> - 0.64		V
			+125°C	V <sub>DD</sub> - 0.8		
			-55°C, 25°C, +125°C	V <sub>DD</sub> - 0.2		
V <sub>OH2</sub>	High-level output voltage <sup>3, 6, 7</sup>	I <sub>OH</sub> = -50mA V <sub>IN</sub> = 2.0V or 0.8V V <sub>DD</sub> = 5.5V V <sub>IN</sub> = 0.8V to 2.0V	-55°C, 25°C	V <sub>DD</sub> - 1.1		V
			+125°C	V <sub>DD</sub> - 1.3		
V <sub>IC+</sub>	Positive input clamp voltage	For input under test, I <sub>IN</sub> = 18mA V <sub>DD</sub> = 0.0V		0.4	1.5	V
V <sub>IC-</sub>	Negative input clamp voltage	For input under test, I <sub>IN</sub> = -18mA V <sub>DD</sub> = open		-1.5	-0.4	V

$P_{total}$	Power dissipation <sup>8, 9, 10</sup>	$C_L = 20\text{pF}$ $V_{DD}$ from 4.5V to 5.5V		1.0	mW/ MHz
$I_{DDQ}$	Standby Supply Current $V_{DD}$  Pre-Rad 25°C Pre-Rad -55°C to +125°C Post-Rad 25°C	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 5.5\text{V}$ $\overline{OEn} = V_{DD}$ $\overline{OEn} = V_{DD}$ $\overline{OEn} = V_{DD}$		10 160 160	$\mu\text{A}$
$\Delta I_{DDQ}$	Quiescent Supply Current Delta, TTL input level	For input under test $V_{IN} = V_{DD} - 2.1\text{V}$ For other inputs  $V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 5.5\text{V}$		1.6	mA
$C_{IN}$	Input capacitance <sup>11</sup>	$f = 1\text{MHz @ } 0\text{V}$ $V_{DD}$ from 4.5V to 5.5V		15	pF
$C_{OUT}$	Output capacitance <sup>11</sup>	$f = 1\text{MHz @ } 0\text{V}$ $V_{DD}$ from 4.5V to 5.5V		15	pF
$V_{OLP}$ $V_{OLV}$	Low level $V_{SS}$ bounce noise <sup>12</sup>	$V_{IH} = 3.0\text{V}$ , $V_{IL} = 0.0\text{V}$ , $T_A = +25^\circ\text{C}$ , $V_{DD} = 5.0\text{V}$		1000 -1000	mV mV
$V_{OHP}$ $V_{OHV}$	High level $V_{DD}$ bounce noise <sup>12</sup>	See figure "Quiet Output Under Test"		$V_{OH}$ +1000 $V_{OH}$ -1300	mV mV

**Notes:**

- All specifications valid for radiation dose  $\leq 1\text{E}5$  rad(Si) per MIL-STD-883, Method 1019.
- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH}(\text{min}) + 20\%$ ,  $- 0\%$ ;  $V_{IL} = V_{IL}(\text{max}) + 0\%$ ,  $- 50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$ .
- Guaranteed; tested on a sample of pins per device.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Supplied as a design limit, but not guaranteed or tested.
- Per MIL-PRF-38535, for current density  $\leq 5.0\text{E}5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
- Transmission driving tests are performed at  $V_{DD} = 5.5\text{V}$ , only one output loaded at a time with a duration not to exceed 2ms. The test is guaranteed, if not tested, for  $V_{IN} = V_{IH}$  minimum or  $V_{IL}$  maximum.
- Guaranteed by characterization.
- Power does not include power contribution of any CMOS output sink current.
- Power dissipation specified per switching output.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- This test is for qualification only.  $V_{SS}$  and  $V_{DD}$  bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture.

## AC ELECTRICAL CHARACTERISTICS<sup>1</sup>

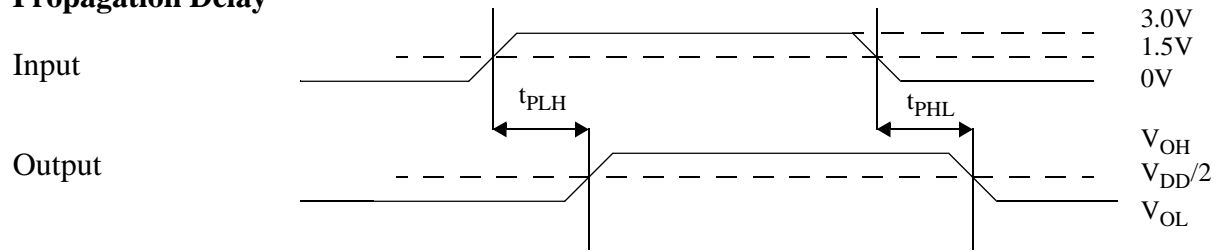
( $V_{DD} = 5V \pm 10\%$ ;  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{PLH}$	Propagation delay In to On	2	8.0	ns
$t_{PHL}$	Propagation delay In to On	2	8.0	ns
$t_{PZL}$	Output enable time $\overline{OEn}$ to On	2	8.0	ns
$t_{PZH}$	Output enable time $\overline{OEn}$ to On	2	8.0	ns
$t_{PLZ}$	Output disable time $\overline{OEn}$ to On	2	9.5	ns
$t_{PHZ}$	Output disable time $\overline{OEn}$ to On	2	9.5	ns
$t_{SKEW}^2$	Output-to-output skew	-	1.0	ns
$t_{DSKEW}^3$	Differential skew between outputs		1.6	ns
$t_{SKEWPP}^{2,4}$	Part-to-Part output skew		500	ps

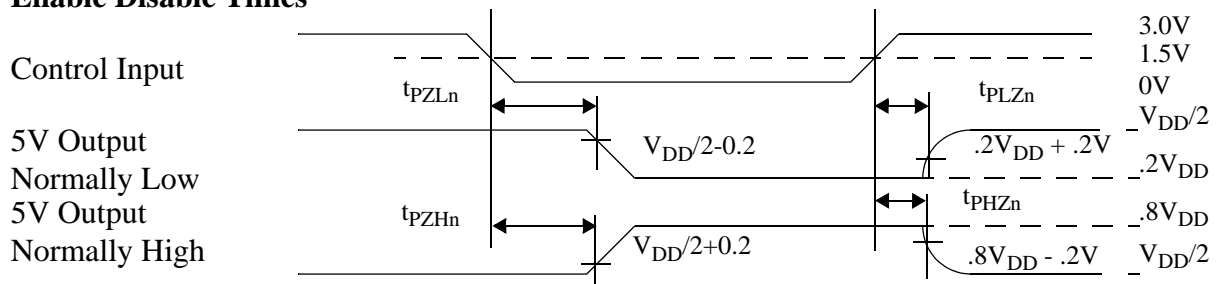
### Notes:

1. All specifications valid for radiation dose  $\leq 1E5$  rad(Si) per MIL-STD-883, Method 1019.
2. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs low-to-high.
3. Differential skew is defined as a comparison of any two output transitions high-to-low vs. low-to-high and low-to-high vs high-to low.
4. Guaranteed by characterization, but not tested.

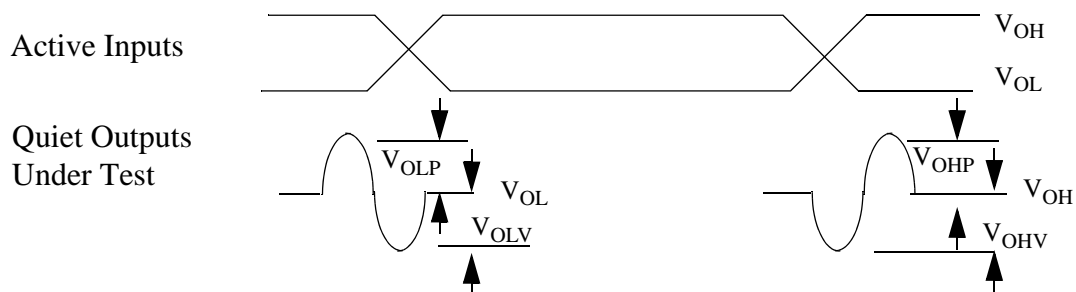
### Propagation Delay



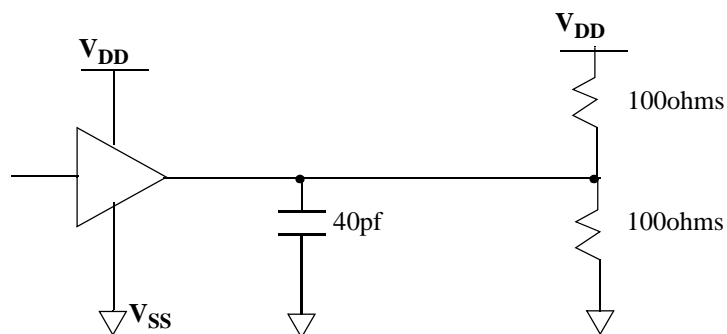
### Enable Disable Times



### Bounce Noise



### Test Load or Equivalent<sup>1</sup>

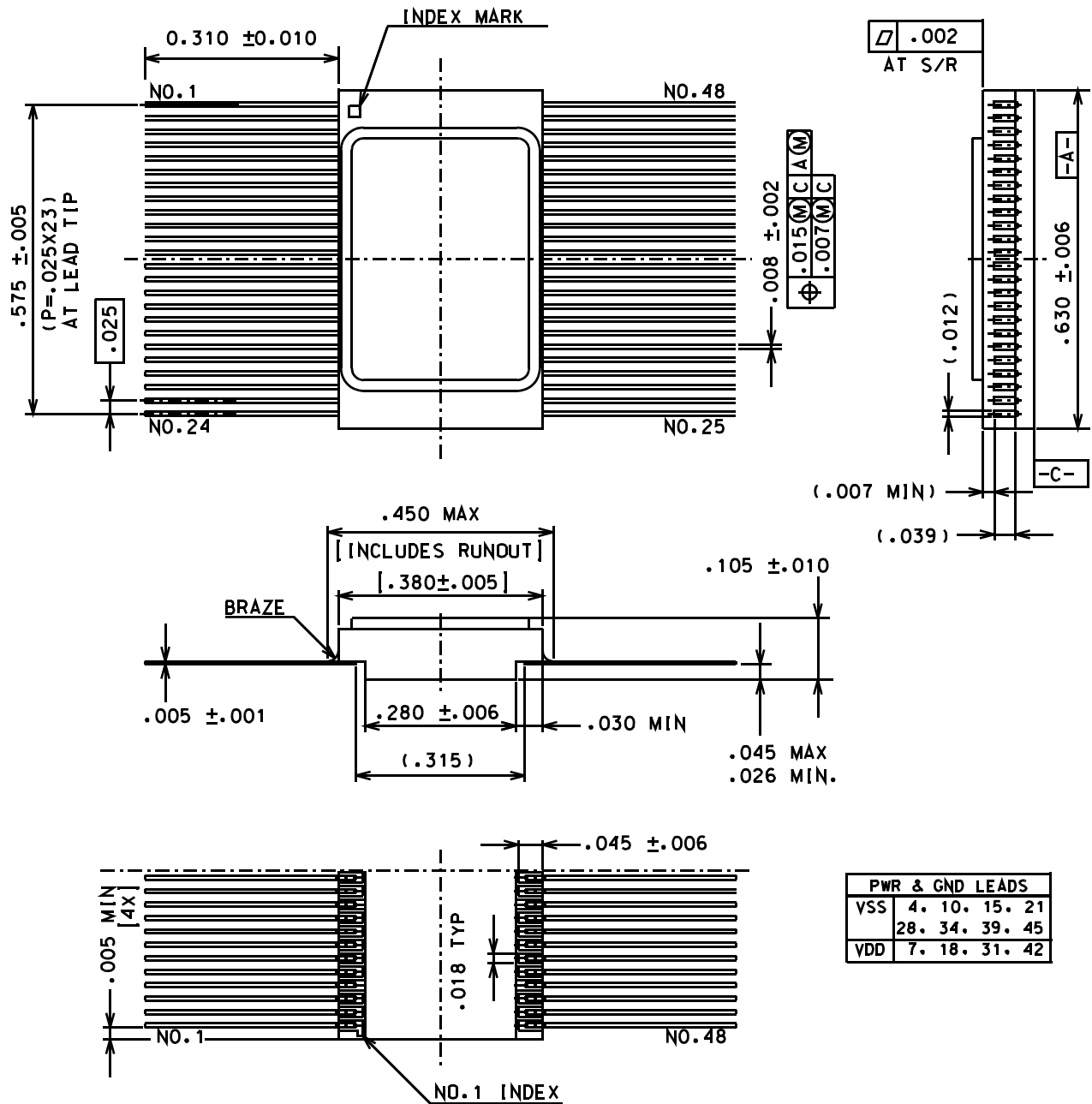


#### Notes

1. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.



# PACKAGE



**NOTE:**

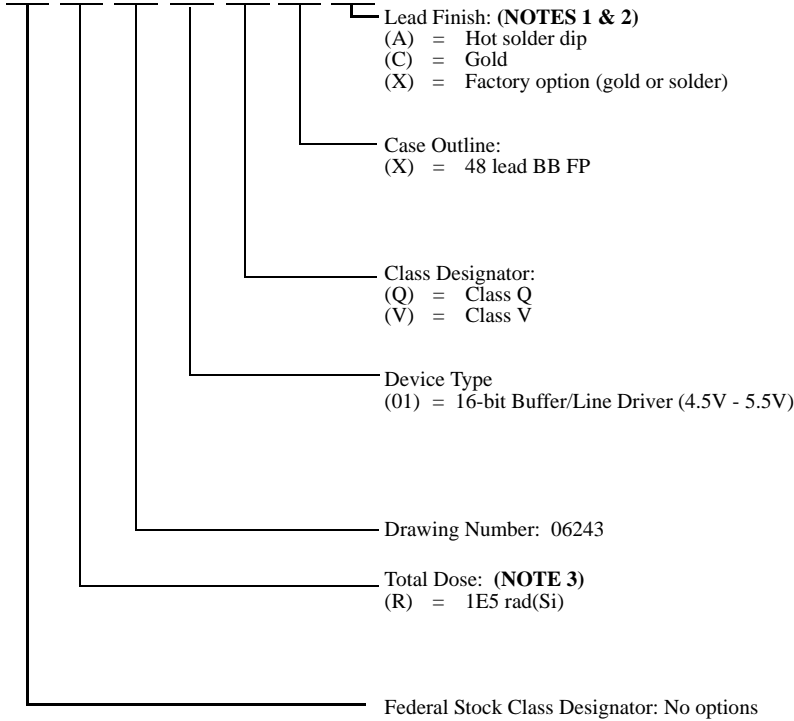
1. Seal ring is connected to  $V_{SS}$ .
2. Units are in inches.
3. All exposed metalized areas must be gold plated 100 to 225 microinches thick. Dyer electroplated nickel undercoating 100 to 350 microinches per MIL-PRF-38535.

**Figure 1. 48-Lead Flatpack**

# ORDERING INFORMATION

## UT54ACTQ16244: SMD

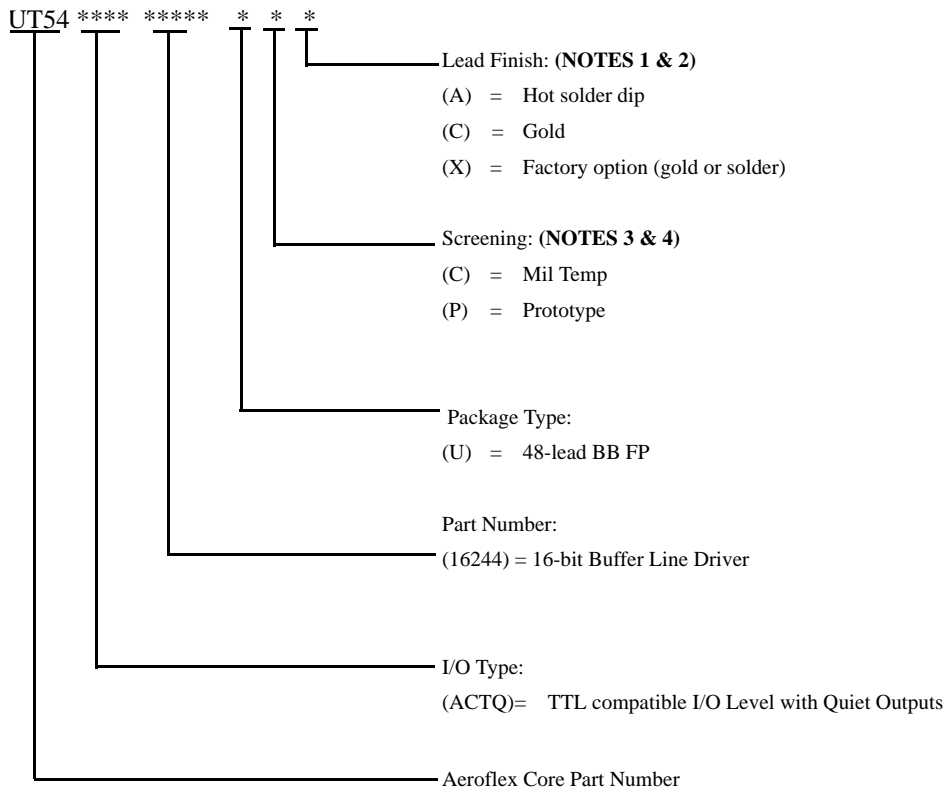
5962 R 06243 \*\* \* \* \*



### Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q not available without radiation hardening. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

## UT54ACTQ16244



### Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Manufacturing Flows Document. Tested at 25°C only. Lead finish is Gold "C" only. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

# ***Aeroflex Colorado Springs - Datasheet Definition***

**Advanced Datasheet - Product In Development**

**Preliminary Datasheet - Shipping Prototype**

**Datasheet - Shipping QML & Reduced Hi-Rel**

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