

UT54ACTQ16374

RadHard CMOS 16-bit D Flip-Flop TTL Inputs, and Three-State Outputs
 Datasheet

May 16, 2012

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FEATURES

- ❑ 16 non-inverting D flip-flops with three-state outputs
- ❑ Guaranteed simultaneously switching noise level and dynamic threshold performance
- ❑ Buffered positive edge-triggered clock
- ❑ Separate control logic for each byte
- ❑ Guaranteed pin-to-pin output skew
- ❑ 0.6µm Commercial RadHard™ CMOS
 - Total dose: 100K rad(Si)
 - Single Event Latchup immune
 - SEU Onset LET >95 MeV -cm²/mg
- ❑ High speed, low power consumption
- ❑ Output source/sink 24mA
- ❑ Standard Microcircuit Drawing 5962-06245
 - QML compliant part
- ❑ Package:
 - 48-lead flatpack, 25 mil pitch (.390 x .640)

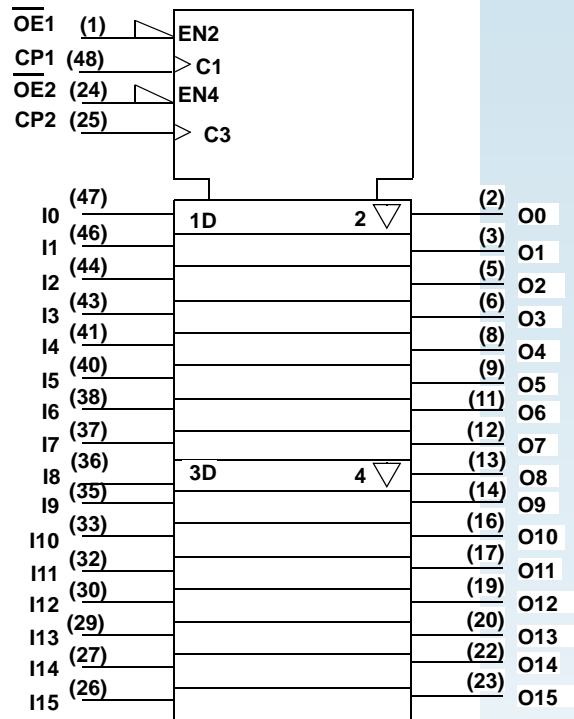
DESCRIPTION

The 16-bit wide UT54ACTQ16374 D flip-flop is built using Aeroflex's Commercial RadHard™ epitaxial CMOS technology and is ideal for space applications. This high-speed, low power UT54ACTQ16374 D flip-flop is designed for bus oriented applications. A buffered clock (CP) and Output Enable (\overline{OE}) are common to each byte and can be shorted together for full 16-bit operation. The UT54ACTQ16374 are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers and working registers. Each flip-flop will store the state of their individual D inputs (In) that meet the setup and hold requirements on the low-to-high clock (CPn) transition. With the Output Enable (\overline{OE}) low, the contents of the flip-flops are available at the output. When \overline{OE} is high, the outputs go to high impedance state. Operation of \overline{OE} input does not affect the state of the D flip-flops.

PIN DESCRIPTION

Pin Names	Description
\overline{OE} n	Output Enable Input (Active Low)
CPn	Clock Pulse Input
I0-I15	Inputs
O0-O15	Outputs

LOGIC SYMBOL



PINOUTS

48-Lead Flatpack Top View

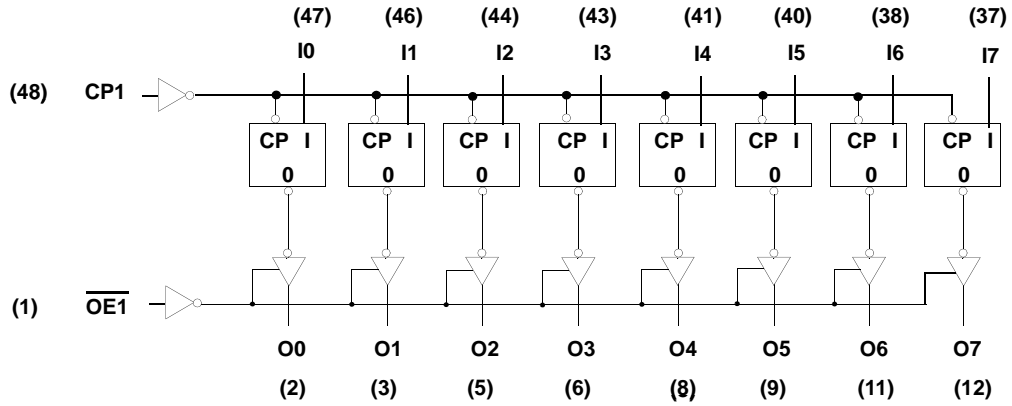
$\overline{\text{OE1}}$	1	48	CP1
O0	2	47	I0
O1	3	46	I1
V _{SS}	4	45	V _{SS}
O2	5	44	I2
O3	6	43	I3
V _{DD}	7	42	V _{DD}
O4	8	41	I4
O5	9	40	I5
V _{SS}	10	39	V _{SS}
O6	11	38	I6
O7	12	37	I7
O8	13	36	I8
O9	14	35	I9
V _{SS}	15	34	V _{SS}
O10	16	33	I10
O11	17	32	I11
V _{DD}	18	31	V _{DD}
O12	19	30	I12
O13	20	29	I13
V _{SS}	21	28	V _{SS}
O14	22	27	I14
O15	23	26	I15
$\overline{\text{OE2}}$	24	25	CP2

FUNCTION TABLE

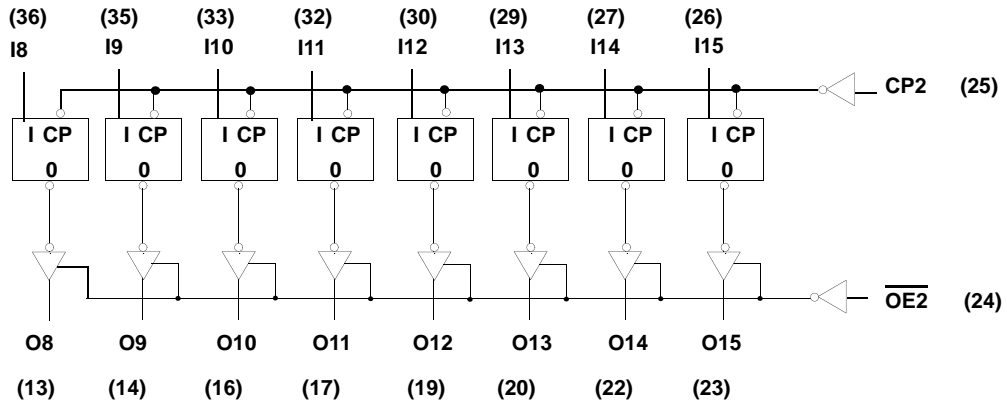
INPUTS			OUTPUT	OPERATION
\overline{OEn}	CPn	In	On	
H	H	L	Z	Hold
H	H	H	Z	Hold
H	↑	L	Z	Load
H	↑	H	Z	Load
L	↑	L	L	Data Available
L	↑	H	H	Data Available
L	H	L	Qo	No change in data
L	H	H	Qo	No change in data

LOGIC DIAGRAM

BYTE 1 (0:7)



BYTE 2 (8:15)



RADIATION HARDNESS SPECIFICATIONS¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rad(Si)
SEL Immune	>108	MeV-cm ² /mg
SEU Onset LET	>95	MeV-cm ² /mg
Neutron Fluence ²	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent of CMOS technology.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
V _{I/O}	Voltage any pin during operation	-.3 to V _{DD} +.3	V
V _{DD}	Supply voltage	-0.3 to 6.0	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
Θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	310	mW

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C
t _{INRISE} t _{INFALL}	Maximum input rise or fall time (V _{IN} transitioning between V _{IL} (max) and V _{IH} (min))	20	ns

DC ELECTRICAL CHARACTERISTICS ¹

(-55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V _{IL}	Low level input voltage ²	V _{DD} from 4.5V to 5.5V		0.8	V
V _{IH}	High level input voltage ²	V _{DD} from 4.5V to 5.5V	2.0		V
I _{IN}	Input leakage current ³	V _{DD} from 4.5V to 5.5V V _{IN} = V _{DD} or V _{SS}	-1	1	μA
I _{OZ}	Three-state output leakage current	V _{DD} from 4.5V to 5.5V V _{IN} = V _{DD} or V _{SS}	-10	10	μA
I _{OS}	Short-circuit output current ^{4, 5}	V _O = V _{DD} or V _{SS} V _{DD} from 4.5V to 5.5V	-600	600	mA
V _{OL1}	Low-level output voltage ⁵	I _{OL} = 24mA I _{OL} = 24mA I _{OL} = 100μA V _{IN} = 2V or 0.8V V _{DD} = 4.5V to 5.5V	-55C, 25C	0.36	V
			+125C	0.5	
			-55C, 25C, +125C	0.2	
V _{OL2}	Low-level output voltage ^{5,6}	I _{OL} = 50mA V _{IN} = 2.0V or 0.8V V _{DD} = 5.5V	-55C, 25C	0.8	V
			+125C	1.0	
V _{OH1}	High-level output voltage ⁵	I _{OH} = -24mA I _{OH} = -24mA I _{OH} = -100μA V _{IN} = 2V or 0.8V V _{DD} = 4.5V to 5.5V	-55C, 25C	V _{DD} - 0.64	V
			+125C	V _{DD} - 0.8	
			-55C, 25C, +125C	V _{DD} - 0.2	
V _{OH2}	High-level output voltage ^{5,6}	I _{OH} = -50mA V _{IN} = 2.0V or 0.8V V _{DD} = 5.5V	-55C, 25C	V _{DD} - 1.1	V
			+125C	V _{DD} - 1.3	
V _{IC+}	Positive input clamp voltage	For input under test, I _{IN} = 18mA V _{DD} = 0.0V	0.4	1.5	V
V _{IC-}	Negative input clamp voltage	For input under test, I _{IN} = -18mA V _{DD} = open	-1.5	-0.4	V

P_{total}	Power dissipation ^{7,6,9}	$C_L = 20\text{pF}$ V_{DD} from 4.5V to 5.5V		0.5	mW/ MHz
I_{DDQ}	Standby Supply Current V_{DD} Pre-Rad 25°C -55°C to +125°C Post-Rad 25°C	$V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5\text{V}$ $\overline{OEn} = V_{DD}$ $\overline{OEn} = V_{DD}$ $\overline{OEn} = V_{DD}$		10 160 160	μA
ΔI_{DDQ}	Quiescent Supply Current Delta, TTL input level	For input under test $V_{IN} = V_{DD} - 2.1\text{V}$ For other inputs $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5\text{V}$		1.6	mA
C_{IN}	Input capacitance ¹⁰	$f = 1\text{MHz @ } 0\text{V}$ V_{DD} from 4.5V to 5.5V		15	pF
C_{OUT}	Output capacitance ¹⁰	$f = 1\text{MHz @ } 0\text{V}$ V_{DD} from 4.5V to 5.5V		15	pF
V_{OLP} V_{OLV}	Low level V_{SS} bounce noise ¹¹	$V_{IN} = 3.0\text{V}$, $V_{IL} = 0.0\text{V}$, $T_A = +25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$		1100 -1300	mV mV
V_{OHP} V_{OHV}	High level V_{DD} bounce noise ¹¹	See figure "Quiet Output Under Test"		$V_{OH} + 1200$ $V_{OH} - 1400$	mV mV

Notes:

- All specifications valid for radiation dose $\leq 1\text{E}5$ rad(Si) per MIL-STD-883, Method 1019.
- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\text{min}) + 20\%$, $- 0\%$; $V_{IL} = V_{IL}(\text{max}) + 0\%$, $- 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Supplied as a design limit, but not guaranteed or tested.
- Per MIL-PRF-38535, for current density $\leq 5.0\text{E}5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
- Transmission driving tests are performed at $V_{DD} = 5.5\text{V}$, only one output loaded at a time with a duration not to exceed 2ms. The test is guaranteed, if not tested, for $V_{IN} = V_{IH}$ minimum or V_{IL} maximum.
- Guaranteed by characterization.
- Power does not include power contribution of any CMOS output sink current.
- Power dissipation specified per switching output.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- This test is for qualification only. V_{SS} and V_{DD} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture.

AC ELECTRICAL CHARACTERISTICS¹

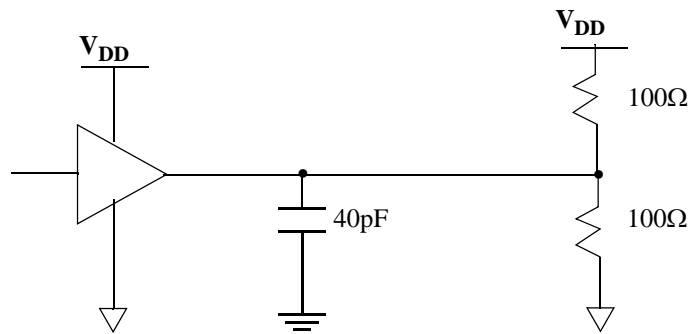
($V_{DD} = 5V \pm 10\%$, $-55^{\circ}C < T_C < +125^{\circ}C$)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{PLH}	Propagation delay CPn to On	2	10	ns
t_{PHL}	Propagation delay CPn to On	2	10	ns
t_{PZL}	Output enable time \overline{OEn} to On	2	9.0	ns
t_{PZH}	Output enable time \overline{OEn} to On	2	9.0	ns
t_{PLZ}	Output disable time \overline{OEn} to On high impedance	2	9.0	ns
t_{PHZ}	Output disable time \overline{OEn} to On high impedance	2	9.0	ns
t_{FMAX}^2	Maximum clock frequency		100	MHz
t_S	Setup time high or low In to CPn	1.5		ns
t_H	Hold time high or low In from CPn	0.5		ns
t_W	Clock pulse, high or low CPn	5.0		ns
t_{SKEW}^3	Output-to-output skew		1.25	ns
t_{DSKEW}^3	Differential skew between outputs		1.5	ns
$t_{DSKEWPP}^{3,5}$	Part-to-part output skew between outputs on multiple devices under identical system conditions.		500	ps

Notes:

1. All specifications valid for radiation dose $\leq 1E5$ rad(Si) per MIL-STD-883, Method 1019.
2. Verified by functional testing.
3. Output skew is defined as a comparison of any two output transitions high-to-low vs. high-to-low and low-to-high vs low-to-high.
4. Differential skew is defined as a comparison of any two output transitions high-to-low vs. low-to-high and low-to-high vs high-to low.
5. Guaranteed by characterization, but not tested.

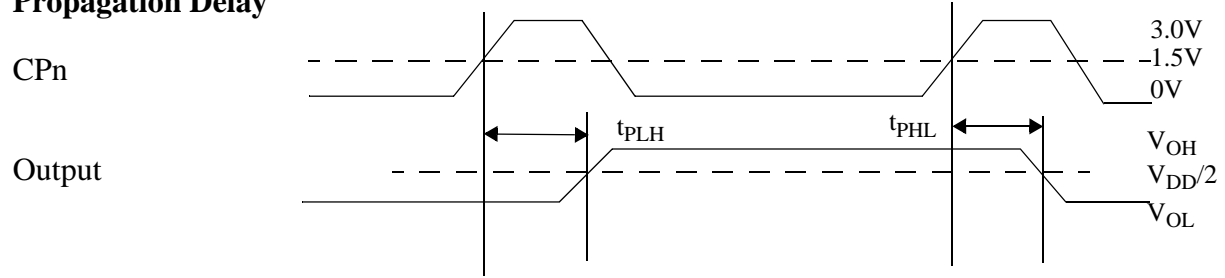
Test Load or Equivalent¹



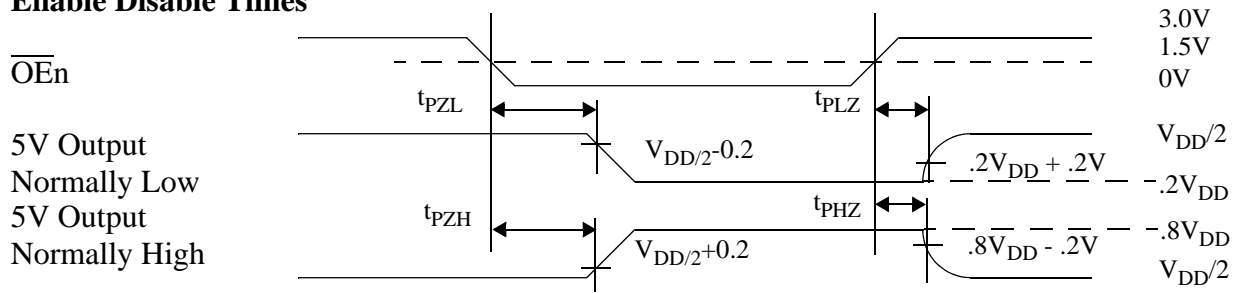
Notes

1. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

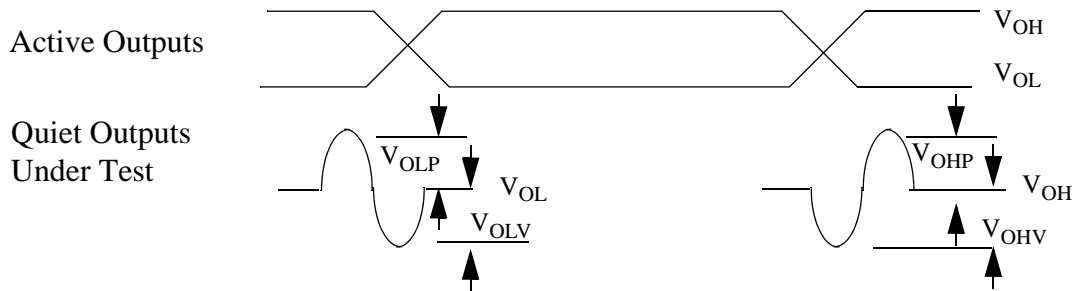
Propagation Delay



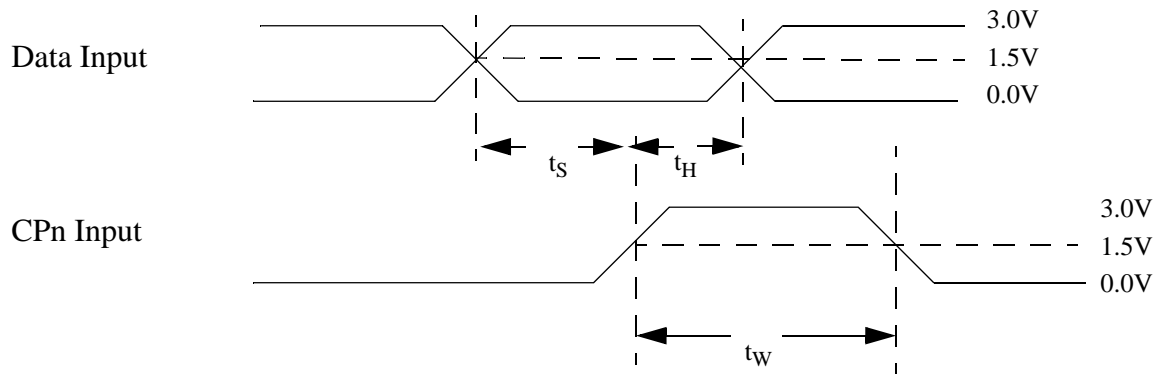
Enable Disable Times



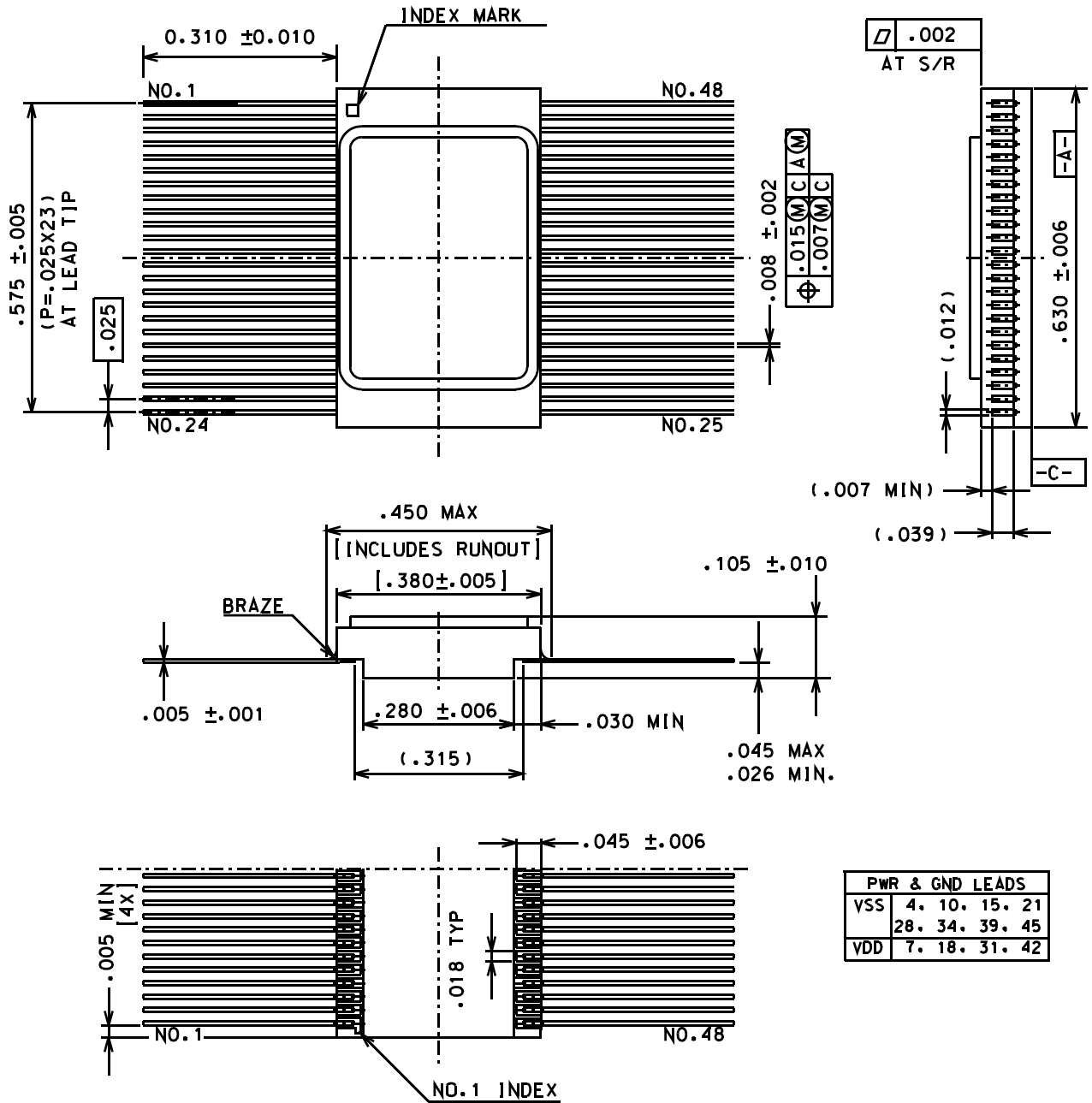
Bounce Noise



Setup and Hold Measurements



PACKAGE



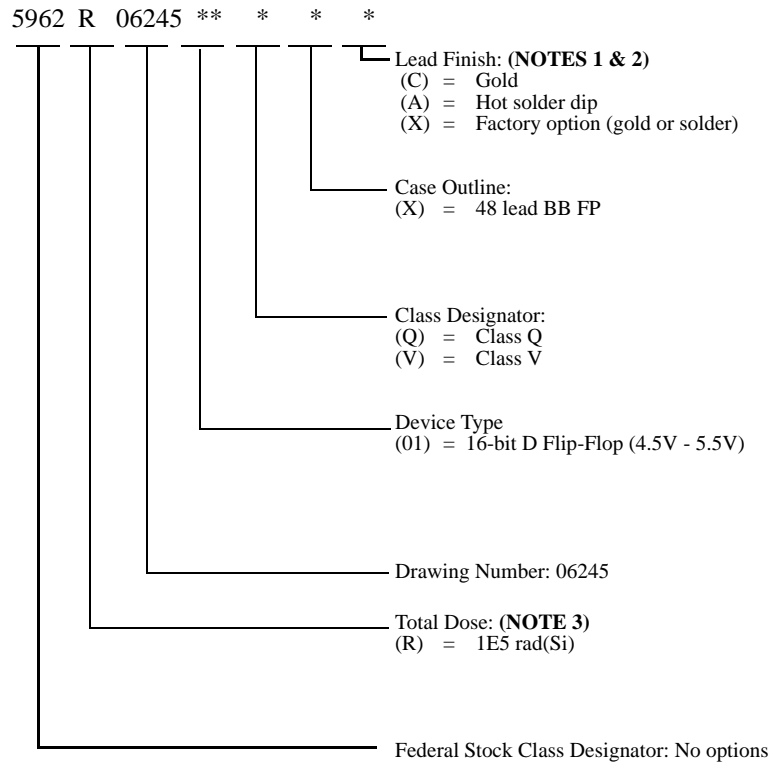
NOTE:

1. Seal ring is connected to V_{SS} .
2. Units are in inches.
3. All exposed metallized areas must be gold plated 100 to 225 microinches thick. Dyer electroplated nickel undercoating 100 to 350 microinches per MIL-PRF-38535.

Figure 1. 48-Lead Flatpack

ORDERING INFORMATION

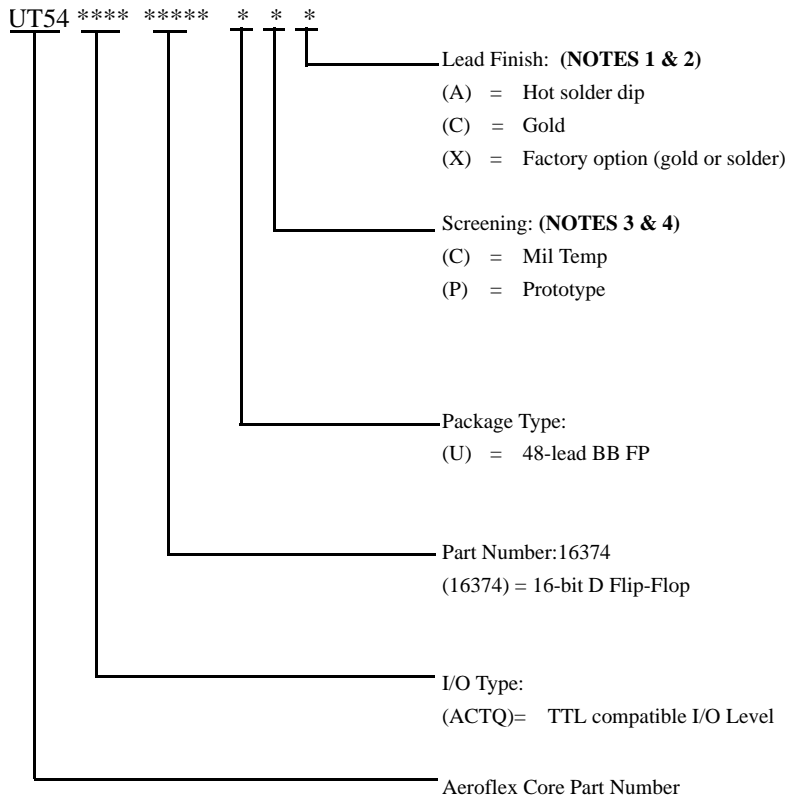
UT54ACTQ16374: SMD



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q not available without radiation hardening.

UT54ACTQ16374



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Manufacturing Flows Document. Tested at 25°C only. Lead finish is Gold "C" only. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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