Standard Products

UT54BS32245 32bit Bus Switch

Preliminary Datasheet
May 2015
www.aeroflex.com/busswitch

FEATURES

□ Provides cold-sparing capability without the need for actual cold-sparing multiplexer inputs
□ Bidirectional Operation
□ 3.3 V operating power supply with typical 11Ω switch connection between ports
□ 5.0V operating power supply typical 5Ω switch connection between ports
□ Isolates non cold-spared devices from an active bus
□ Ultra low power CMOS technology
□ ESD Rating HBM: 2000V, Class 2
□ Operational environment:
- Total-dose: up to 300 krad(Si)
- Latchup immune (LET <= 100 MeV-cm^2/mg)

□ Packaging options:
- 99-lead CCGA, CLGA, CBGA

□ Standard Microcircuit Drawing (SMD)
- QML Q and V pending

INTRODUCTION

The UT54BS32245 provides 32 bits of high-speed CMOS-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When output enable (/EN) is low, the switch is on and port A is connected to port B. When /EN is high, the switch is open and the high-impedance state exists between the two ports.

APPLICATIONS INFORMATION

Memory Interface
- Solution for multiple memory devices on a bus

Bus Isolation
- Ability to electrically isolate a device, or banks of devices, from memory bus or ADC output when not needed
- Enables bank switching for redundancy or device failure
- Provides cold-sparing capability without the need for actual cold-sparing buffers

Redundancy
- Allows multiple non cold-spare devices to be present on a bus

Supports Analog Applications
- In voltage range: 3.0 to 3.6V or 4.5 to 5.5V
- Signal isolation: -60dB
- Bandwidth (3dB): 500 MHz

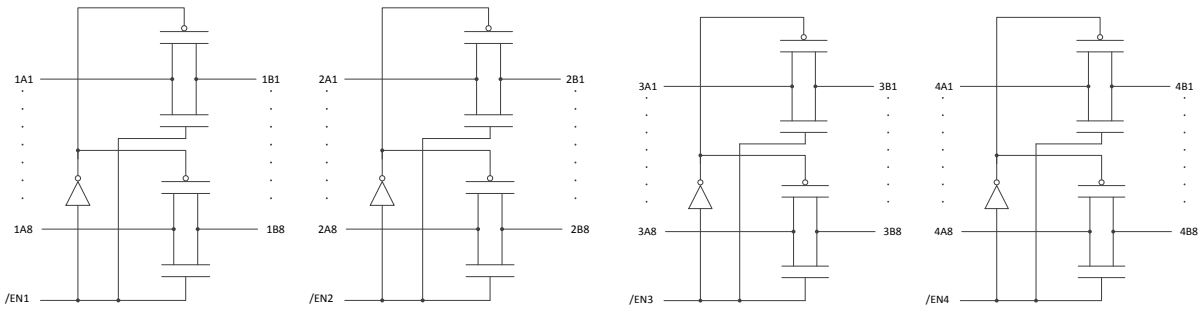


Figure 1. UT54BS32245 Block Diagram

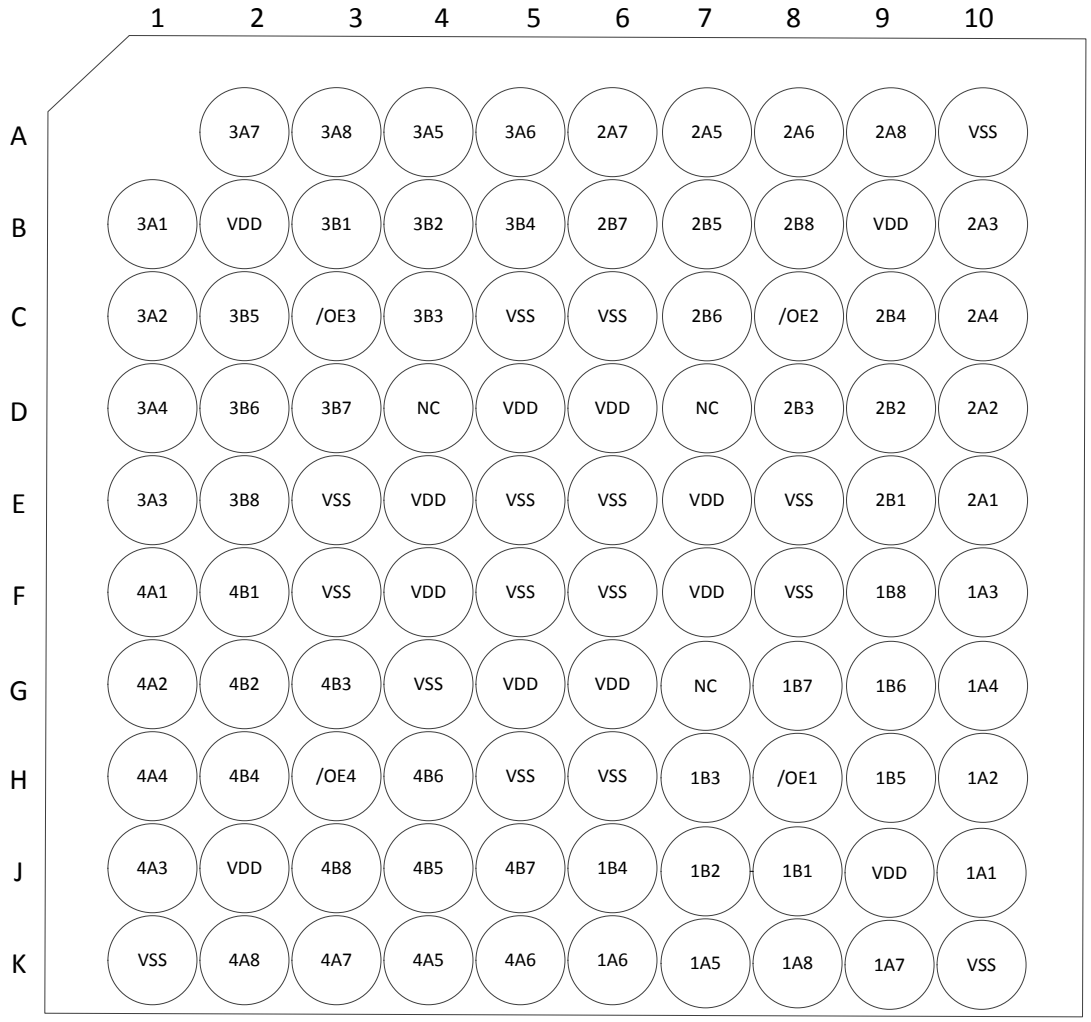


Figure 2. UT54BS32245 Pinout

PIN DESCRIPTION

Pin No.	Name	Description
A2, A3, A4, A5, A6, A7, A8, A9, B1, B10, C1, C10, D1, D10, E1, E10, F1, F10, G1, G10, H1, H10, J1, J10, K2, K3, K4, K5, K6, K7, K8, K9	nAn	Port A pins
B3, B4, B5, B6, B7, B8, C2, C4, C7, C9, D2, D3, D8, D9, E2, E9, F2, F9, G2, G3, G8, G9, H2, H4, H7, H9, J3, J4, J5, J6, J7, J8	nBn	Port B pins
C3, C8, H3, H8	/ENn	Active LOW enable pin
A10, D4, D7, C5, C6, E3, E5, E6, E8, F3, F5, F6, F8, G4, H5, H6, K1, K10	VSS	Ground Pin
B2, B9, D5, D6, E4, E7, F4, F7, G5, G6, G7, J2, J9	VDD	Supply Pin, +3.3V –or- +5.0V

TRUTH TABLE

INPUT (/EN)	Function
L	A port to B port -or- B port to A port
H	DISCONNECT

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Parameter	MIN	MAX	Unit
V_{DD}[2]	Positive Output Supply Voltage	-0.5	7.2	V
V_I[2]	Voltage on an Input pin during operation		V_{DD}+ 0.3V	V
I_{CCC}	Continuous DC Channel Current		65	mA
P_D[3]	Maximum package power dissipation permitted at T_C=125°C		1.6	W
T_J	Junction Temperature		+150	°C
Θ_{JC}	Thermal resistance, junction-to-case		15	°C/W
T_{STG}	Storage Temperature	-65	+150	°C
ESD	ESD protection (Human Body Model) Class 2		2000	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. All voltages referenced to VSS
3. Per MIL-STD-883, method 1012.1, section 3.4.1, PD=(Tj(max) - Tc(max)) / Θjc
4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	LIMIT	Unit
V_{DD}[1]	Positive Output Supply Voltage	3.0 to 3.6 or 4.5 to 5.5	V
V_{IN}[1]	Input Voltage on any pin	0.0 to V_{DD}	V
T_C	Case Temperature Range	-55 to +125	°C
t_R	Rise time	>5	ns
t_F	Fall time	>5	ns
I_{CCC}	Continuous DC Channel Current	60	mA

Notes:

1. All voltages referenced to VSS

OPERATIONAL ENVIROMENT

PARAMETER	LIMIT	UNITS
Total Ionizing Dose (TID)	3.0E5	rad(Si)
Single Event Latchup (SEL)	>100	MeV-cm^2/mg

DC CHARACTERISTICS[*,1]

(V_{DD}= 5.0V ± 0.5V, 3.3V ± 0.3V, -55°C < T_C < +125°C); Unless otherwise noted, Tc is per the temperature range ordered

Symbol	Parameter	Condition		MIN	MAX	Unit
V_{IH}	High level input voltage	V_{DD}=3.6V, 5.5V		0.7*V_{DD}		V
V_{IL}	Low level input voltage	V_{DD}=3.0V, 4.5V			0.3*V_{DD}	V
I_{ID}	Leakage current digital	V_{DD}= MAX; V_I = V_{DD} or V_{SS}		-1	1	µA
I_{IA}	Leakage current analog	V_{DD}= MAX; V_I = V_{DD} or V_{SS}		-3	3	µA
I_{DD}	Active Supply Current	V_{DD}=3.6V, 5.5V			0.5	mA/MHz
I_{DDQ}	Quiescent Supply Current	V_{DD}= MAX; I_O = 0mA; V_I = V_{DD} or V_{SS}			15	µA
C_I	Input Capacitance (/EN)	V_I = V_{DD} or VSS			5	pF
$C_{IO(OFF)}$	I/O Capacitance when device OFF	V_{DD} = MAX V_O = V_{DD} or VSS V_I = V_{DD}/2 /EN = V_{DD}			5	pF
$C_{IO(ON)}$	I/O Capacitance when device ON	V_{DD} = MAX V_O = open V_I = V_{DD}/2 /EN = 0V			16	pF
R_{ONL} [2,3]	Resistance through switch	V_{DD}= 4.5V V_I = VSS	I_O = 30mA I_O = 15mA		10 13	Ω
		V_{DD}= 3.0V V_I = VSS	I_O = 30mA I_O = 15mA		10 13	Ω
$R_{ON(Flat)}$ [1,2]	Switch On Resistance	V_{DD}=3.0V,4.5V V_I = V_{DD}			5 6	Ω
		V_{DD}=3.0V V_I = V_{DD}/2	I_O = -30mA I_O = -15mA		10 13	Ω

Symbol	Parameter	Condition		MIN	MAX	Unit
R_{ONH} [1,2]	Resistance through switch	V_{DD}=4.5V $V_I = V_{DD}$	I_O = -30mA I_O = -15mA		10 13	Ω
		V_{DD}= 3.0V $V_I = V_{DD}$	I_O = -30mA I_O = -15mA		10 13	Ω
$R_{ON(Flat)}$ [1,2]	Switch On Resistance	V_{DD}=3.0V,4.5V $V_I = V_{DD}$	I_O = -30mA I_O = -15mA		5 6	Ω

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.
2. Guaranteed by design.

AC CHARACTERISTICS *,1

(V_{DD}= 5.0V ±0.5V, -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	From (INPUT)	To (OUTPUT)	Cond.	MIN	MAX	Unit
t_{PD30} [1]	A or B	B or A	I_I =+/-30mA		500	ps
t_{PD15} [1]	A or B	B or A	I_I =+/-15mA		650	ps
t_{EN}	/EN=V_{SS}	A or B		1	5	ns
t_{DIS}	/EN=V_{DD}	A or B		1	6	ns

(V_{DD}= 3.3V ±0.3V, -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	From (INPUT)	To (OUTPUT)	Cond.	MIN	MAX	Unit
t_{PD30} [1]	A or B	B or A	I_I =+/-30mA		1	ns
t_{PD15} [1]	A or B	B or A	I_I =+/-15mA		1.3	ns
t_{EN}	/EN=V_{SS}	A or B		2	6	ns
t_{DIS}	/EN=V_{DD}	A or B		1	7	ns

Notes:

***** For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. The propagation delay through the channel is based upon the RC time constant of the channel resistance and switch ON capacitance, 11 Ω and 17pF.

Symbol	Parameter	Condition	MIN	MAX	Unit
X_{TALK} [1]	Cross talk between channels V_{DD} = 5.0V	RL = 50Ω, CL = 50pF, f = 1MHz, V_{IN1} = $1V_{RMS}$ Centered at $V_{DD}/2$		-60	dB
X_{TALK} [1]	Cross talk between channels V_{DD} = 3.3V	RL = 50Ω, CL = 50pF, f = 1MHz, V_{IN1} = $1V_{RMS}$ Centered at $V_{DD}/2$		-60	dB
I_{SOOFF} [1]	Off Isolation	RL = 50Ω, CL = 50pF, f = 1MHz, V_{IN1} = $1V_{RMS}$ Centered at $V_{DD}/2$		-60	dB

Notes:

1. Guaranteed by design.

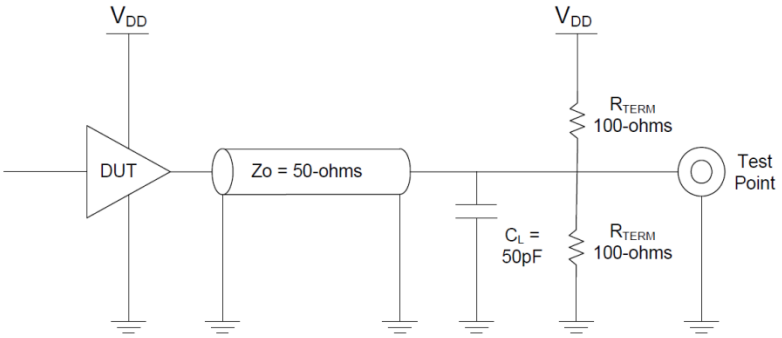


Figure 3. Output Test Load Circuit

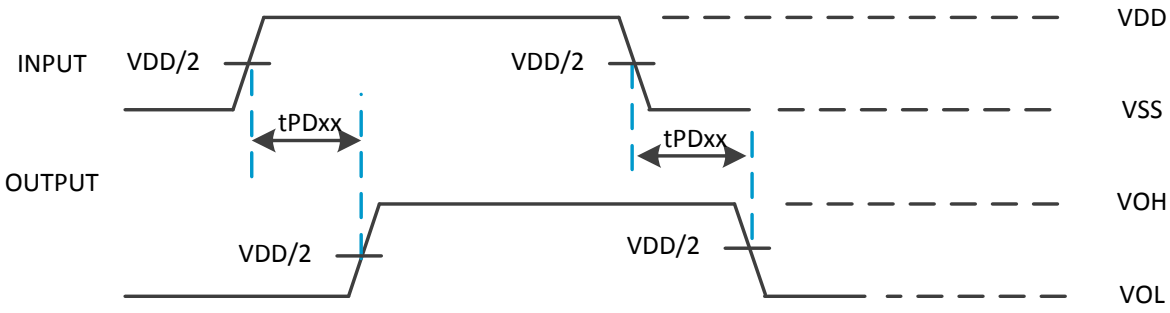


Figure 4. Propagation Waveform

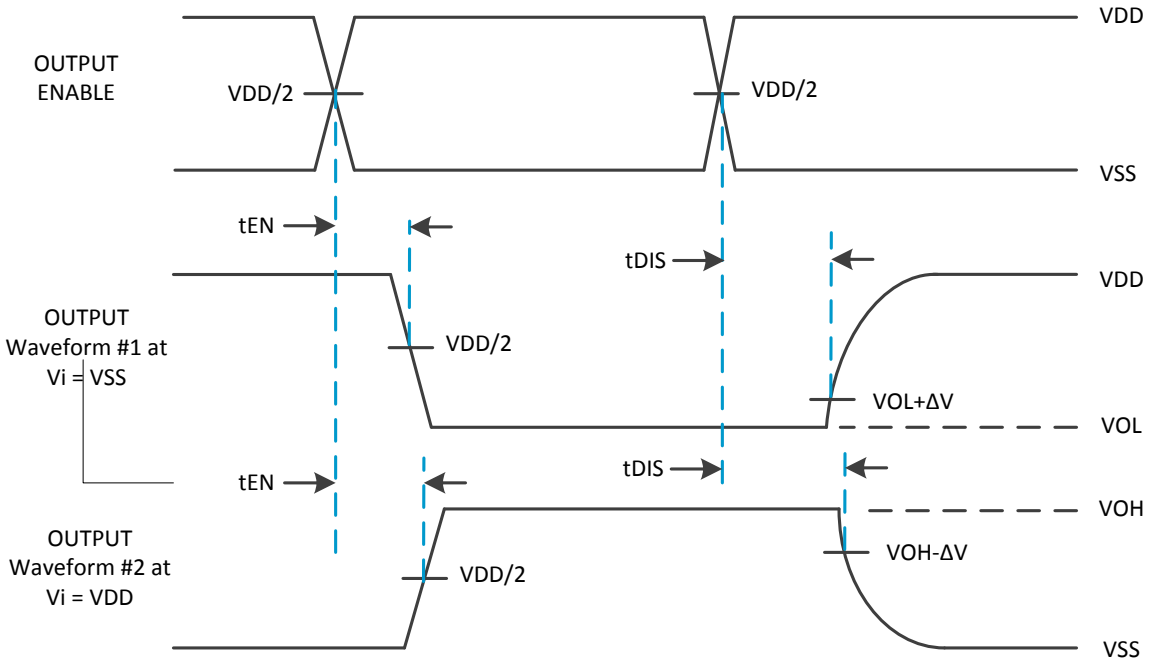


Figure 5. Propagation Waveform

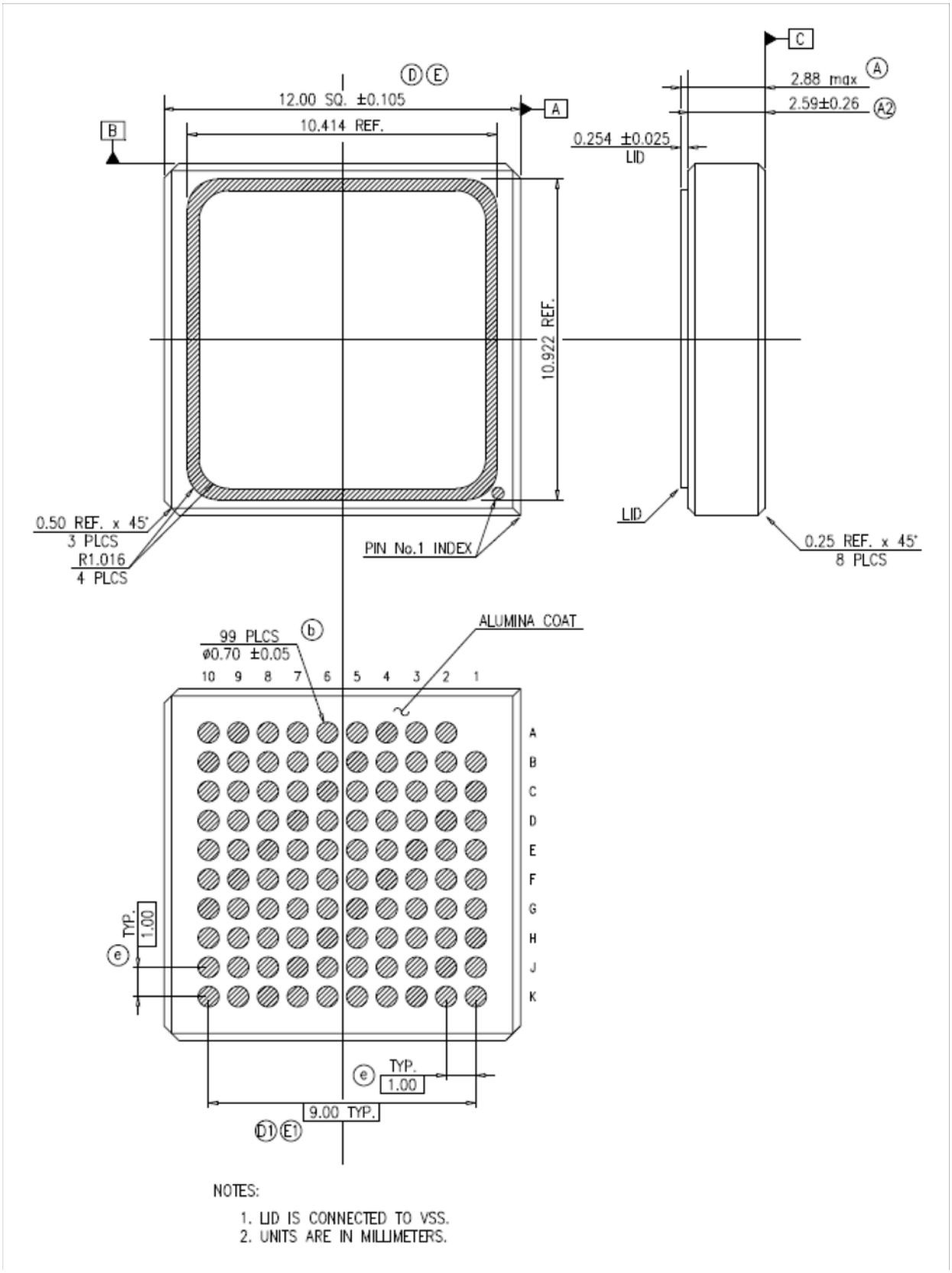
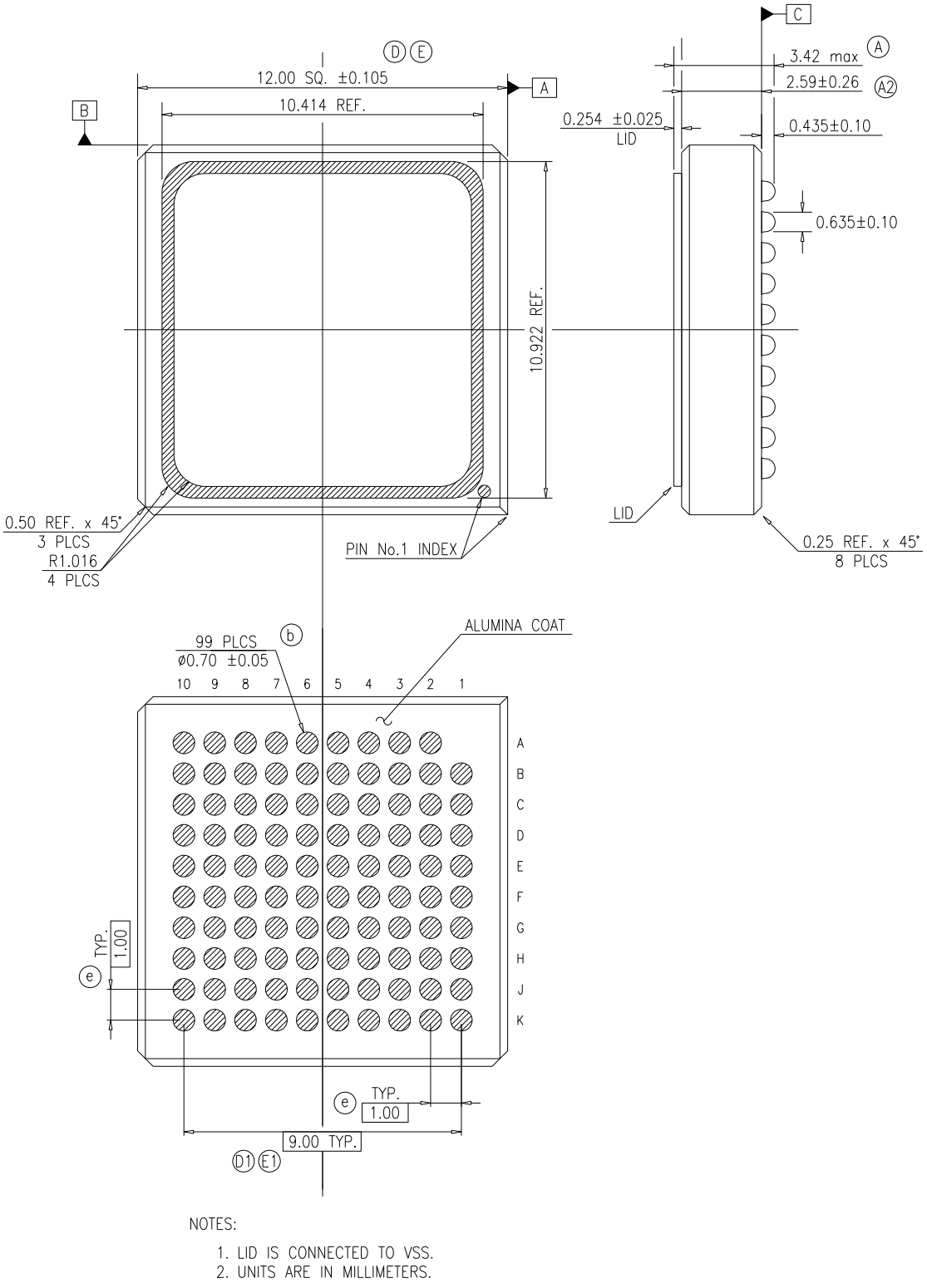


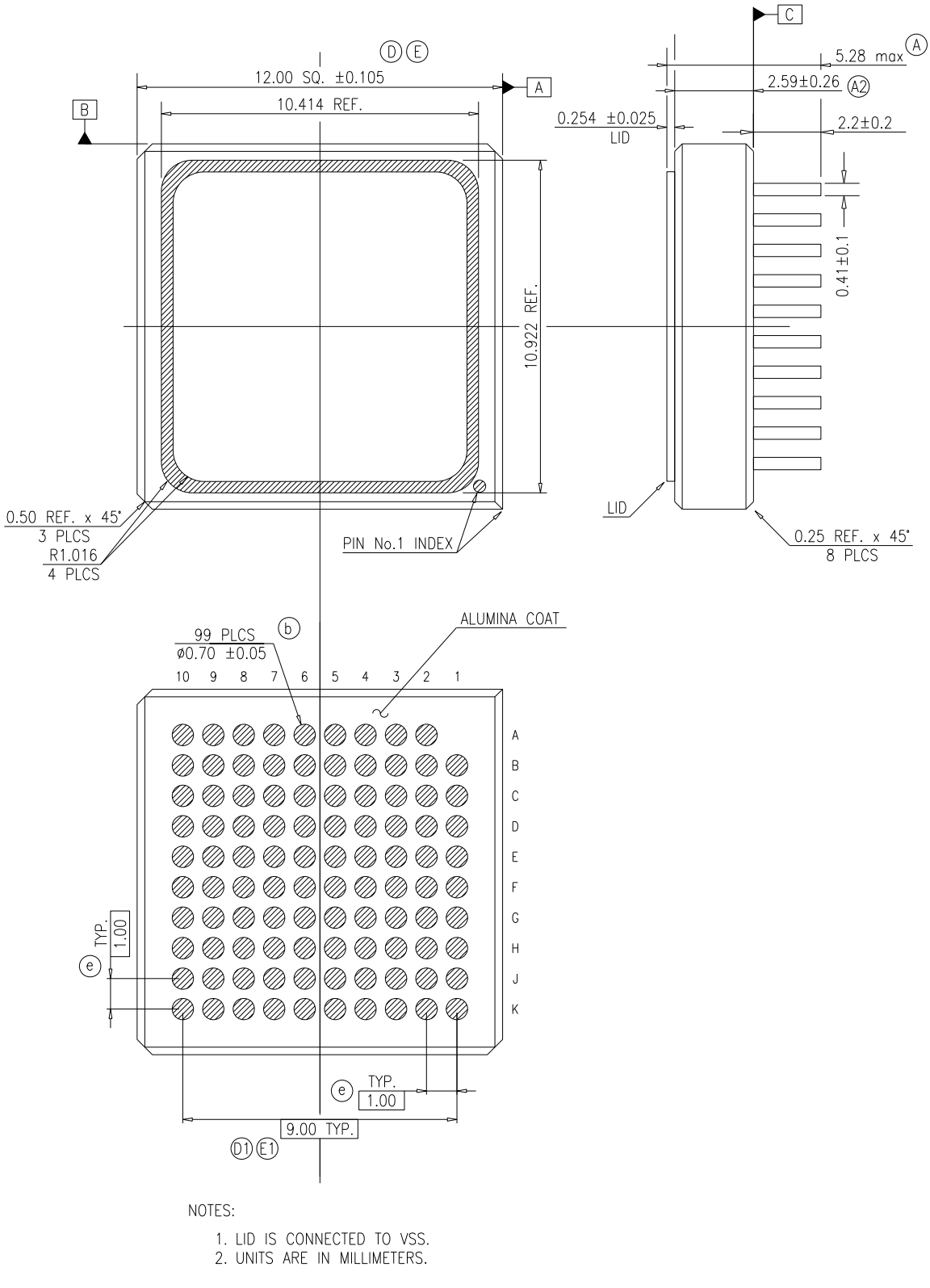
Figure 6. 99-Lead CLGA



NOTES:

1. LID IS CONNECTED TO VSS.
2. UNITS ARE IN MILLIMETERS.

Figure 7. 99 Lead CBGA



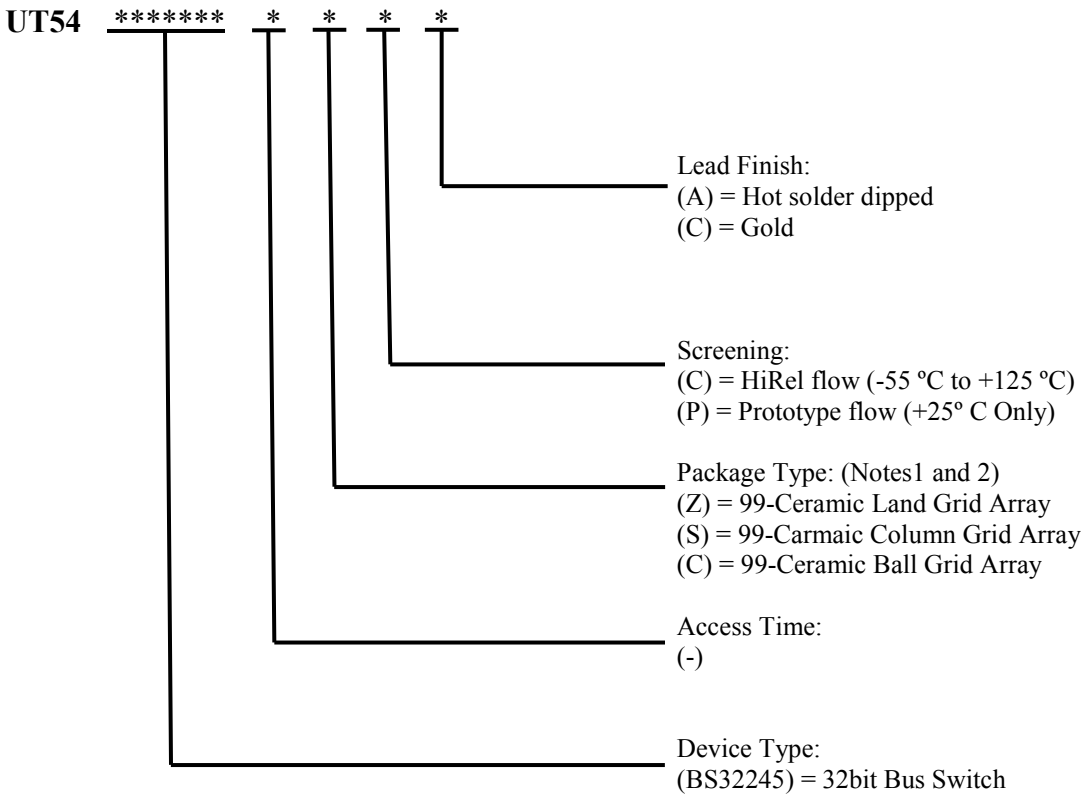
NOTES:

1. LID IS CONNECTED TO VSS.
2. UNITS ARE IN MILLIMETERS.

Figure 8. 99 Lead CCGA

ORDERING INFORMATION

UT54BS32245 32bit Bus Switch Analog:



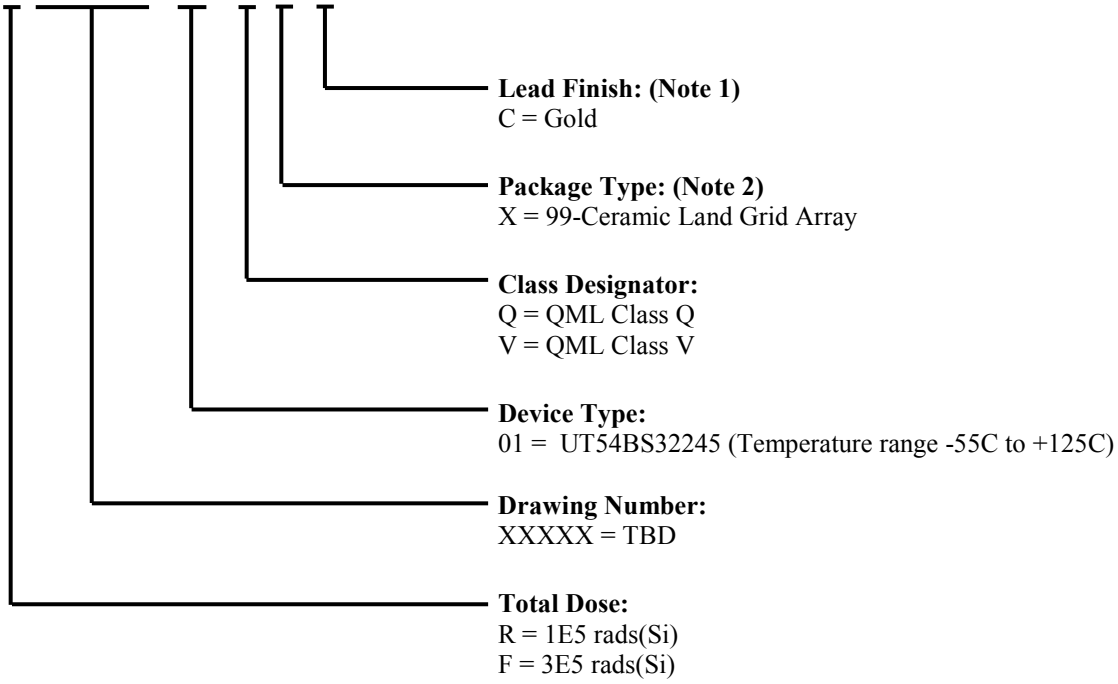
Notes:

1. Prototype flow per Aeroflex Manufacturing Flows Document. Tested at 25 º C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
2. HiRel Temperature Range flow per Aeroflex Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

Package Option	Associated Lead Finish
(Z) 99-CLGA	(C) Gold
(S) 99-CCGA	(A) Hot Solder Dipped
(C) 99-CBGA	(A) Hot Solder Dipped

UT54BS32245 Bus Switch Analog SMD:

5962 – XXXXX ** * * *



Notes:

1. Lead finish is "C" (gold) only.
2. Aeroflex offer Column Attachment as an additional service for the Ceramic Grid Array (Case outline "S." If needed, please ask for COLUMN ATTACHMENT when submitting your request for quotation.

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi – Rel

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