

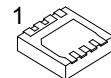


-40A, -20V P-CHANNEL POWER MOSFET

■ DESCRIPTION

The UTC **UT7407** is a P-channel Power Mosfet, it uses UTC's advanced technology to provide the customers with a minimum on state resistance, etc.

The UTC **UT7407** is suitable for load switch and battery protection applications.

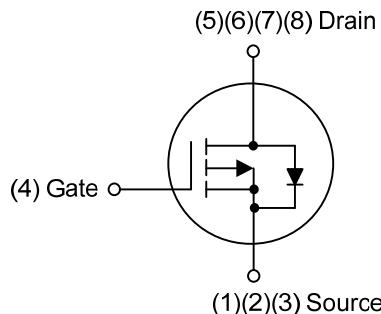


PDFN3x3

■ FEATURES

- * $R_{DS(ON)} \leq 9.5 \text{ m}\Omega @ V_{GS}=-4.5V, I_D=-14A$
- $R_{DS(ON)} \leq 15.5 \text{ m}\Omega @ V_{GS}=-2.5V, I_D=-13A$
- $R_{DS(ON)} \leq 20 \text{ m}\Omega @ V_{GS}=-1.8V, I_D=-11A$
- * Low thermal resistance

■ SYMBOL



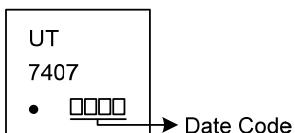
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT7407L-P3030-R	UT7407G-P3030-R	PDFN3x3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT7407G-P3030-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P3030: PDFN3x3 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	RATINGS	UNIT	
Drain-Source Voltage	V_{DSS}	-20	V	
Gate-Source Voltage	V_{GSS}	± 8	V	
Continuous Drain Current ($T_A=25^\circ\text{C}$)	I_D	-14	A	
Continuous Drain Current	I_D	-40	A	
Pulsed Drain Current (Note 2)	I_{DM}	-80	A	
Avalanche Energy $L=0.1\text{mH}$ (Note 3)	E_{AS}	96	mJ	
Power Dissipation	$T_c=25^\circ\text{C}$	P_D	28	W
Junction Temperature		T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = -43.8\text{A}$, $V_{DD} = -20\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	60	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	4.46	$^\circ\text{C}/\text{W}$

Notes: 1. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

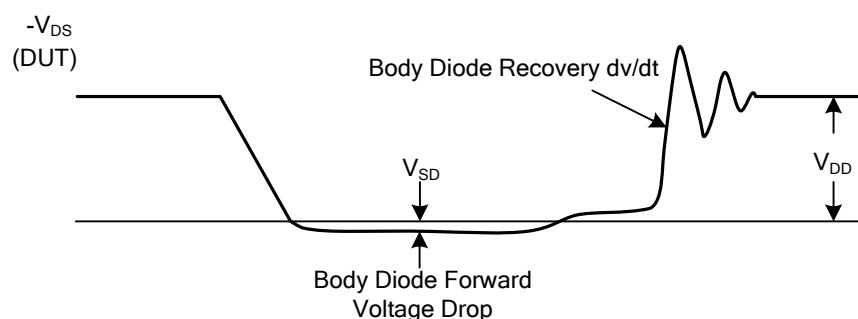
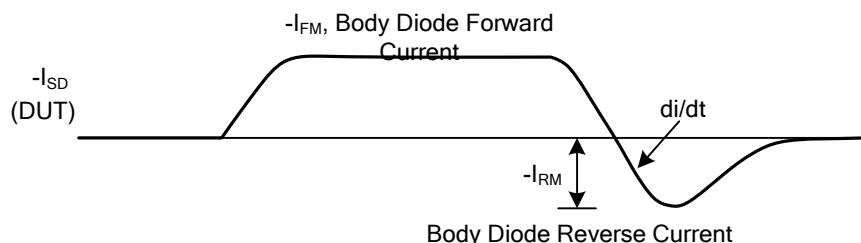
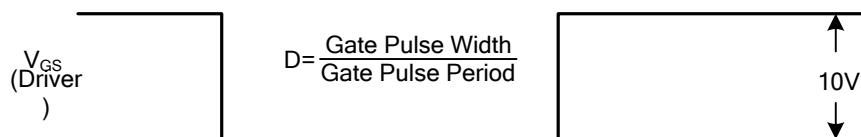
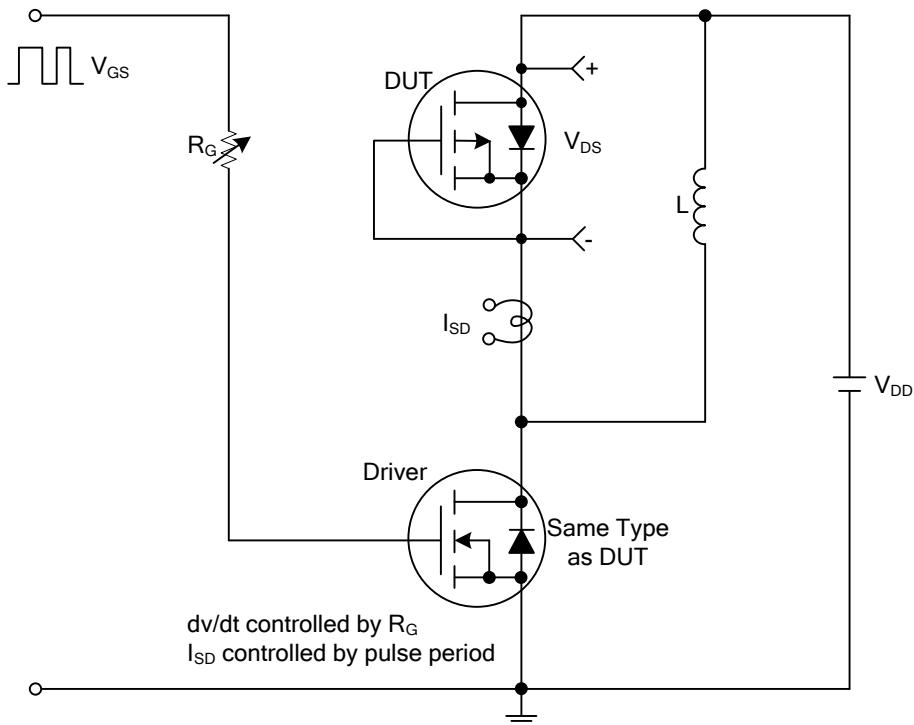
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$			-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 8\text{V}$, $V_{DS}=0\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-0.3		-0.9	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5\text{V}$, $I_D=-14\text{A}$			9.5	$\text{m}\Omega$
		$V_{GS}=-2.5\text{V}$, $I_D=-13\text{A}$			15.5	$\text{m}\Omega$
		$V_{GS}=-1.8\text{V}$, $I_D=-11\text{A}$			20	$\text{m}\Omega$
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=-10\text{V}$, $f=1.0\text{MHz}$		3830		pF
Output Capacitance	C_{OSS}			840		pF
Reverse Transfer Capacitance	C_{RSS}			725		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=-4.5\text{V}$, $V_{DS}=-16\text{V}$, $I_D=-40\text{A}$		37		nC
Gate to Source Charge	Q_{GS}			4.5		nC
Gate to Drain Charge	Q_{GD}			11.5		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=-10\text{V}$, $V_{GS}=-4.5\text{V}$, $I_D=-40\text{A}$, $R_G=3\Omega$ (Note 1, 2)		14		ns
Rise Time	t_R			23		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			150		ns
Fall-Time	t_F			135		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current (Note)	I_S				-40	A
Maximum Body-Diode Pulsed Current	I_{SM}				-80	A
Diode Forward Voltage	V_{SD}	$I_S=-1.0\text{A}$, $V_{GS}=0\text{V}$			-1.2	V

Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

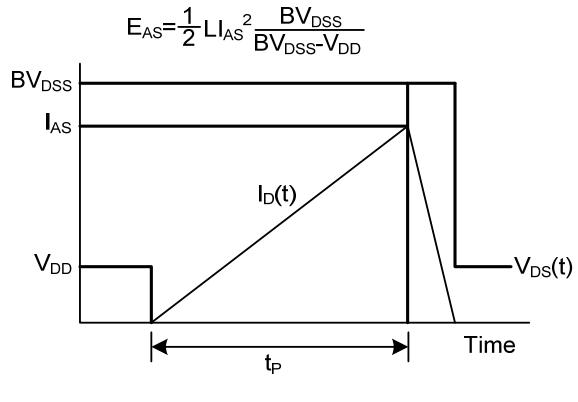
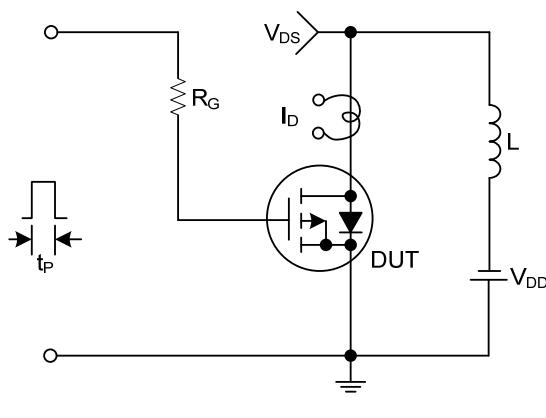
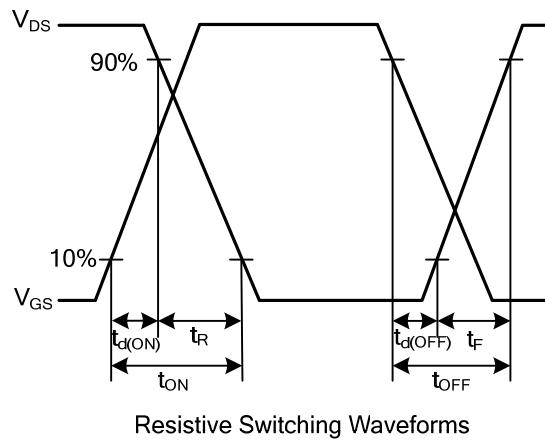
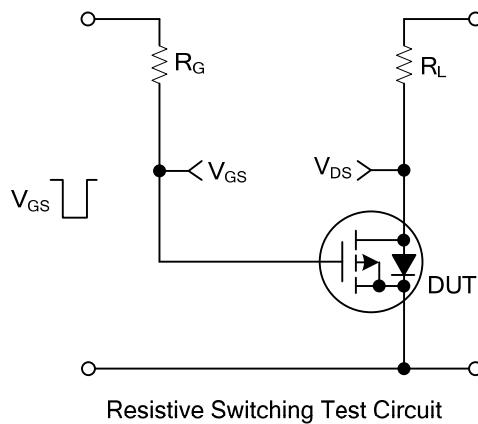
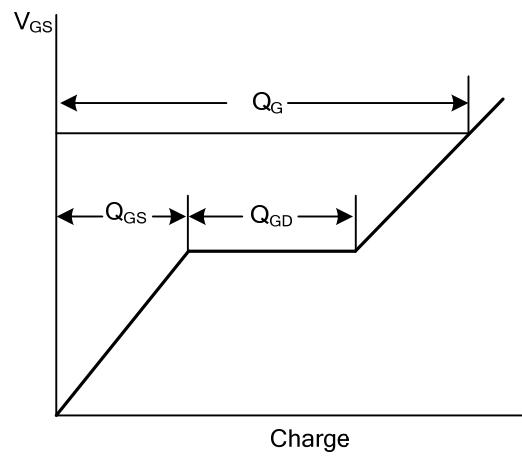
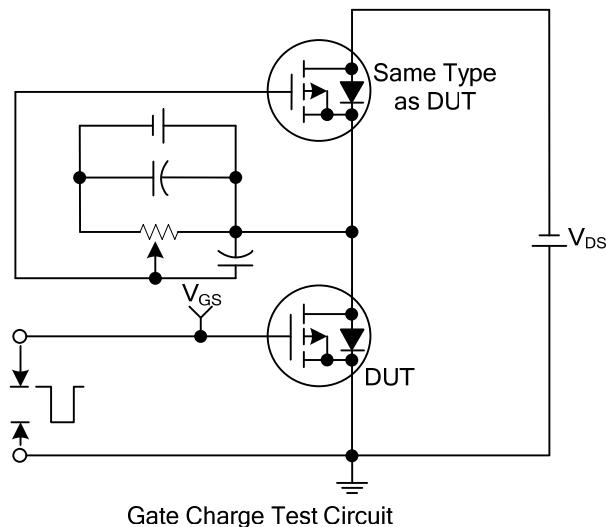
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit and Waveforms

■ TEST CIRCUITS AND WAVEFORMS



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