



## UT75N10H

Preliminary

Power MOSFET

### 75A, 100V N-CHANNEL POWER MOSFET

#### DESCRIPTION

The UTC **UT75N10H** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance, low gate charge and high switching speed.

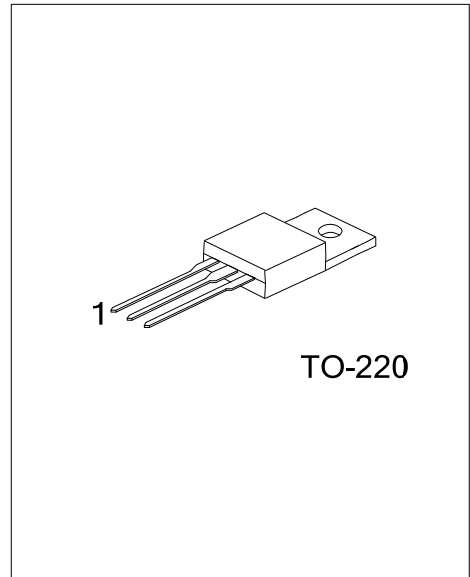
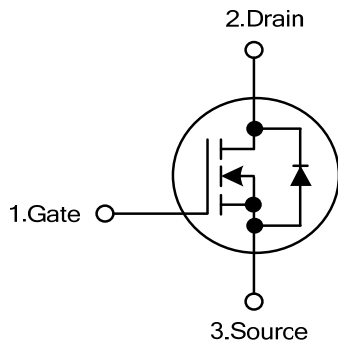
The UTC **UT75N10H** is suitable for high voltage synchronous rectifier and DC/DC converters, etc.

#### FEATURES

\*  $R_{DS(ON)} \leq 14 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=37.5\text{A}$

\* High Switching Speed

#### SYMBOL



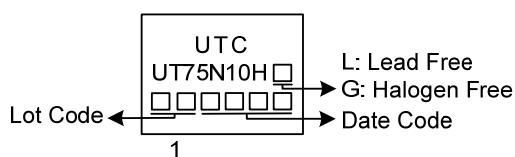
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT75N10HL-TA3-T	UT75N10HG-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: Source G: Gate D: Drain

<p>UT75N10HG-TA3-T</p>	<p>(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	100	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Drain Current	Continuous ( $V_{GS}=10\text{V}$ ) $T_C=25^{\circ}\text{C}$	$I_D$	75	A
	Pulsed	$I_{DM}$	150	A
Avalanche Energy (Note 3)	Single Pulsed	$E_{AS}$	63	mJ
Peak Diode Recovery $dv/dt$ (Note 4)		$dv/dt$	3.4	V/ns
Power Dissipation		$P_D$	142	W
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3.  $L=0.1\text{mH}$ ,  $I_{AS}=35.7\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^{\circ}\text{C}$ .

4.  $I_{SD}\leq 30\text{A}$ ,  $di/dt\leq 200\text{A}/\mu\text{s}$ ,  $V_{DD}\leq BV_{DSS}$ , Starting  $T_J=25^{\circ}\text{C}$ .

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	$\theta_{JA}$	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	0.88	$^{\circ}\text{C}/\text{W}$

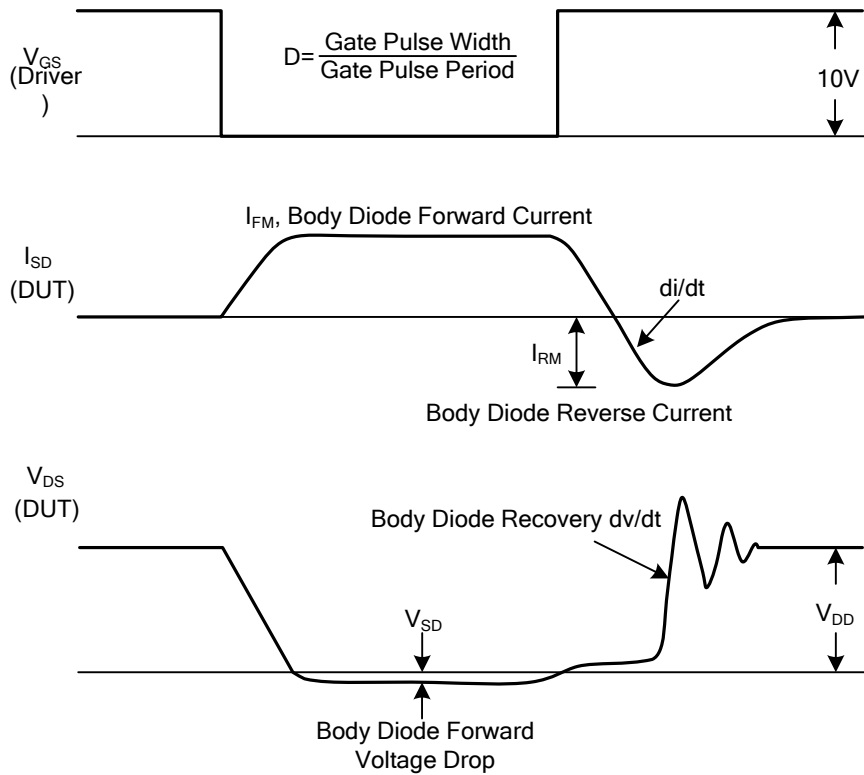
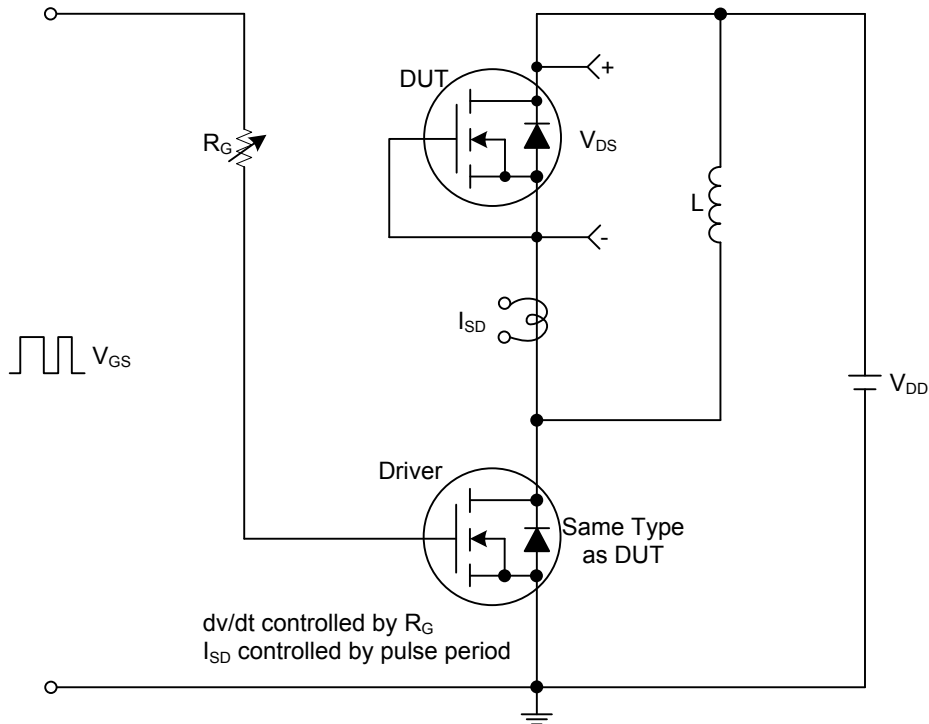
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	100			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=100\text{V}$ , $V_{GS}=0\text{V}$			1	$\mu\text{A}$
Gate- Source Leakage Current	Forward	$I_{GSS}$ $V_{GS}=+20\text{V}$ , $V_{DS}=0\text{V}$ $V_{GS}=-20\text{V}$ , $V_{DS}=0\text{V}$			+100	nA
	Reverse				-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=37.5\text{A}$			14	m $\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{MHz}$		4400		pF
Output Capacitance	$C_{OSS}$			286		pF
Reverse Transfer Capacitance	$C_{RSS}$			240		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge at 10V	$Q_G$	$V_{DS}=80\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=75\text{A}$ , $I_G=1\text{mA}$ (Note 1, 2)		115		nC
Gate to Source Charge	$Q_{GS}$			21		nC
Gate to Drain Charge	$Q_{GD}$			42		nC
Turn-ON Time	$t_{ON}$	$V_{DD}=50\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=75\text{A}$ , $R_G=3.3\Omega$ (Note 1, 2)		21		ns
Turn-ON Delay Time	$t_{D(ON)}$			20		ns
Rise Time	$t_R$			58		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			24		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				75	A
Continuous Drain-Source Current	$I_{SD}$				150	A
Drain-Source Diode Forward Voltage	$V_{SD}$	$I_S=75\text{A}$ , $V_{GS}=0\text{V}$			1.4	V
Reverse Recovery Time	$t_{rr}$	$I_F=30\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$		46		ns
Reverse Recovery Charge	$Q_{rr}$			63		nC

Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

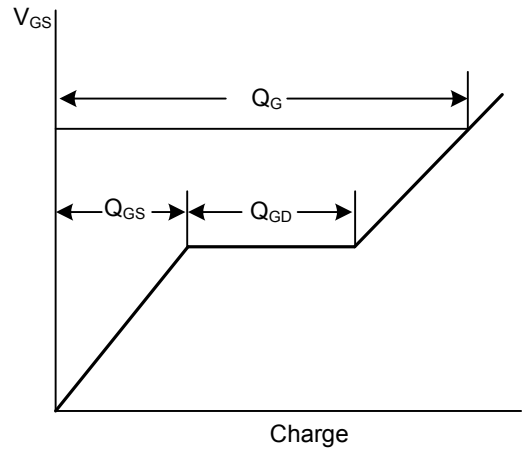
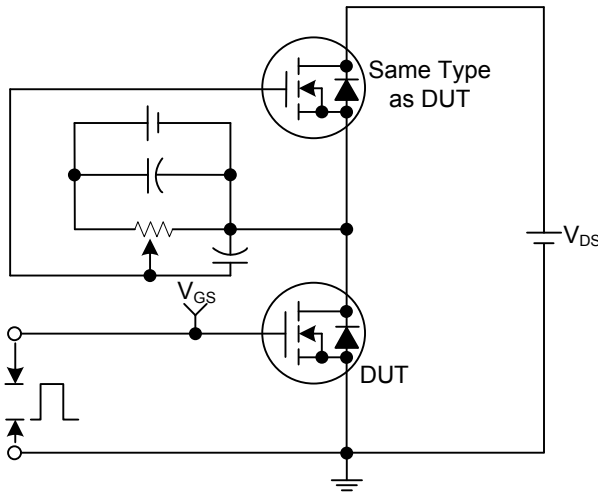
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



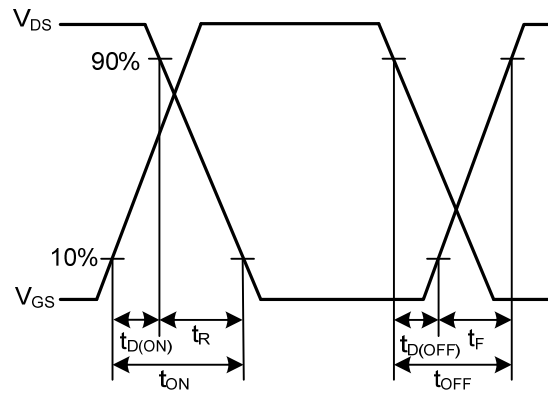
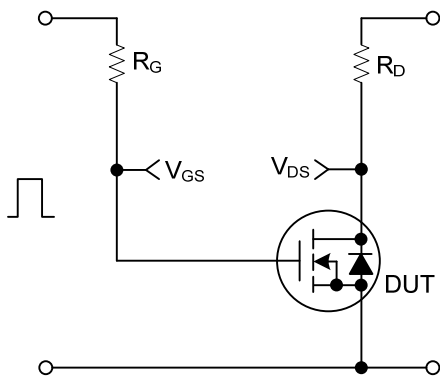
Peak Diode Recovery dv/dt Test Circuit and Waveforms

■ TEST CIRCUITS AND WAVEFORMS



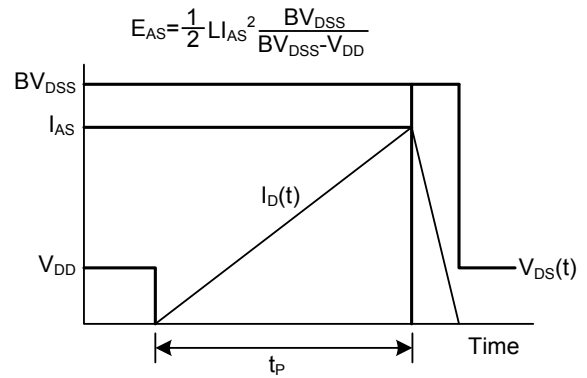
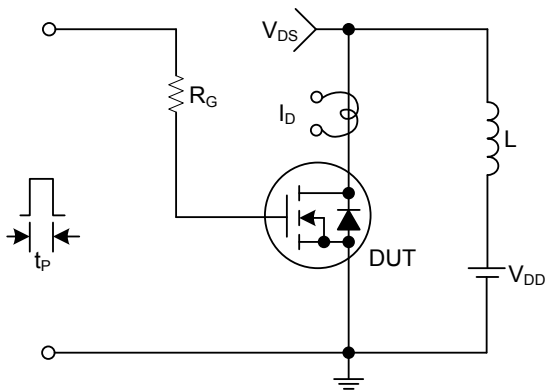
Gate Charge Test Circuit

Gate Charge Waveforms



Resistive Switching Test Circuit

Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

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