Standard Products

UT8ER512K32 Monolithic 16M SRAM

Data Sheet

July 24, 2012
www.aeroflex.com/memories

FEATURES

- 20ns Read, 10ns Write maximum access times
- Functionally compatible with traditional 512K x 32 SRAM devices
- CMOS compatible input and output levels, three-state bidirectional data bus
  - I/O Voltage 3.3 volt, 1.8 volt core
- Operational environment:
  - Total-dose: 100 krad(Si)
  - SEL Immune: $\leq$111MeV-cm^2/mg
  - SEU error rate = 8.1x10^{-16} errors/bit-day assuming geosynchronous orbit, Adam's 90% worst environment, and 6600ns default Scrub Rate Period (=97% SRAM availability)
- Packaging options:
  - 68-lead ceramic quad flatpack (6.898 grams)
- Standard Microcircuit Drawing 5962-06261
  - QML Q & V

INTRODUCTION

The UT8ER512K32 is a high-performance CMOS static RAM organized as 524,288 words by 32 bits. Easy memory expansion is provided by active LOW and HIGH chip enables ($\overline{E1}$, E2), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to the device is accomplished by driving chip enable one ($\overline{E1}$) input LOW, chip enable two (E2) HIGH and write enable ($\overline{W}$) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by taking chip enable one ($\overline{E1}$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$) and chip enable two (E2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ($\overline{E1}$ HIGH or E2 LOW), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E1}$ LOW, E2 HIGH and $\overline{W}$ LOW).

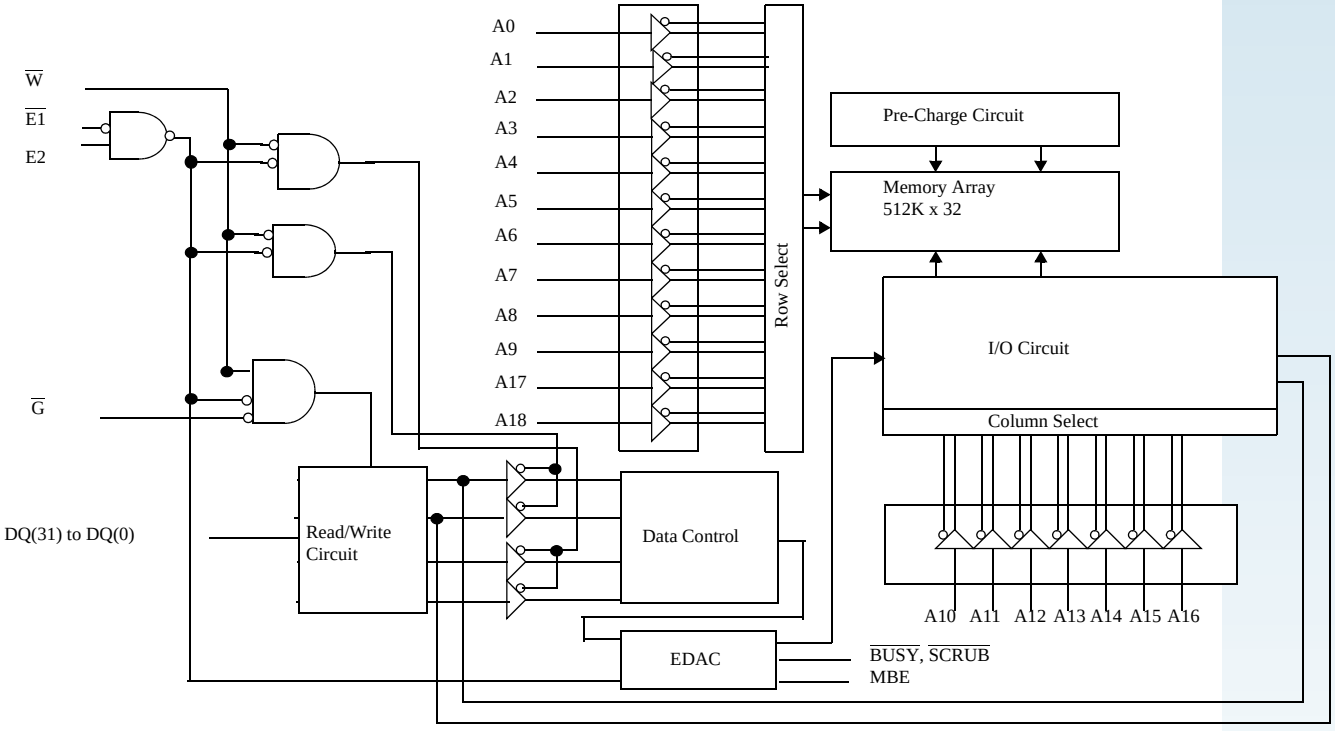


Figure 1. UT8ER512K32 SRAM Block Diagram

UT8ER512K32 Master or Slave Options

To reduce the bit error rates, the UT8ER512K32 employs an embedded EDAC (error detection and correction) with user programmable auto scrubbing options. The UT8ER512K32 device automatically corrects single bit word errors in event of an upset. During a read operation, if a multiple bit error occurs in a word, the UT8ER512K32 asserts the MBE (multiple bit error) output to notify the host.

The UT8ER512K32 is offered in two options: Master (UT8ER512K32M) or Slave (UT8ER512K32S). The master is a full function device which features user defined autonomous EDAC scrubbing options. The slave device employs a scrub on demand feature.

The UT8ER512K32M (master) and UT8ER512K32S (slave) device pins $\overline{\text{SCRUB}}$ and $\overline{\text{BUSY}}$ are physically different. The $\overline{\text{SCRUB}}$ pin is an output on master devices, but an input on slave devices. The master $\overline{\text{SCRUB}}$ pin asserts low when a scrub cycle initiates, and can be used to demand scrub cycles from multiple slave units when connected to the $\overline{\text{SCRUB}}$ input of slave(s). The $\overline{\text{BUSY}}$ pin is an output for the master device and can be used to generate wait states by the memory controller. The $\overline{\text{BUSY}}$ pin is a no connect (NC) for slave units.

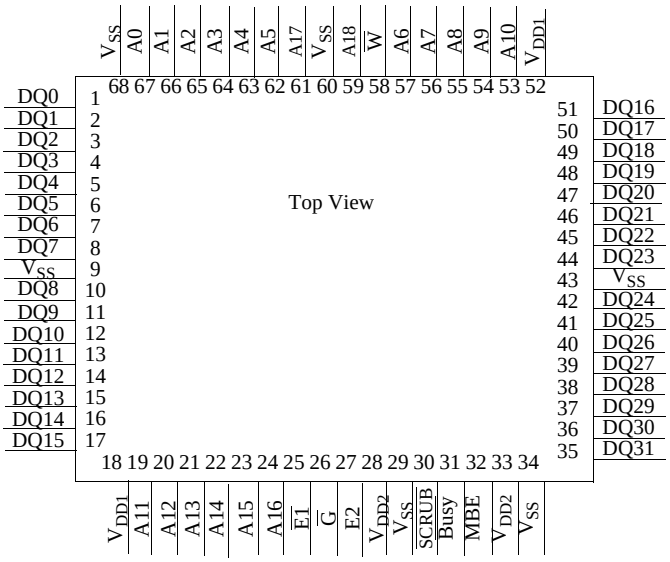


Figure 2. 20ns SRAM Pinout (68)

Note: Pin 31 on the UT8ER512K32S (Slave) is a no connect (NC).

PIN DESCRIPTIONS

Pins	Type	Description
A(18:0)	I	Address
DQ(31:0)	BI	Data Input/Output
$\overline{\text{E1}}$	I	Enable (Active Low)
E2	I	Enable (Active High)
$\overline{\text{W}}$	I	Write Enable
$\overline{\text{G}}$	I	Output Enable
V_{DD1}	P	Power (1.8)
V_{DD2}	P	Power (3.3V)
V_{SS}	P	Ground
MBE	BI	Multiple Bit Error
$\overline{\text{SCRUB}}$	I	Slave SCRUB Input
$\overline{\text{SCRUB}}$	O	Master SCRUB Output
$\overline{\text{BUSY}}$	NC	Slave No Connect
$\overline{\text{BUSY}}$	O	Master Wait State Control

DEVICE OPERATION

The UT8ER512K32 has four control inputs called Enable 1 ($\overline{\text{E1}}$), Enable 2 (E2), Write Enable ($\overline{\text{W}}$), and Output Enable ($\overline{\text{G}}$); 19 address inputs, A(18:0); and 32 bidirectional data lines, DQ(31:0). $\overline{\text{E1}}$ and E2 device enables control device selection, active, and standby modes. Asserting $\overline{\text{E1}}$ and E2 enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. $\overline{\text{W}}$ controls read and write operations. During a read cycle, $\overline{\text{G}}$ must be asserted to enable the outputs.

Table 1. SRAM Device Control Operation Truth Table

$\overline{\text{G}}$	$\overline{\text{W}}$	E2	$\overline{\text{E1}}$	I/O Mode	Mode
X	X	X	H	DQ(31:0) 3-State	Standby
X	X	L	X	DQ(31:0) 3-State	Standby
L	H	H	L	DQ(31:0) Data Out	Word Read
H	H	H	L	DQ(31:0) All 3-State	Word Read[2]
X	L	H	L	DQ(31:0) Data In	Word Write

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

Table 2. EDAC Control Pin Operation Truth Table

MBE	$\overline{\text{SCRUB}}$	$\overline{\text{BUSY}}$	I/O Mode	Mode
H	H	H	Read	Uncorrectable Multiple Bit Error
L	H	H	Read	Valid Data Out
X	H	H	X	Device Ready
X	H	L	X	Device Ready / Scrub Request Pending
X	L	X	Not Accessible	Device Busy

Notes:
1. "X" is defined as a "don't care" condition
2. $\overline{\text{Busy}}$ signal is a "NC" for UT8ER512K32S slave device and is an "X" don't care.

READ CYCLE

A combination of $\overline{W}$ and E2 greater than V_{IH} (min) and $\overline{E1}$ and $\overline{G}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs while $\overline{E1}$ and E2 are asserted, $\overline{G}$ is asserted, and $\overline{W}$ is deasserted. Valid data appears on data outputs DQ(31:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by the latter of either $\overline{E1}$and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 32-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} (reference Figure 3b) have not been satisfied.

SRAM EDAC Status Indications during a Read Cycle, if MBE is Low, the data is good. If MBE is High the data is corrupted (reference Table 2).

WRITE CYCLE

A combination of $\overline{W}$ and $\overline{E1}$ less than V_{IL}(max), and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E1}$ and E2. To avoid bus contention t_{WLQZ} must be satisfied before data is applied to the 32 bidirectional pins DQ(31:0) unless the outputs have been previously placed in high impedance state by deasserting $\overline{G}$.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by either $\overline{E1}$or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the thirty-two bidirectional pins DQ(31:0) to avoid bus contention.

CONTROL REGISTER WRITE/READ CYCLES

Configuration options can be selected by writing to the control register. The configuration table (Table 4) details the programming options. The control register is accessed by applying a series of values to the address bus as shown in Figure 6a. The contents of the control register are written following the fifth address. The contents of the address bus are written to the control register if bit 9 is zero. The contents of the control register are output to the data bus if bit 9 is one. **NOTE:** MBE must be driven high by the user for both a write or a read of the control register.

MEMORY SCRUBBING/CYCLE STEALING

The UT8ER512K32 SRAM uses architectural improvements and embedded error detection and correction to maintain unsurpassed levels of error protection. This is accomplished by what Aeroflex refers to as Cycle Stealing. To minimize the system design impact on the speed of operation, the edge relationship between $\overline{BUSY}$ and $\overline{SCRUB}$ is programmable via the sequence described in figure 6a.

The effective error rate is a function of the intrinsic rate and the environment. As a result, some users may desire an increased scrub rate to lower the error rate at the sacrifice of reduced total throughput, while others may desire a lower scrub rate to

increase the total throughput and accept a higher error rate. This rate at which the SRAM controller will correct errors from the memory is user programmable. The required sequence is described in figure 6a.

A master mode scrub cycle will occur at the user defined Scrub Rate Period. A scrub cycle is defined as the verification and correction (if necessary) of data for a single word address location. Address locations are scrubbed sequentially every Scrub Rate Period (t_{SCRT}). Scrub cycles will occur at every Scrub Rate Period regardless of the status of control pins. Control pin function will be returned upon deassertion of $\overline{BUSY}$ pin. The Slave mode scrub cycle occurs anytime the $\overline{SCRUB}$ pin is asserted. The scrub cycle is defined the same as the master mode, and will occur regardless of control pin status. Control pin function will be returned upon $\overline{SCRUB}$ deassertion.

Data is not only corrected during the internal scrub, but again during a user requested read cycle. If the data presented contains two or more errors after t_{AVAV} is satisfied, the MBE signal will be asserted. (Note: Reading un-initialized memory locations may result in un-intended MBE assertions.)

Operational Environment

The UT8ER512K32 SRAM incorporates special design, layout, and process features which allows operation in a limited environment.

Table 3. Operational Environment Design Specifications[1]

Total Dose	100K	rad(Si)
Heavy Ion Error Rate[2]	$8.1x10^{-16}$	Errors/Bit-Day

Notes:

1. The SRAM is immune to latchup to particles $\leq$111MeV-cm^2/mg.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum and default EDAC scrub rate.

SUPPLY SEQUENCING

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

POWER-UP REQUIREMENTS

During power-up of the UT8ER512K32 device, the power supply voltages will transverse through voltage ranges where the device is not guaranteed to operate before reaching final levels. Since some circuits on the device will start to operate at lower voltage levels than others, the device may power-up in an unknown state. To eliminate this with most power-up situations, the device employs an on-chip power-on-reset (POR) circuit. The POR, however, requires time to complete the operation. Therefore, it is recommended that all device activity be delayed by a minimum of 100ms, after both V_{DD1} and V_{DD2} supplies have reached their respective minimum operating voltage.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage (Core)	-0.3 to 2.1V
V_{DD2}	DC supply voltage (I/O)	-0.3 to 3.8V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8V
T_{STG}	Storage temperature	-65 to +150°C
P_D[2]	Maximum package power dissipation permitted @ Tc = +125°C	5W
T_J	Maximum junction temperature	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[2]	5°C/W
I_I	DC input current	±10 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Per MIL-STD-883, Method 1012, Section 3.4.1, $P_D = \frac{(T_{JC}(max) - Tc\ (max))}{\Theta_{JC}}$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage (Core)	1.7 to 1.9V[1]
V_{DD2}	DC supply voltage (I/O)	3.0 to 3.6V
T_C	Case temperature range	(C) Screening: -55 to +125°C (W) Screening: -40 to +125°C
V_{IN}	DC input voltage	0V to V_{DD2}

Notes:

1. For increased noise immunity, supply voltage V_{DD1} can be increased to 2.0V. All characteristics contained herein are guaranteed by characterization at V_{DD1} = 2.0Vdc unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*

(Tc = -55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening) (V_{DD1} = 1.7V to 1.9V; V_{DD2} = 3.0V to 3.6V)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage		0.7*V_{DD2}		V
V_{IL}	Low-level input voltage			0.3*V_{DD2}	V
V_{OL}[1]	Low-level output voltage	I_{OL} = 8mA, V_{DD2} = V_{DD2} (min)		0.2*V_{DD2}	V
V_{OH}	High-level output voltage	I_{OH} = -4mA, V_{DD2} = V_{DD2} (min)	0.8*V_{DD2}		V
C_{IN}[2]	Input capacitance	*f* = 1MHz @ 0V		12	pF
C_{IO}[2]	Bidirectional I/O capacitance	*f* = 1MHz @ 0V		12	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD2} and V_{SS}	-2	2	µA
I_{OZ}[3]	Three-state output leakage current	V_O = V_{DD2} and V_{SS} V_{DD2} = V_{DD2} (max), $\overline{G}$ = V_{DD2} (max)	-2	2	µA
I_{OS}[4, 5]	Short-circuit output current	V_{DD2} = V_{DD2} (max), V_O = V_{DD2} V_{DD2} = V_{DD2} (max), V_O = V_{SS}	-100	+100	mA
$I_{DD1}(OP_1$[6,7,8])	V_{DD1} Supply current operating @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 4).	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0, V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max) — -55°C and 25°C		25	mA
		V_{DD1} = 2.0V, 125°C		70	mA
		V_{DD1} = 1.9V, 125°C		65	mA
$I_{DD1}(OP_2$[6,7,8])	V_{DD1} Supply current operating @ 50MHz, EDAC enabled @ default Scrub Rate Period (see table 4).	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0, V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max) — -55°C and 25°C		250	mA
		V_{DD1} = 2.0V, 125°C		300	mA
		V_{DD1} = 1.9V, 125°C		270	mA
$I_{DD2}(OP_1$[6,8])	V_{DD2} Supply current operating @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 4).	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0, V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		2	mA
$I_{DD2}(OP_2$[6,8])	V_{DD2} Supply current operating @ 50MHz, EDAC enabled @ default Scrub Rate Period (see table 4).	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0, V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)		5	mA

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
$I_{DD1}(SB)^{7,9}$	Supply current standby @ 0Hz, EDAC bypassed	CMOS inputs, I_{OUT} = 0 $\overline{E1}$ = V_{DD2} -0.2, E2 = GND V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C		25	mA
			125°C		70	mA
$I_{DD2}(SB)^{9}$	Supply current standby @ 0Hz, EDAC bypassed	CMOS inputs, I_{OUT} = 0 $\overline{E1}$ = V_{DD2} -0.2, E2 = GND V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			2	mA
$I_{DD1}(SB)^{7,9}$	Supply current standby A(18:0) @ 50MHz, EDAC bypassed	CMOS inputs, I_{OUT} = 0 $\overline{E1}$ = V_{DD2} - 0.2, E2 = GND, V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C		25	mA
			125°C		70	mA
$I_{DD2}(SB)^{9}$	Supply current standby A(18:0) @ 50MHz, EDAC bypassed	CMOS inputs, I_{OUT} = 0 $\overline{E1}$ = V_{DD2} - 0.2, E2 = GND, V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			2	mA

Notes:

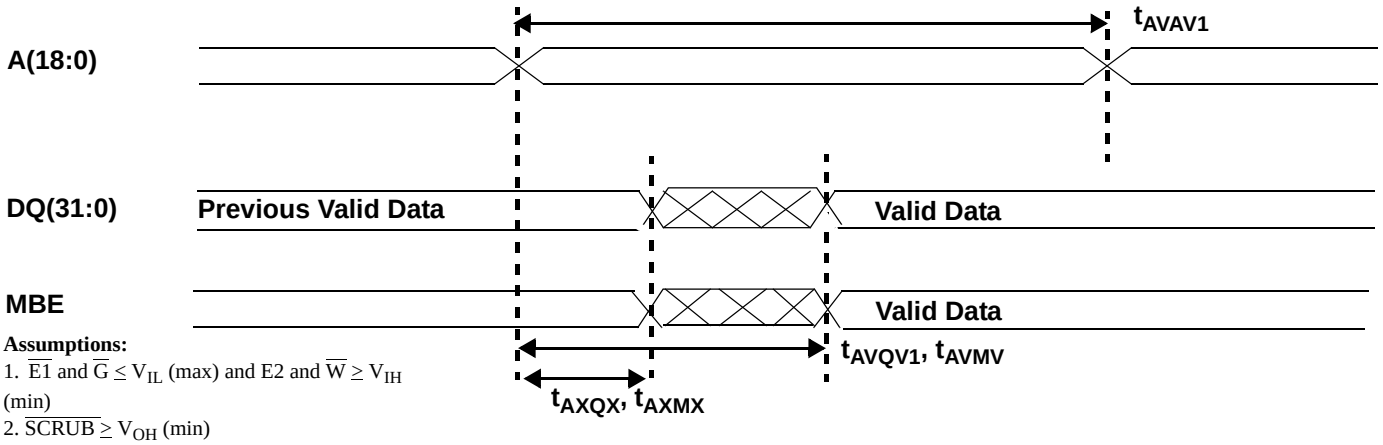
* For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.
1. The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for UT8ER512K32M (master) are tested functionally for VOL specification.
2. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
3. The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for UT8ER512K32M (master) are guaranteed by design, but neither tested nor characterized.
4. Supplied as a design limit but not guaranteed or tested.
5. Not more than one output may be shorted at a time for maximum duration of one second.
6. EDAC enabled. Default Scrub Rate Period applicable to master device only.
7. Post radiation limits are the 125°C temperature limit when specified.
8. Operating current limit includes standby current.
9. V_{IH} = V_{DD2} (max), V_{IL} = 0V.

AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

(Tc = -55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = 1.7V to 1.9V, V_{DD2} = 3.0V to 3.6V)

SYMBOL	PARAMETER			UNIT	FIGURE
		MIN	MAX		
t_{AVAV1}[1]	Read cycle time	20		ns	3a
t_{AVQV1}	Address to data valid from address change		20	ns	3c
t_{AXQX}[2]	Output hold time	3		ns	3a
t_{GLQX}[1,2]	$\overline{G}$-controlled output enable time	2		ns	3c
t_{GLQV}	$\overline{G}$-controlled output data valid		8	ns	3c
t_{GHQZ1}[2]	$\overline{G}$-controlled output three-state time	2	6	ns	3c
t_{ETQX}[2,3]	E-controlled output enable time	5		ns	3b
t_{ETQV}[3]	E-controlled access time		20	ns	3b
t_{EFQZ}[2,4]	E-controlled output three-state time[2]	2	7	ns	3b
t_{AVMV}	Address to error flag valid		20	ns	3a
t_{AXMX}[2]	Address to error flag hold time from address change	3		ns	3a
t_{GLMX}[2]	$\overline{G}$-controlled error flag enable time	2		ns	3c
t_{GLMV}	$\overline{G}$-controlled error flag valid		7	ns	3c
t_{ETMX}[2]	E-controlled error flag enable time	5		ns	3b
t_{ETMV}[3]	E-controlled error flag time		20	ns	3b
t_{GHMZ}[2]	G-controlled error flag three-state time	2	6	ns	3b

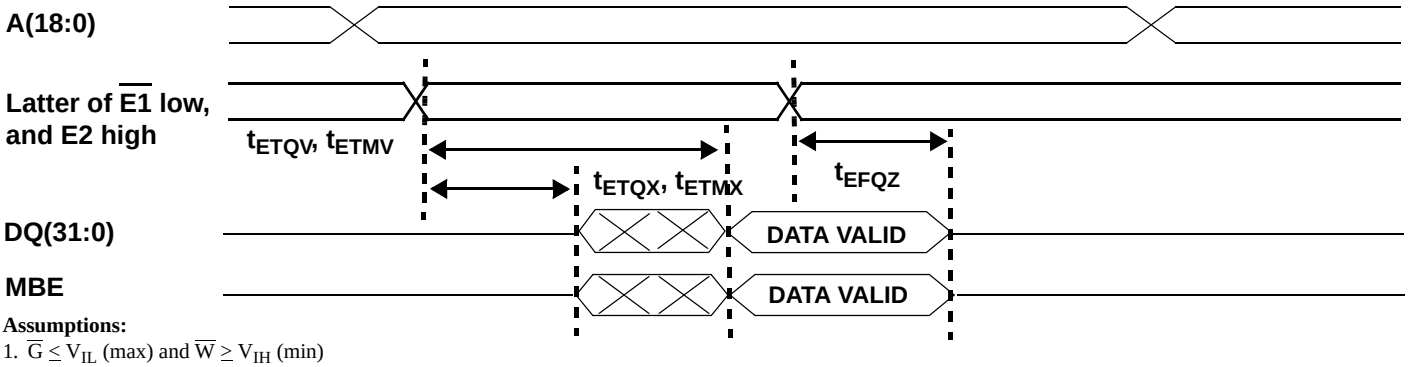
Notes:
* For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.
1. Guaranteed by characterization, but not tested.
2. Three-state is defined as a 300mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the latter falling edge of $\overline{E1}$ or rising edge of E2.
4. The EF (enable false) notation refers to the latter rising edge of $\overline{E1}$ or falling edge of E2.



Assumptions:

1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max) and E2 and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

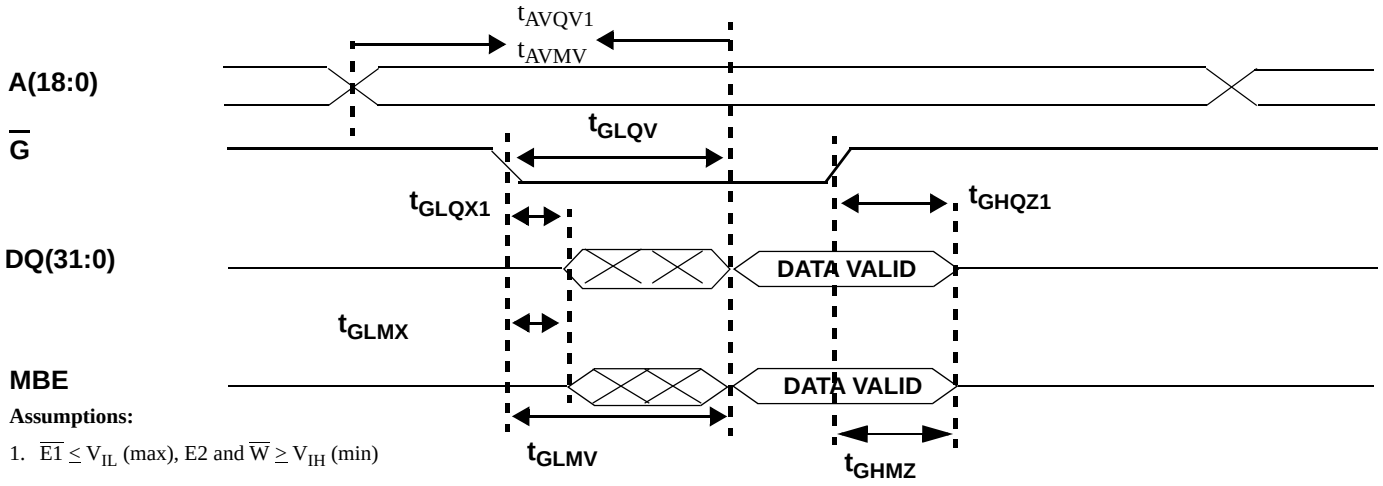
Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:

1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:

1. $\overline{E1} \leq V_{IL}$ (max), E2 and $\overline{W} \geq V_{IH}$ (min)
2. $\overline{SCRUB} \geq V_{OH}$ (min)
3. Reading uninitialized addresses will cause MBE to be asserted.

Figure 3c. SRAM Read Cycle 3: Output Enable Access

AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)*

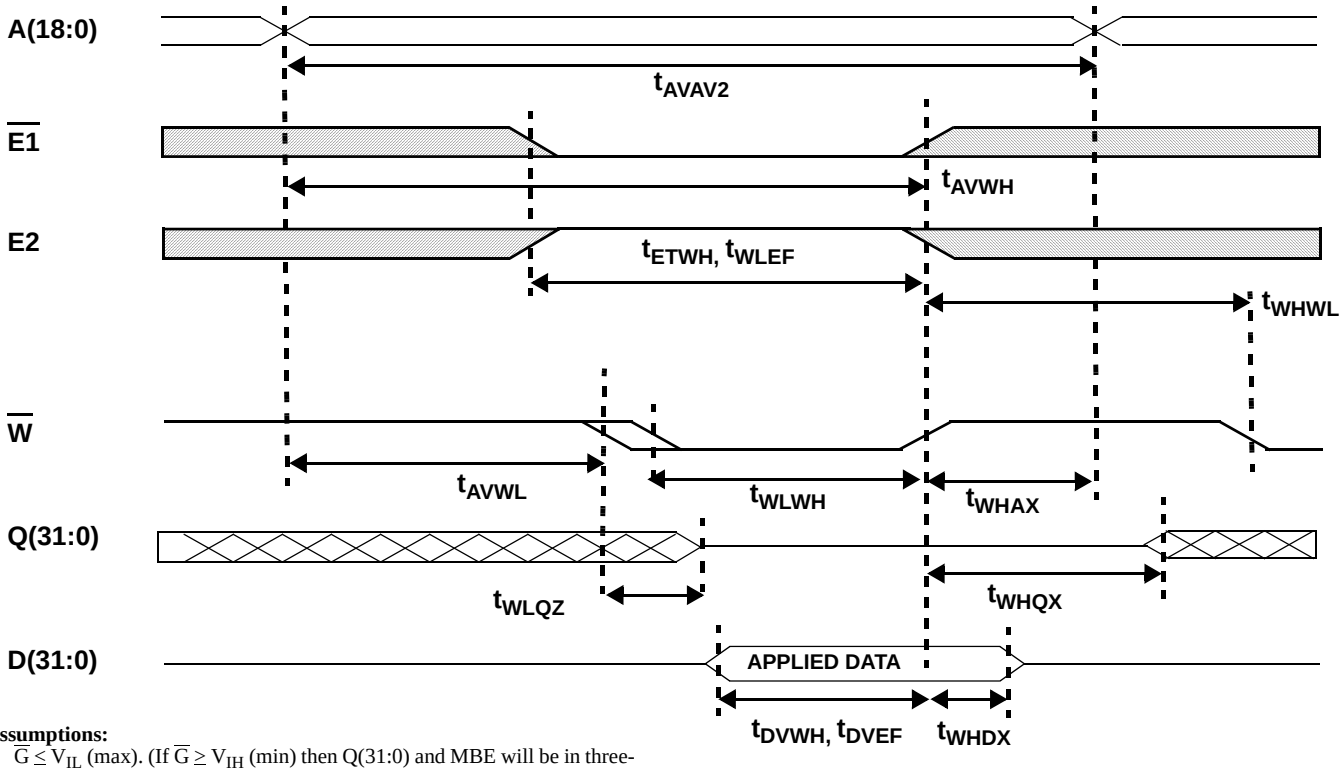
(Tc = -55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = 1.7V to 1.9V, V_{DD2} = 3.0V to 3.6V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{AVAV2}[1]	Write cycle time	10		ns	4a/4b
t_{ETWH}	Device enable to end of write	10		ns	4a
t_{AVET}	Address setup time for write ($\overline{E1}$/E2- controlled)	0		ns	4b
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		ns	4a
t_{WLWH}[1]	Write pulse width	8		ns	4a
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	0		ns	4a
t_{EFAX}	Address hold time for device enable ($\overline{E1}$/E2- controlled)	0		ns	4b
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		7	ns	4a/4b
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	3		ns	4a
t_{ETEF}	Device enable pulse width ($\overline{E1}$/E2 - controlled)	10		ns	4b
t_{DVWH}	Data setup time	5		ns	4a
t_{WHDX}	Data hold time	2		ns	4a
t_{WLEF}[1]	Device enable controlled write pulse width	8		ns	4b
t_{DVEF}	Data setup time	5		ns	4a/4b
t_{EFDX}	Data hold time	2		ns	4b
t_{AVWH}	Address valid to end of write	10		ns	4a
t_{WHWL}[1]	Write disable time	2		ns	4a

Notes:

* For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.

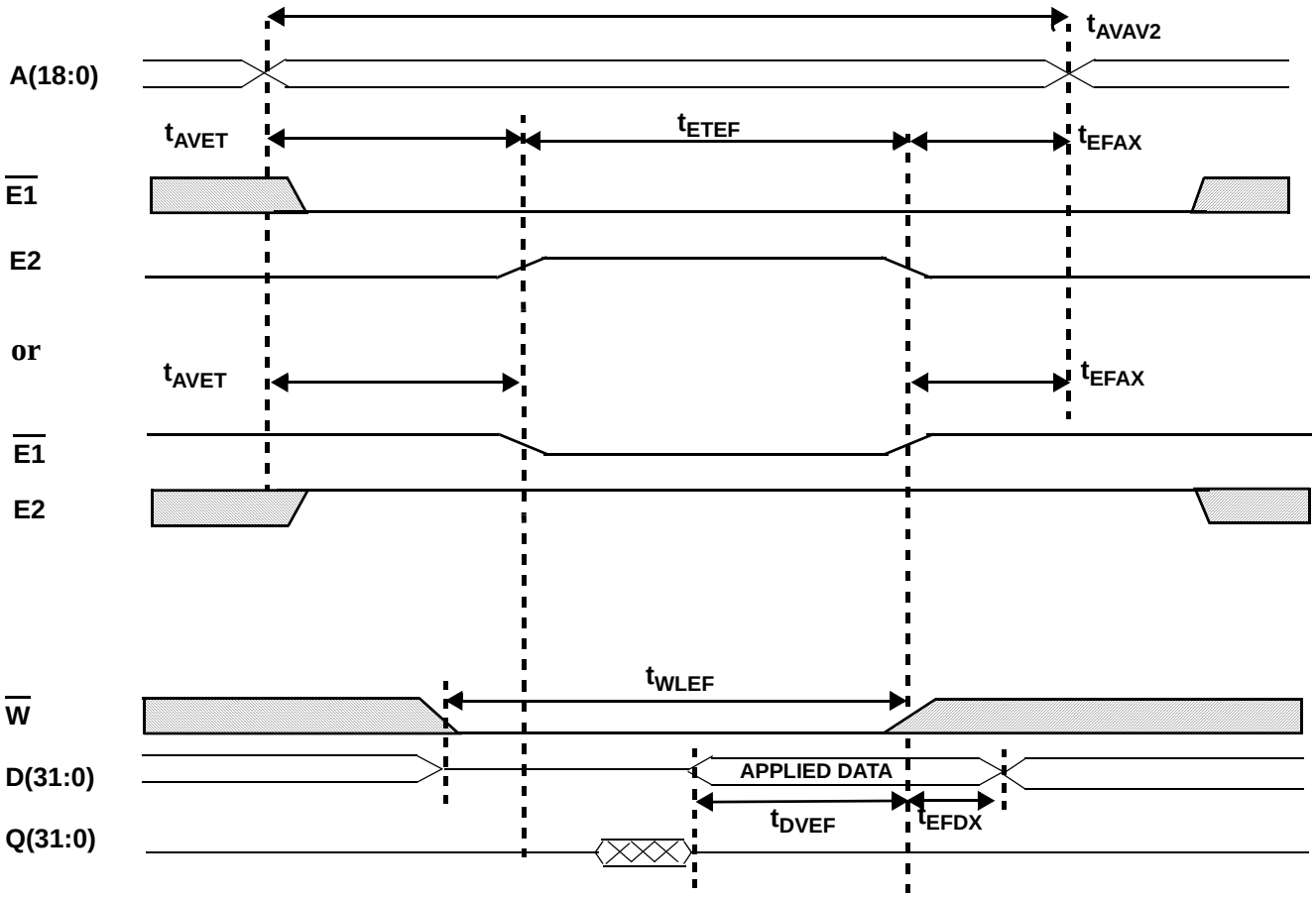
1. Tested with $\overline{G}$ high.
2. Three-state is defined as 300mV change from steady-state output voltage.



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and MBE will be in three-state for the entire cycle.)

2. $\overline{SCRUB} \geq V_{OH}$ (min)

Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access

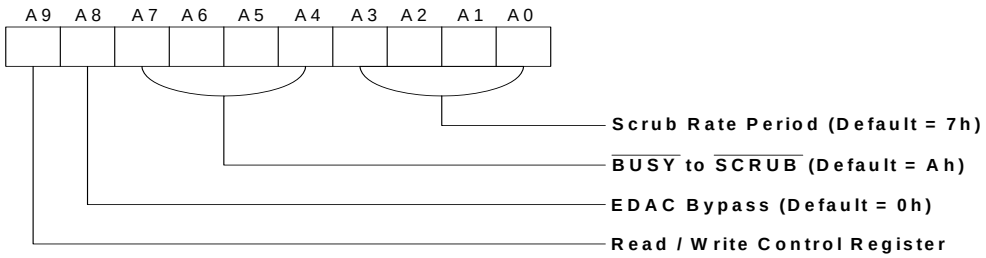


Assumptions & Notes:
1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and MBE will be in three-state for the entire cycle.)

2. Either $\overline{E1}$ / E2 scenario can occur.

3. $\overline{SCRUB} \geq V_{OH}$ (min)

Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access



Note:
1. See Table 4 for Control Register Definitions

Figure 5. EDAC Control Register

Table 4: EDAC Programming Configuration Table

ADDR BIT	PARAMETER	VALUE	FUNCTION
A (0 - 3)	Scrub Rate Period[1,2,3]	3-15 Note: 0-2 reserved	As Scrub Rate Period changes from 0 - 15, then the interval between Scrub cycles will change as follows: 3 = 600 ns 8 = 13.0 us 12 = 205 us 4 = 1000 ns 9 = 25.8 us 13 = 409.8 us[4] 5 = 1800 ns 10 = 51.4 us 14 = 819.4 us[4] 6 = 3400 ns 11 = 102.6 us 15 = 1.64 ms[4] 7 = 6600 ns
A (4 - 7)	$\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$[1,3,5]	0-15	If $\overline{\text{BUSY}}$ changes from 0 - 15, then the interval t_{BLSL} between $\overline{\text{SCRUB}}$ and BUSY will change as follows: 0 = 0 ns 6 = 300 ns 11 = 550 ns 1 = 50 ns 7 = 350 ns 12 = 600 ns 2 = 100 ns 8 = 400 ns 13 = 650 ns 3 = 150 ns 9 = 450 ns 14 = 700 ns 4 = 200 ns 10 = 500 ns 15 = 750 ns 5 = 250ns
A (8)	Bypass EDAC Bit [6]	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed.
A (9)	Read / Write Control Register	0, 1	0 = A0 to A8 will be written to the control register 1 = Control register will be asserted to the data bus

Notes:
1. Values based on minimum specifications. For guaranteed ranges of Scrub Rate Period (t_{SCRT}) and $\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ (t_{BLSL}), reference the Master Mode AC Characteristic table.
2. Default Scrub Rate Period is 6600 ns.
3. Scrub Rate Period and $\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ applicable to the UT8ER512K32M device only.
4. Period below test capability.
5. The default for t_{BLSL} is 500 ns.
6. The default state for A8 is 0.

EDAC CONTROL REGISTER AC CHARACTERISTICS (Pre and Post-Radiation)*

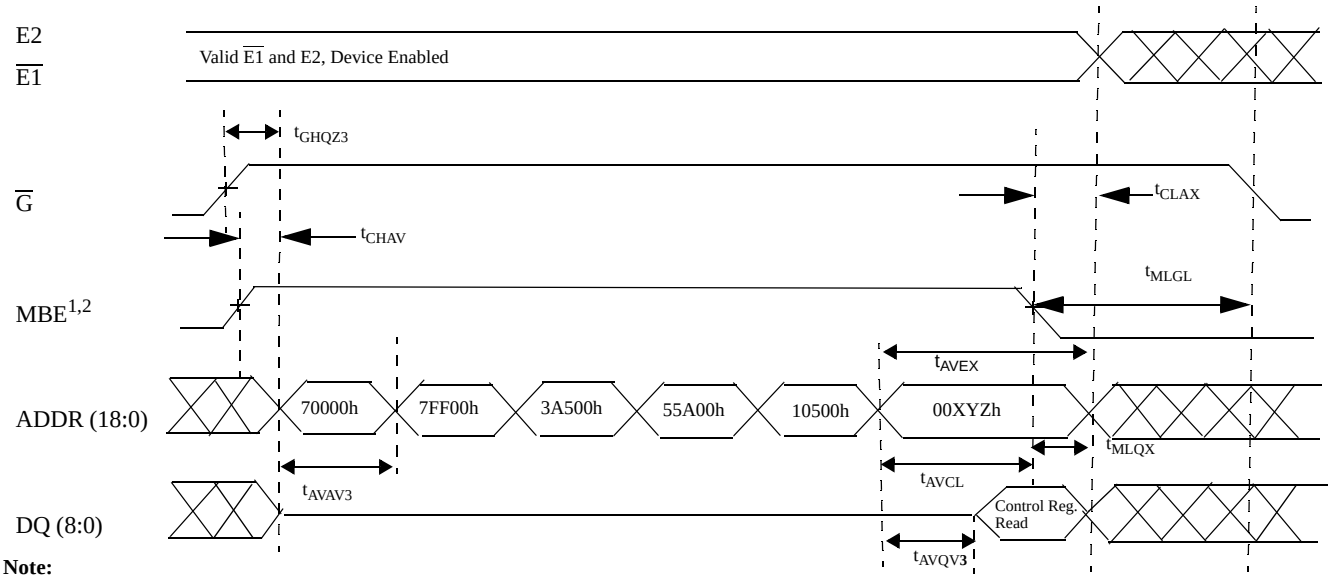
(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = 1.7V to 1.9V, V_{DD2} = 3.0V to 3.6V

SYMBOL	PARAMETER			UNIT	FIGURE
		MIN	MAX		
t_{AVAV3}	Address valid to address valid for control register cycle	200		ns	6a
t_{AVCL}	Address valid to control low	400		ns	6a
t_{AVEX}	Address valid to enable valid	200		ns	6a
t_{AVQV3}	Address to data valid control register read		400	ns	6a
t_{CHAV}	MBE high to address valid	0		ns	6a
t_{CLAX}	MBE low to address hold time	0		ns	6a
t_{MLQX}[1]	MBE control EDAC disable time	3		ns	6a
t_{GHQZ3}[1]	Output tri-state time	2	9	ns	6a
t_{MLGL}[2]	MBE low to output enable	85		ns	6a

Notes:

* For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.

1. Three-state is defined as 300mV change from steady-state output.
2. Guaranteed by design neither tested or characterized.



Note:

1. MBE is driven high by the user.
2. Device must see a transistion to address 70000h coincident with or subsequent to MBE assertion.
3. Lower 10 bits of the last address are used to read or configure the control register (ref Control Register Write/Read Cycles page 3 and Table 4).

Assumptions:

1. $\overline{SCRUB} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.

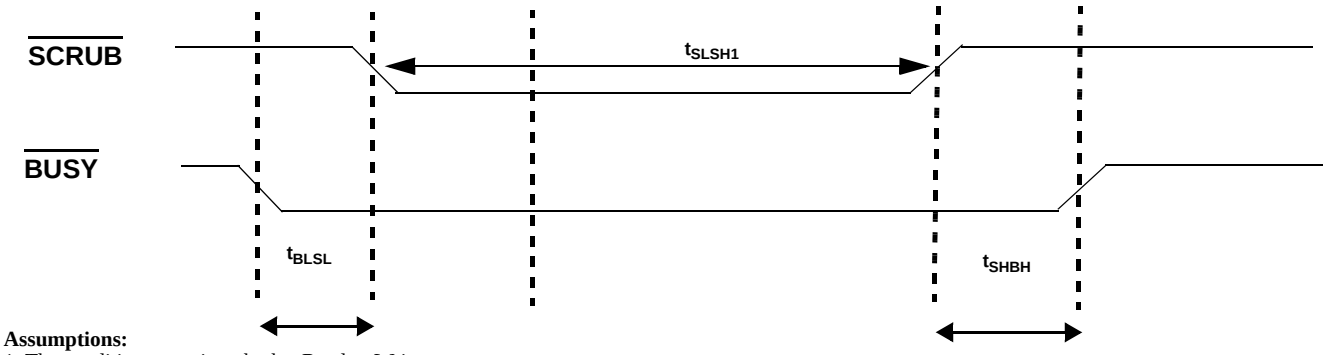
Figure 6a. EDAC Control Register Cycle

MASTER MODE AC CHARACTERISTICS (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = 1.7V to 1.9V, V_{DD2} = 3.0V to 3.6V

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{BLSL}[1]	User Programmable - $\overline{BUSY}$ low to $\overline{SCRUB}$	(50)(n)	(90)(n)+1	ns	6b
t_{SLSH1}	$\overline{SCRUB}$ low to $\overline{SCRUB}$ high	200	350	ns	6b
t_{SHBH}	$\overline{SCRUB}$ high to $\overline{BUSY}$ high	50	85	ns	6b
t_{SCRT}[2]	Scrub Rate Period	$(2^n)(50)+200$	$(2^n)(90)+350$	ns	

Notes:
* For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.
1. See Table 4 for User Programmable information. The value "n" is decimal equivalent of hexidecimal value 0x0 through 0xF programmed into control register address bits A_4-A_7 by user. Default value "n" = 10.
2. See Table 4 for User Programmable information. The value "n" is decimal equivalent of hexidecimal value 0x3 through 0xF programmed into control register address bits A_0-A_3. Default value is "n" = 7.



Assumptions:
1. The conditions pertain to both a Read or Write.

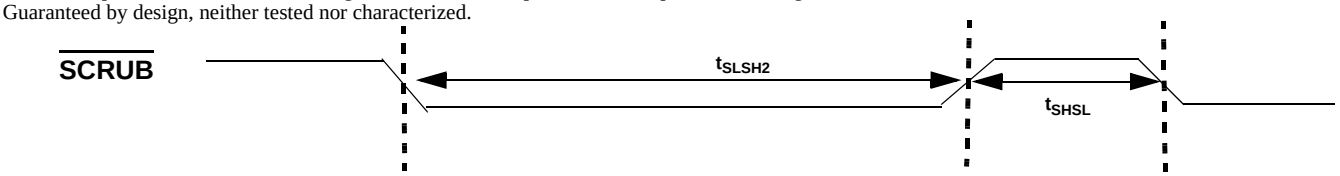
Figure 6b. Master Mode Scrub Cycle

SLAVE MODE AC CHARACTERISTICS (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = V_{DD1} (min), V_{DD2} = V_{DD2} (min))

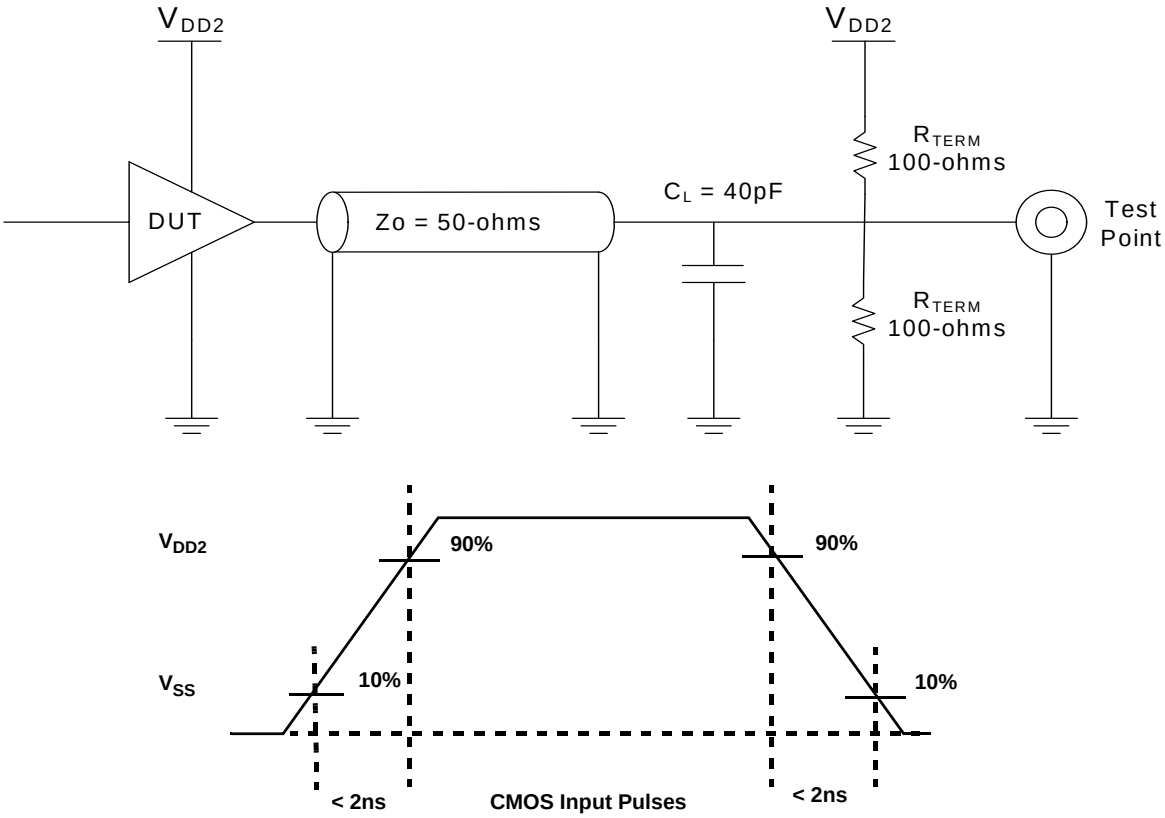
SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t_{SLSH2}	$\overline{SCRUB}$ low to $\overline{SCRUB}$ high (slave)	200		ns	6c
t_{SHSL}[1]	$\overline{SCRUB}$ high to $\overline{SCRUB}$ low (slave)	400		ns	6c

Notes:
* For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.
1. Guaranteed by design, neither tested nor characterized.



Assumptions:
1. The conditions pertain to both a Read or Write.

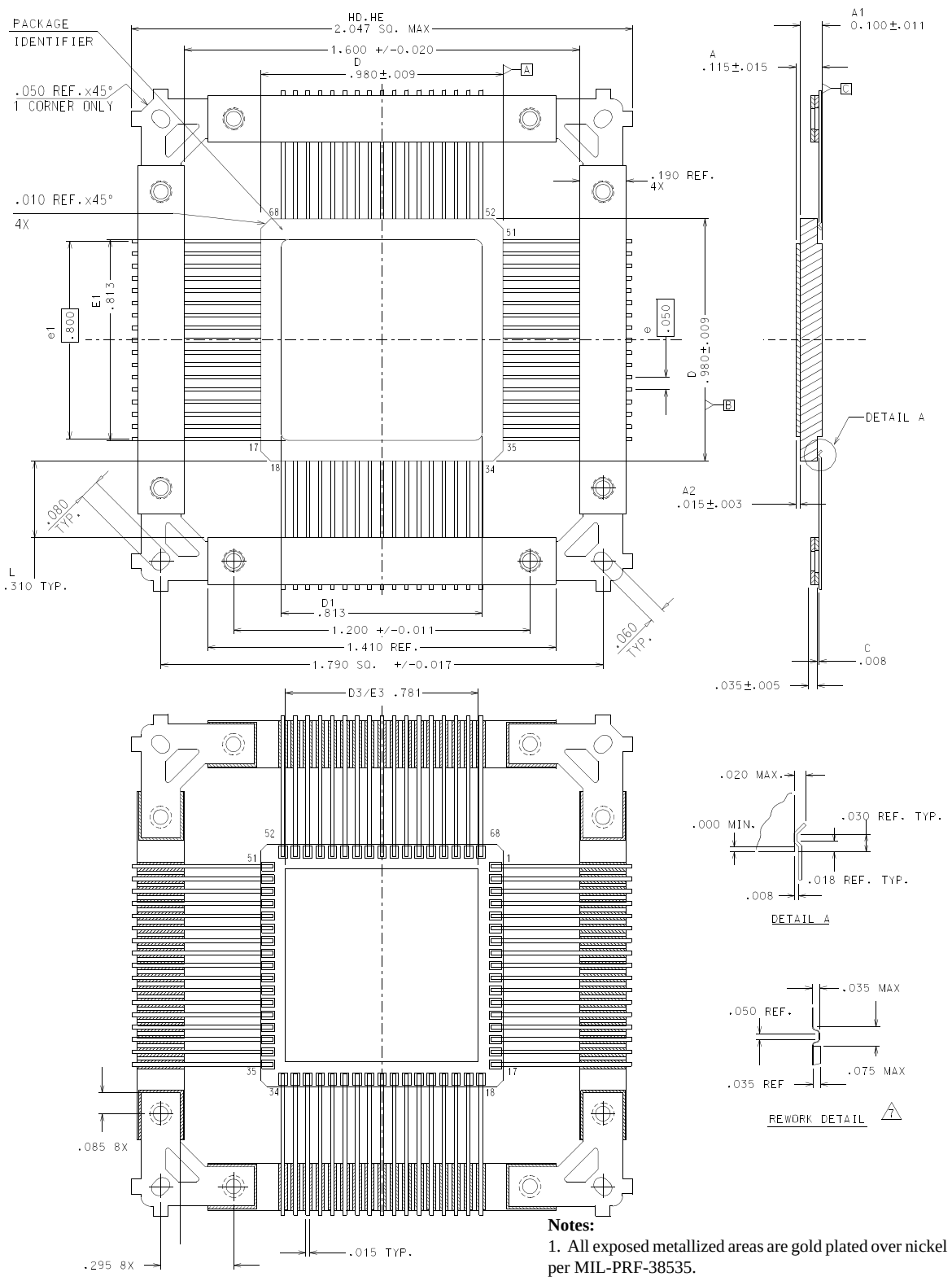
Figure 6c. Slave Mode Scrub Cycle



Notes:
1. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$

Figure 7. AC Test Loads and Input Waveforms

PACKAGING



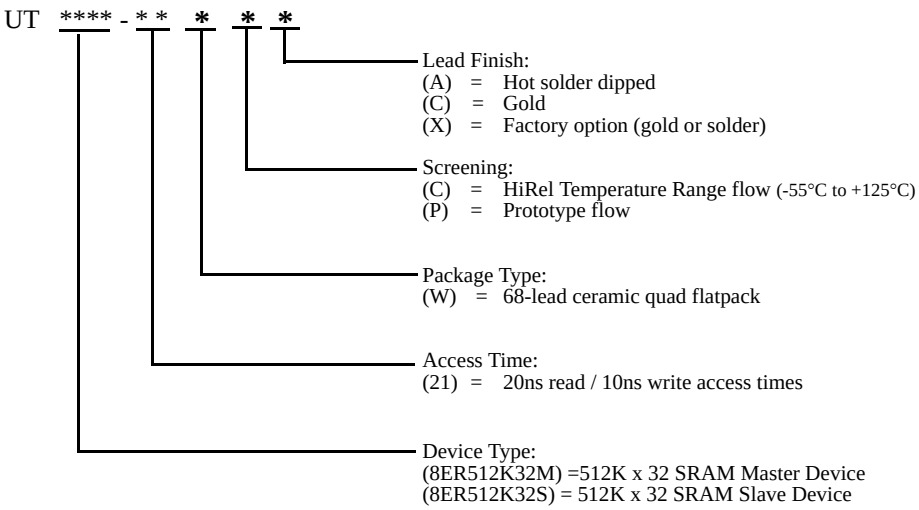
Notes:

1. All exposed metallized areas are gold plated over nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.

Figure 8. 68-Lead Ceramic Quad Flatpack

ORDERING INFORMATION

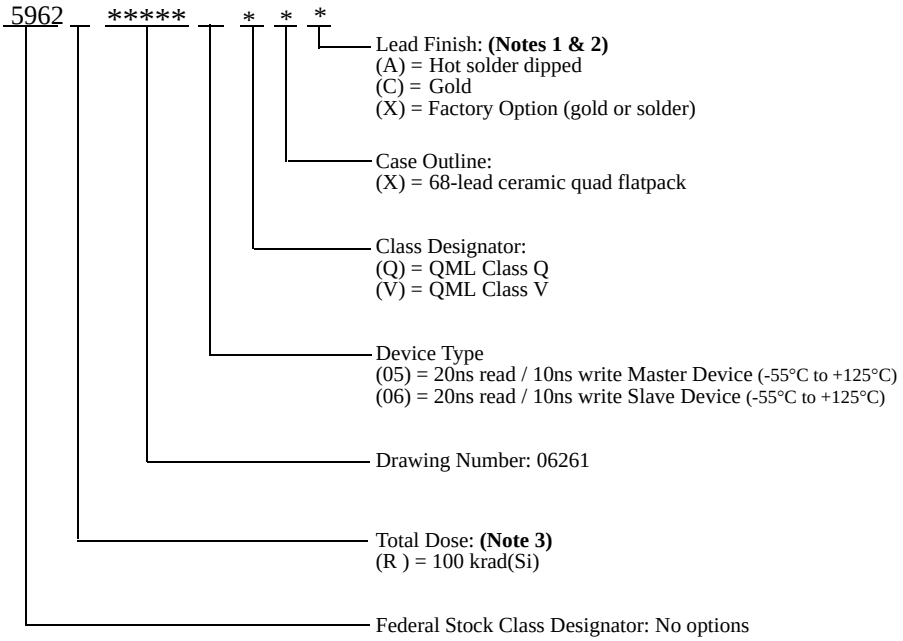
512K x 32 SRAM



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. HiRel Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

512K x 32 SRAM: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3.TID tolerance guarantee is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2 resulting in an effective dose rate of 1 rad(Si)/sec.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

COLORADO
Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
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A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused

Low Power SRAM Read Operations

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number:*
4M Asynchronous SRAM	UT8R128K32	5962-03236	01 & 02	WC03
4M Asynchronous SRAM	UT8R512K8	5962-03235	01 & 02	WC01
16M Asynchronous SRAM	UT8CR512K32	5962-04227	01 & 02	MQ08
16M Asynchronous SRAM	UT8ER512K32	5962-06261	05 & 06	WC04/05
4M Asynchronous SRAM	UT8Q512E	5962-99607	05 & 06	WJ02
4M Asynchronous SRAM	UT9Q512E	5962-00536	05 & 06	WJ01
16M Asynchronous SRAM	UT8Q512K32E	5962-01533	02 & 03	QS04
16M Asynchronous SRAM	UT9Q512K32E	5962-01511	02 & 03	QS03
32M Asynchronous SRAM	UT8ER1M32	5962-10202	01 - 04	QS16/17
64M Asynchronous SRAM	UT8ER2M32	5962-10203	01 - 04	QS09/10
128M Asynchronous SRAM	UT8ER4M32	5962-10204	01 - 04	QS11/12
40M Asynchronous SRAM	UT8R1M39	5962-10205	01 & 02	QS13
80M Asynchronous SRAM	UT8R2M39	5962-10206	01 & 02	QS14
160M Asynchronous SRAM	UT8R4M39	5962-10207	01 & 02	QS15

* PIC = Aeroflex's internal Product Identification Code

1.0 Overview

The purpose of this application note is to discuss the Aeroflex SRAMs low power read architecture and to inform users of the affects associated with the low power read operations.

2.0 Low Power Read Architecture

The aforementioned Aeroflex designed SRAMs all employ an architecture which reduces power consumption during read accesses. The architecture internally senses data only when new data is requested. A request for new data occurs anytime the chip enable device pin is asserted, or any of the device address inputs transition states while the chip enable is asserted. A trigger is generated and sent to the sensing circuit anytime a request for new data is observed. Since several triggers could occur simultaneously, these triggers are wire-ORed to result in a single sense amplifier activity for the read request. This design method results in less power consumption than designs that continually sense data. Aeroflex's low power SRAMs listed above activate the sensing circuit for approximately 5ns whenever and access is requested, thereby, significantly reducing active power.

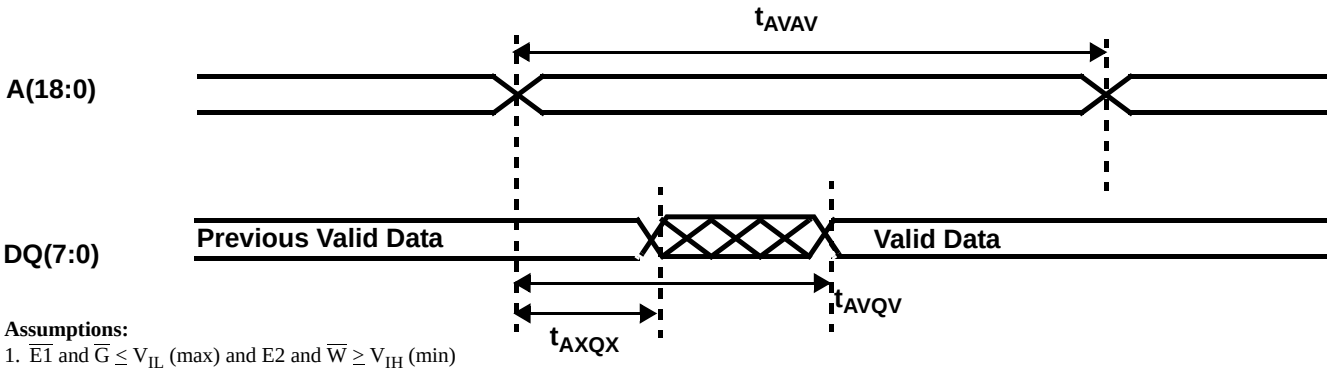
2.1 The SRAM Read Cycles.

The data sheets for all the devices noted in Table #1 discuss three methods for performing a read operation. The two most common methods for reading data are an Address Access and a Chip Enabled-Controlled Access. The third access discussed is the Output Enable-Controlled Access. The sequence at which control lines and address inputs are toggled determines which cycle is considered relevant. As discussed in section 2.0, an assertion of chip enable or any address transition while chip enable is asserted, initiates a read cycle. If the device chip enable is asserted prior to any address input transitions, then the read access is considered an Address Access. By keeping the device enabled and repeatedly switching address locations, the user retrieves all data of interest. A Chip Enable-Controlled Access occurs when the address signals are stable prior to asserting the chip enable. The Output Enabled-Controlled Access requires that either an Address Access or Chip Enable-Controlled Access has already been performed and the data is waiting for the Output Enable pin to assert, driving data to the device I/O pins.

The subsequent read cycle verbiage and diagrams are based on the Aeroflex UT8R512K8 data sheet. The number of control, input, and I/O pins will vary across the products listed in Table 1. The basic design family functionality for read operations is common among all the devices.

2.1.0 Address Access Read Cycle

The Address Access is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).



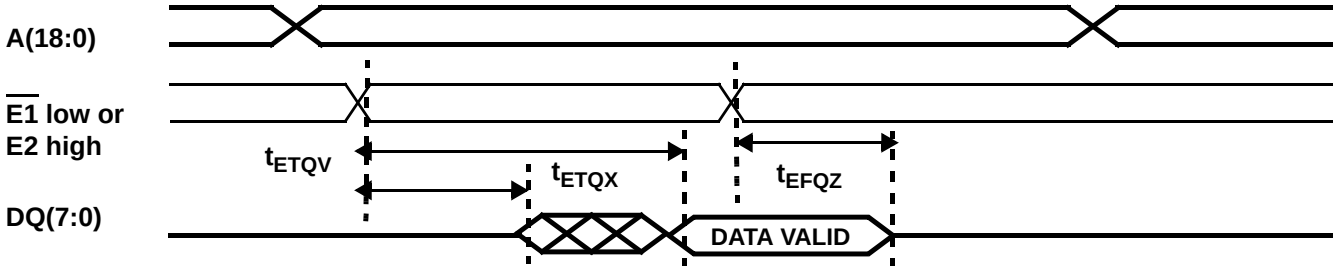
Assumptions:
1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max) and E2 and $\overline{W} \geq V_{IH}$ (min)

Note: No time references are relevant with respect to Chip Enable(s). Chip Enable(s) is assumed to be asserted.

SRAM Read Cycle 1: Address Access

2.1.1 Chip Enable-Controlled Read Cycle

The Chip Enable-controlled Access is initiated by $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).



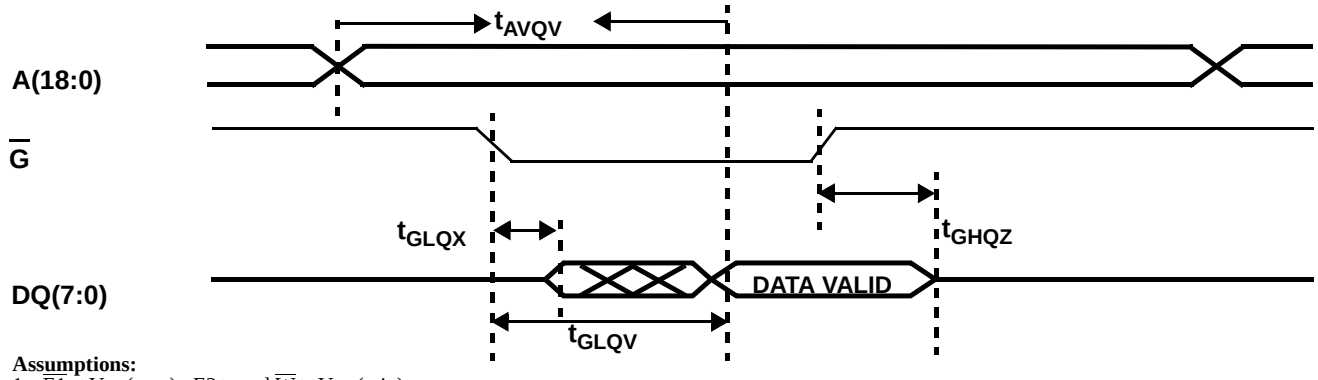
Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Note: No specification is given for address set-up time with respect to chip enable assertion. The read cycle description states that addresses are to remain stable for the entire cycle. Address set-up time relative to chip enable is assumed to be 0ns minimum.

SRAM Read Cycle 2: Chip Enable Access

2.1.1 Output Enabled-Controlled Read Cycle

The Output Enable-controlled Access is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.



Assumptions:
1. $\overline{E1} \leq V_{IL}$ (max) , E2 > and $\overline{W} \geq V_{IH}$ (min)

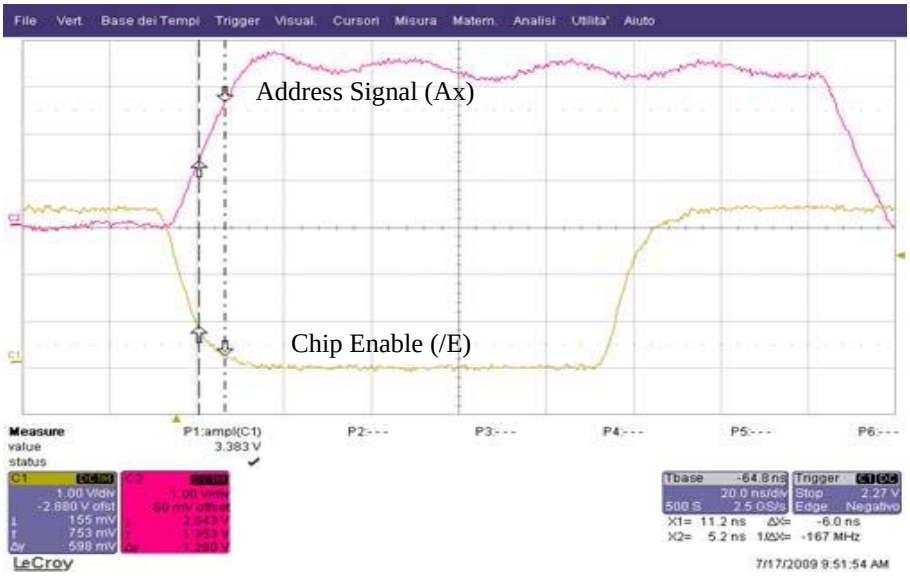
SRAM Read Cycle 3: Output Enable Access

3.0 Low Power Read Architecture Timing Consideration

The low power read architecture employed by Aeroflex designed SRAMs results in significant power reduction, especially in applications with longer than minimum read cycle times. However, this type of architecture is responsive to excessive input signal skew when device addressing and chip enable assertion occur simultaneously. Signal skew of greater than 4-5ns between all of the read triggering activities is sufficient to start another read cycle.

3.1 Simultaneous Control and Address Switching

Simultaneous switching of controls and address pins, alone, is not a problem; excessive skew between them is the concern. Consider the application where several SRAM devices are connected to the same memory bus. The address bus is commonly connected to all the devices, but the chip enable pin is singularly connected to each individual SRAM. This configuration results in a loading difference between the address inputs and the chip enable. This lightly loaded chip enable propagates to the memory more quickly than the heavily loaded address lines. The oscilloscope capture of Figure #1 is the actual timing of an application which had intermittent data errors due to address transitions lagging chip enable.



- Timing shown from VIL (yellow trace /CS) and VIH (pink for address signal) as delta X = 6ns. Even at actual internal gate switching point (~ VDD/2), the skew is still around 6ns.

Figure #1 SRAM Signal Capture

The signal transitions in the scope plot of Figure #1 appear to be fairly coincidental. A closer look however, reveals the chip enable signal actually starts and reaches V_{IL} approximately 6ns before the address signal reaches V_{IH}. Even at one half V_{DD} (closer to actual logical gate switching of the inputs), the delta in signal times is still approximately 6ns.

Simultaneous switching of controls and address inputs is not recommended for a couple of reasons. The first is the previously described signal skew sensitivity between controls and/or address inputs. The second reason is that activating all the controls and address inputs simultaneously results in peak instantaneous current consumption. This condition causes maximum strain to the power decoupling. Chip Enable activates address decoding circuits, address switching introduces input buffer switching current, and output enable assertion turns on all the device output drivers. Peforming all three simultaneously results in worst case transient current demand by the memory.

3.1.0 Technical Overview of Skew Sensitivity

Recall from section 2.0 that any activity requesting new data causes a read trigger. The triggers are wire-ORed together. In order to meet the faster access times demanded by today's applications, the ORed trigger only exists during the first 4-5ns of the read cycle. Since the slowest of the address transitions occurs more than 5ns after the initiation of the read activity, a second read activity is initiated. The sensing circuit does not have time to normalize before the second read activity has started. For this reason a Chip Enable-Controlled read cycle requires that address inputs remain stable for the entire cycle. Infrequent and random sensing errors can result if the bit columns are continually pulled to one state then quickly requested to sense the opposite state. Another effect of the low power read architecture that differs from previous generation designs (those that continually sense for data) is that the bit line will not be sensed again until another read triggering event occurs. If another read trigger event (chip enable assertion and/or address change) does no occur for a particular address, the incorrect data remains at the outputs.

4.0 Summary and Conclusion

The Aeroflex SRAMs in Table #1 all employ a low power consumption read architecture. Power is conserved by sensing data only when new data is requested. A request occurs anytime chip enable is asserted or any address input signal transitions while chip enable is asserted. The data sheets for the SRAMs listed in Table #1 do not explicitly define the case of simultaneous switching of address and control signals during read operations. Data sheet read cycle descriptions indicate that control inputs are established prior to address changes, and address inputs are stable prior to control assertions. Simultaneous switching of addresses and controls is tolerable, when the skew between all input signals is < 4ns. For designs that must employ the simultaneous activation of address and control signals, two important issues should be considered by the designer. The first is the input signal skew sensitivity of the low power read architecture discussed by this application note. The second is the instantaneous current consumption that results from simultaneous access methods. Aeroflex recommends the use of only one read access method at a time. If multiple read accesses (simultaneous chip enable assertion and address switching) cannot be avoided, then Aeroflex recommends that the chip enable signal be delayed until all addresses have completed transitions.