Standard Products

UT9Q512K32E 16 Megabit RadTolerant SRAM MCM

Data Sheet

June 28, 2011

FEATURES

- 25ns maximum (5 volt supply) address access time
- Asynchronous operation for compatible with industry standard 512K x 8 SRAMs
- TTL compatible inputs and output levels, three-state bidirectional data bus
- Operational environment:
  - Total dose: 50 krads(Si)
  - SEL Immune >110 MeV-cm^2/mg
  - LET$_{TH}$(0.25) = >52 MeV-cm^2/mg
  - Saturated Cross Section (cm^2) per bit, 2.8E-8
    - ≤1.1E-9 errors/bit-day, Adams 90% geosynchronous heavy ion
- Packaging:
  - 68-lead dual cavity ceramic quad flatpack (CQFP) (11.0 grams)
- Standard Microcircuit Drawing 5962-01511
  - QML Q and Vcompliant part

INTRODUCTION

The UT9Q512K32E RadTol product is a high-performance 2M byte (16Mbit) CMOS static RAM multi-chip module (MCM), organized as four individual 524,288 x 8 bit SRAMs with a common output enable. Memory expansion is provided by an active LOW chip enable ($\overline{E}$n), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to each memory is accomplished by taking chip enable ($\overline{E}$n) input LOW and write enable ($\overline{W}$n) inputs LOW. Data on the eight I/O pins (DQ_0 through DQ_7) is then written into the location specified on the address pins (A_0 through A_{18}). Reading from the device is accomplished by taking chip enable ($\overline{E}$n) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$n) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The input/output pins are placed in a high impedance state when the device is deselected ($\overline{E}$n HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E}$n LOW and $\overline{W}$n LOW). Perform 8, 16, 24 or 32 bit accesses by making $\overline{W}$n along with $\overline{E}$n a common input to any combination of the discrete memory die.

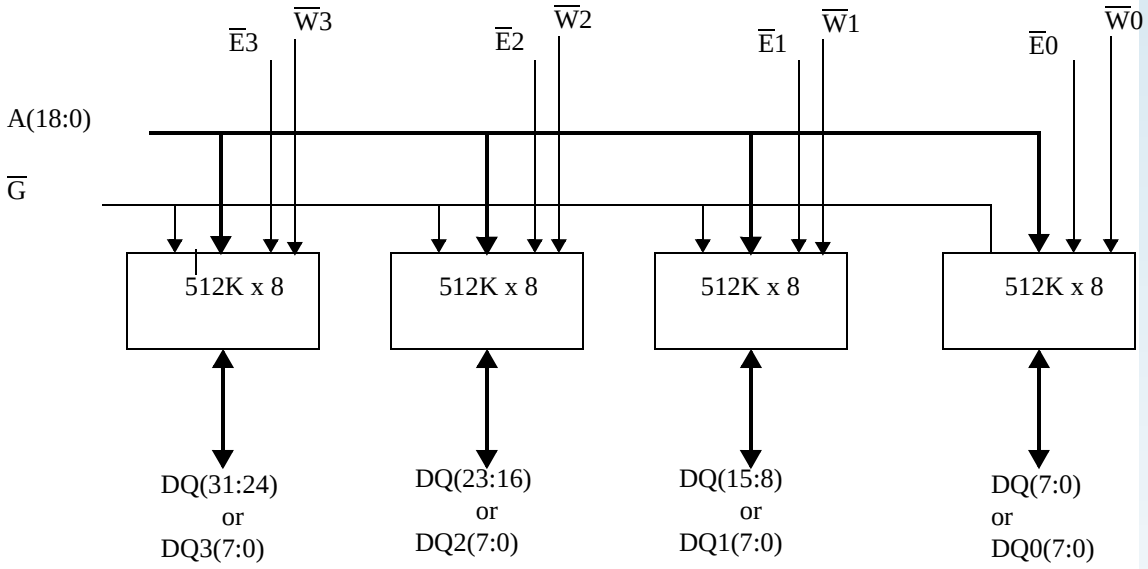


Figure 1. UT9Q512K32E SRAM Block Diagram

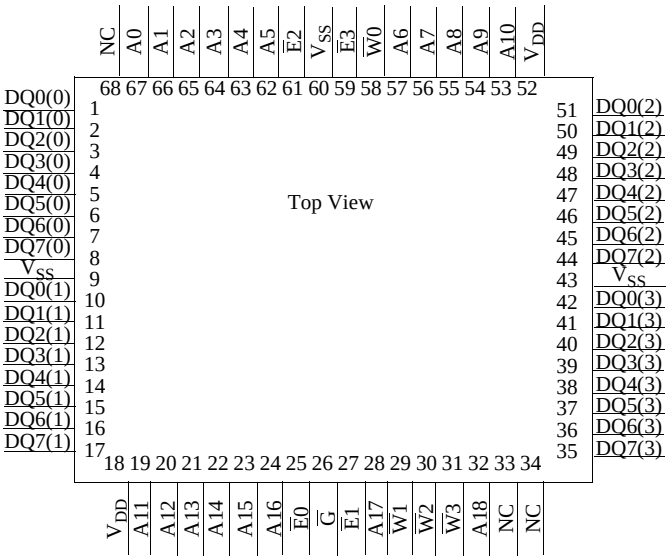


Figure 2. 25ns SRAM Pinout (68)

PIN NAMES

A(18:0)	Address	$\overline{Wn}$	Write Enable
DQn(7:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{E}n$	Enable	V_{DD}	Power
		V_{SS}	Ground

DEVICE OPERATION

The UT9Q512K32E has three control inputs called Enable 1 ($\overline{E}n$), Write Enable ($\overline{W}n$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0). $\overline{E}n$ Device Enable controls device selection, active, and standby modes. Asserting $\overline{E}n$ enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. $\overline{W}n$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{Wn}$	$\overline{En}$	I/O Mode	Mode
X[1]	X	1	3-state	Standby
X	0	0	Data in	Write
1	1	0	3-state	Read[2]
0	1	0	Data out	Read

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of $\overline{W}n$ greater than V_{IH} (min) and $\overline{E}n$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of Device Enable, Output Enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}n$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as Device Enable and Output Enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM read Cycle 2, the Chip Enable - Controlled Access in figure 3b, is initiated by $\overline{E}n$ going active while $\overline{G}$ remains asserted, $\overline{W}n$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).

SRAM read Cycle 3, the Output Enable - Controlled Access in figure 3c, is initiated by $\overline{G}$ going active while $\overline{E}n$ is asserted, $\overline{W}n$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}n$ less than V_{IL}(max) and $\overline{E}n$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}n$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access is defined by a write terminated by $\overline{W}n$ going high, with $\overline{E}n$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}n$, and by t_{ETWH} when the write is initiated by $\overline{E}n$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the nine bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access is defined by a write terminated by the latter of $\overline{E}n$ going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}n$, and by t_{ETEF} when the write is initiated by the $\overline{E}n$ going active. For the $\overline{W}n$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

OPERATIONAL ENVIRONMENT

The UT9Q512K32E SRAM incorporates features which allows operation in a limited environment.

Table 2. Operational Environment Design Specifications[1]

Total Dose	50	krad(Si)
Heavy Ion Error Rate[2]	<1.1E-9	Errors/Bit-Day

Notes:
1. The SRAM will not latchup during radiation exposure under recommended operating conditions.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.5 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.5 to 7.0V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.0W (per byte)
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	4.5 to 5.5V
T_C	Case temperature range	(W) Screen - 40°C to 105°C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

-40°C to +105°C (V_{DD} = 5.0V ± 10% for (W) screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage	(TTL)	2.0		V
V_{IL}	Low-level input voltage	(TTL)		0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA, V_{DD} =4.5V (TTL)		0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = 200µA,V_{DD} =4.5V (CMOS)		0.08	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA,V_{DD} =4.5V (TTL)	2.4		V
V_{OH2}	High-level output voltage	I_{OH} = 200µA,V_{DD} =4.5V (CMOS)	3.0		V
C_{IN}[1]	Input capacitance	*f* = 1MHz @ 0V		45	pF
C_{IO}[1]	Bidirectional I/O capacitance	*f* = 1MHz @ 0V		25	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}, V_{DD} = V_{DD} (max)	-2	2	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS} V_{DD} = V_{DD} (max) $\overline{G}$ = V_{DD} (max)	-2	2	µA
I_{OS}[2, 3]	Short-circuit output current	V_{DD} = V_{DD} (max), V_O = V_{DD} V_{DD} = V_{DD} (max), V_O = 0V	-90	90	mA
I_{DD}(OP)	Supply current operating @ 1MHz (per byte)	Inputs: V_{IL} = 0.8V, V_{IH} = 2.0V I_{OUT} = 0mA V_{DD} = V_{DD} (max)		40	mA
I_{DD1}(OP)	Supply current operating @40MHz (per byte)	Inputs: V_{IL} = 0.8V, V_{IH} = 2.0V I_{OUT} = 0mA V_{DD} = V_{DD} (max)		70	mA
I_{DD2}(SB)	Supply current standby @0MHz (per byte)	Inputs: V_{IL} = V_{SS} -40°C and 25°C I_{OUT} = 0mA $\overline{E1}$ = V_{DD} - 0.5, V_{DD} = V_{DD} (max) 105°C V_{IH} = V_{DD} - 0.5V		9 24	mA mA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

AC CHARACTERISTICS READ CYCLE (Pre/Post-Radiation)*

-40°C to +105°C (V_{DD} = 5.0V ± 10% for (W) screening)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}[1]	Read cycle time	25		ns
t_{AVQV}	Read access time		25	ns
t_{AXQX}[2]	Output hold time	3		ns
t_{GLQX}[2]	$\overline{G}$-controlled Output Enable time	0		ns
t_{GLQV}	$\overline{G}$-controlled Output Enable time (Read Cycle 3)		10	ns
t_{GHQZ}[2]	$\overline{G}$-controlled output three-state time		10	ns
t_{ETQX}[2,3]	$\overline{E}$n-controlled Output Enable time	3		ns
t_{ETQV}[3]	$\overline{E}$n-controlled access time		25	ns
t_{EFQZ}[1,2,4]	$\overline{E}$n-controlled output three-state time		10	ns

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Functional test.
2. Three-state is defined as a 500mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the falling edge of $\overline{E}$n. SEU immunity does not affect the read parameters.
4. The EF (enable false) notation refers to the rising edge of $\overline{E}$n. SEU immunity does not affect the read parameters.

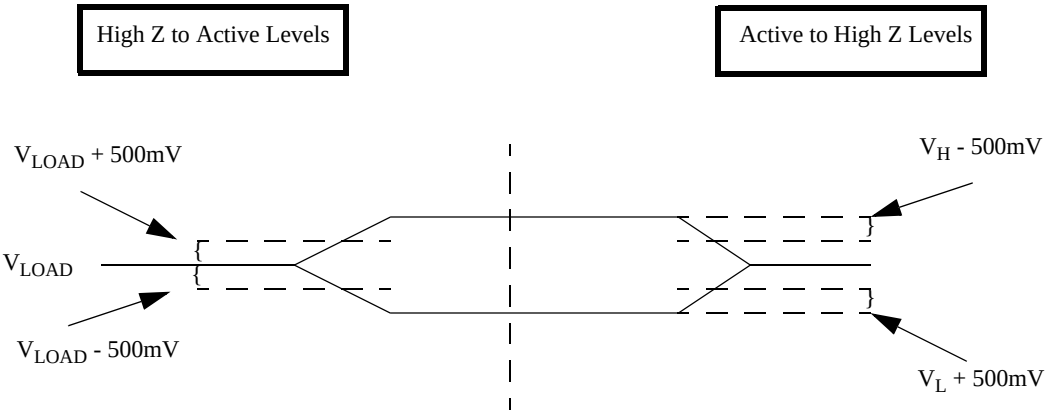
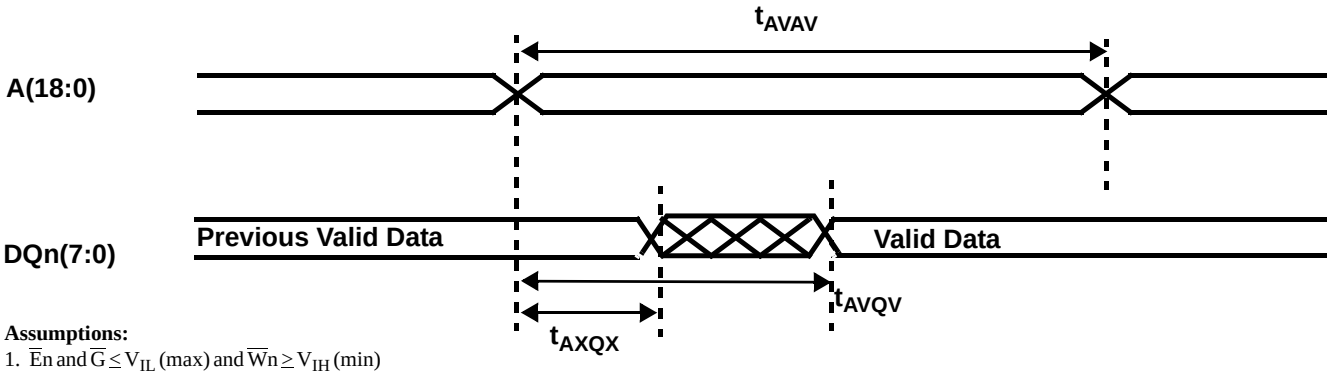
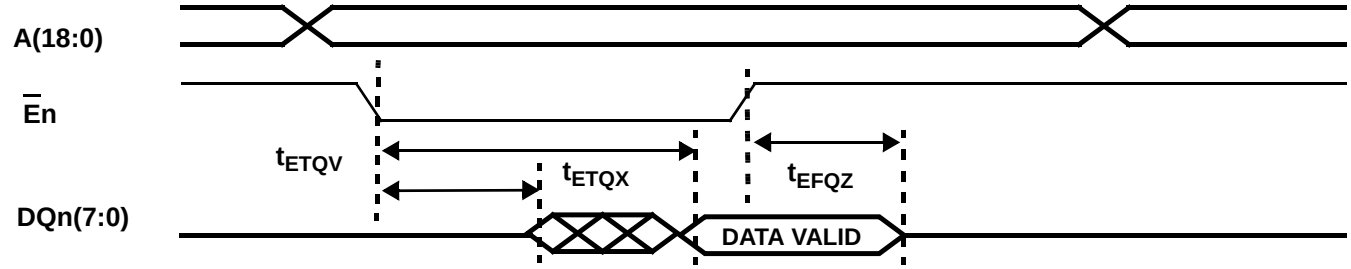


Figure 3. 5-Volt SRAM Loading



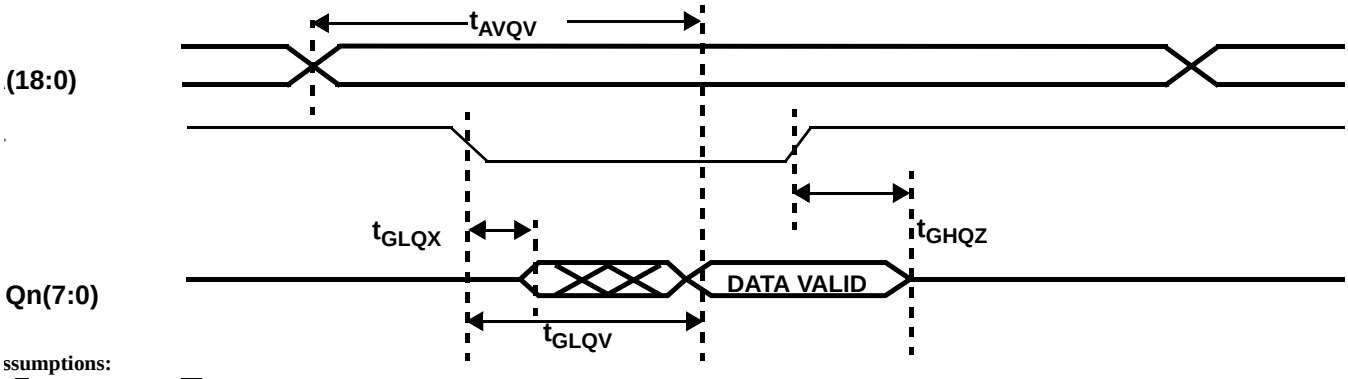
Assumptions:
1. $\overline{E}n$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W}n \geq V_{IH}$ (min)

Figure 4a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W}n \geq V_{IH}$ (min)

Figure 4b. SRAM Read Cycle 2: Chip Enable-Controlled Access



ssumptions:
$\overline{E}n \leq V_{IL}$ (max) and $\overline{W}n \geq V_{IH}$ (min)

Figure 4c. SRAM Read Cycle 3: Output Enable-Controlled Access

AC CHARACTERISTICS WRITE CYCLE (Pre/Post-Radiation)*

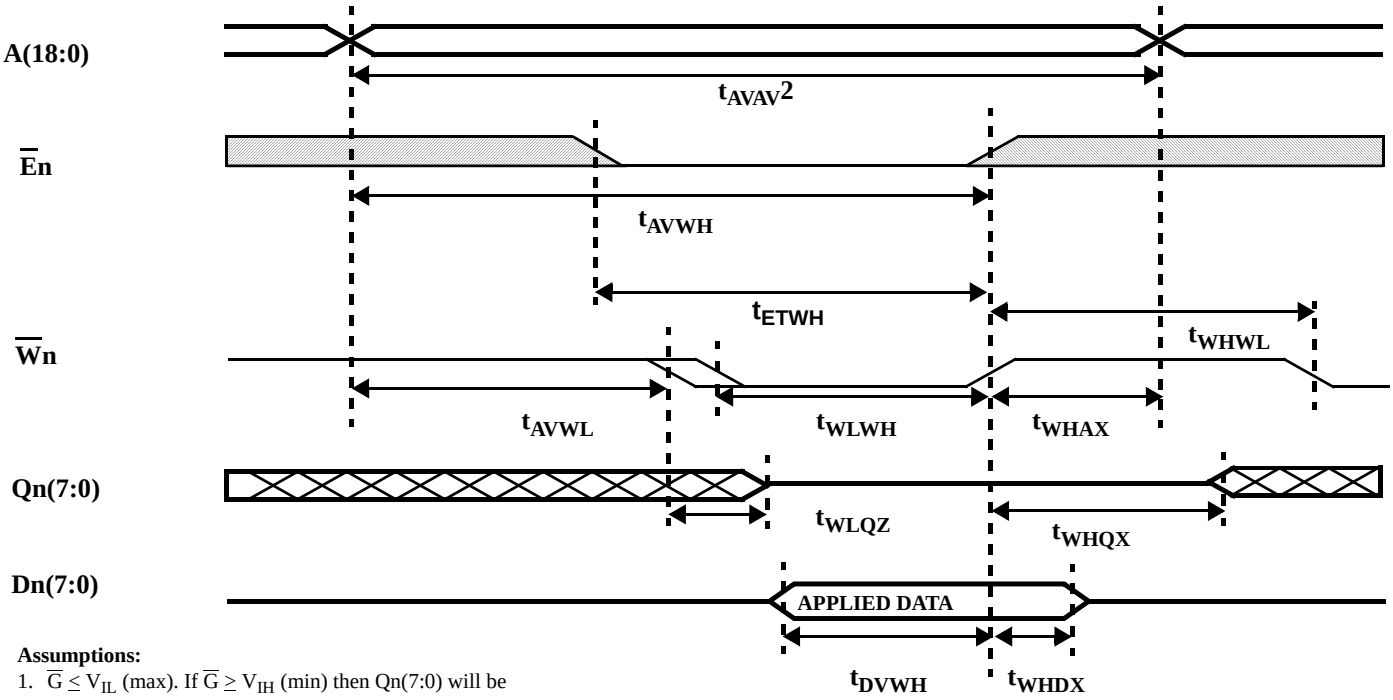
-40°C to +105°C (V_{DD} = 5.0V ± 10% for (W) screening)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}[1]	Write cycle time	25		ns
t_{ETWH}	Device Enable to end of write	20		ns
t_{AVET}	Address setup time for write ($\overline{E}$n - controlled)	1		ns
t_{AVWL}	Address setup time for write ($\overline{W}$n - controlled)	0		ns
t_{WLWH}	Write pulse width	20		ns
t_{WHAX}	Address hold time for write ($\overline{W}$n - controlled)	0		ns
t_{EFAX}	Address hold time for Device Enable ($\overline{E}$n - controlled)	0		ns
t_{WLQZ}[2]	$\overline{W}$n - controlled three-state time		10	ns
t_{WHQX}[2]	$\overline{W}$n - controlled Output Enable time	5		ns
t_{ETEF}	Device Enable pulse width ($\overline{E}$n - controlled)	20		ns
t_{DVWH}	Data setup time	15		ns
t_{WHDX}	Data hold time	2		ns
t_{WLEF}	Device Enable controlled write pulse width	20		ns
t_{DVEF}	Data setup time	15		ns
t_{EFDX}	Data hold time	2		ns
t_{AVWH}	Address valid to end of write	20		ns
t_{WHWL}[1]	Write disable time	5		ns

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

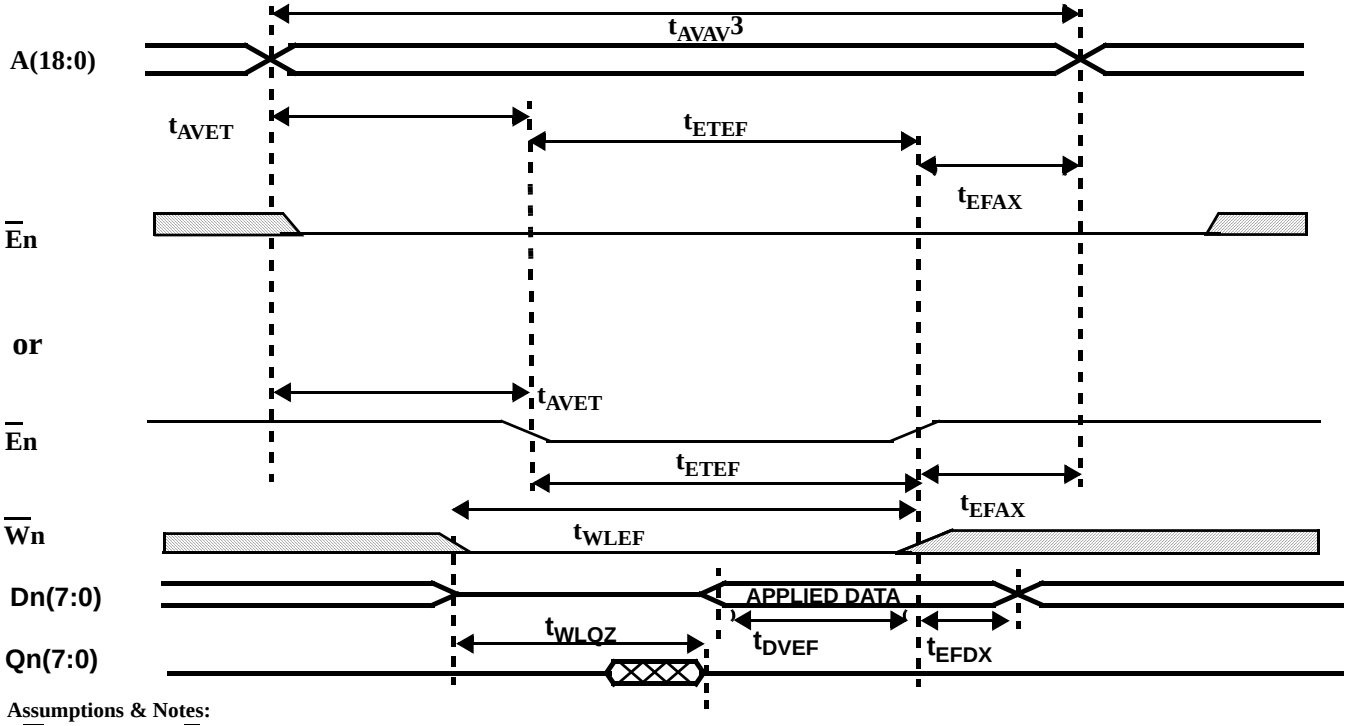
1. Functional test performed with outputs disabled ($\overline{G}$ high).
2. Three-state is defined as 500mV change from steady-state output voltage.



Assumptions:

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
2. $\overline{G}$ high for t_{AVAV} cycle.

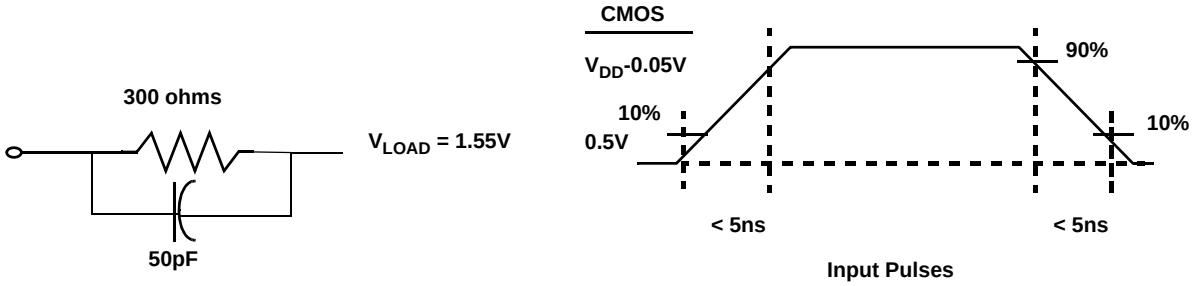
Figure 5a. SRAM Write Cycle 1: Write Enable - Controlled Access



Assumptions & Notes:

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
2. Either $\overline{E}n$ scenario above can occur.
3. $\overline{G}$ high for t_{AVAV} cycle.

Figure 5b. SRAM Write Cycle 2: Chip Enable - Controlled Access



Notes:

1. 50pF including scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = V_{DD}/2).

Figure 6. AC Test Loads and Input Waveforms

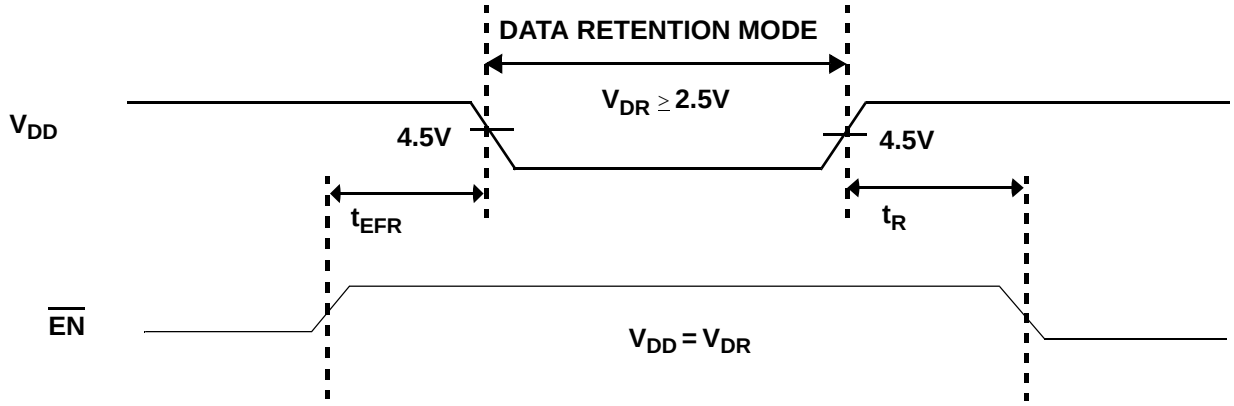


Figure 7. Low V_{DD} Data Retention Waveform

DATA RETENTION CHARACTERISTICS (Pre-Radiation) *($V_{DD2} = V_{DD2}$ (min), 1 Sec DR Pulse)

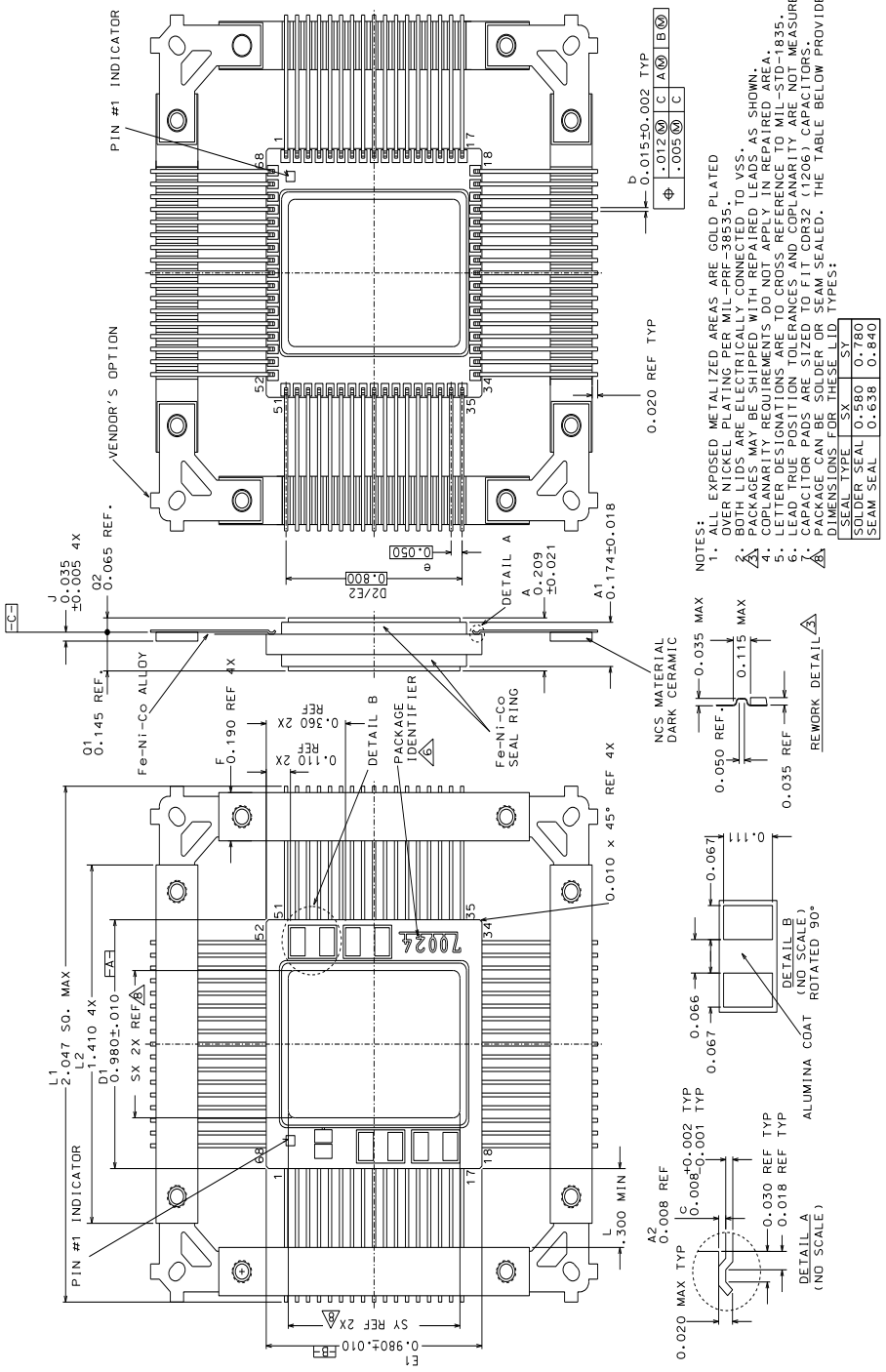
SYMBOL	PARAMETER	TEMP	MINIMUM	MAXIMUM	UNIT
V_{DR}	V_{DD1} for data retention	--	2.5	--	V
I_{DDR} [1]	Data retention current (per byte)	-40°C	--	9	mA
		25°C	--	9	mA
		105°C	--	24	mA
t_{EFR} [1]	Chip deselect to data retention time	--	0	--	ns
t_R [1]	Operation recovery time	--	t_{AVAV}	--	ns

Notes:

*****Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. $\overline{E}$ n= V_{DD} all other inputs = V_{DD} or V_{SS}

PACKAGING



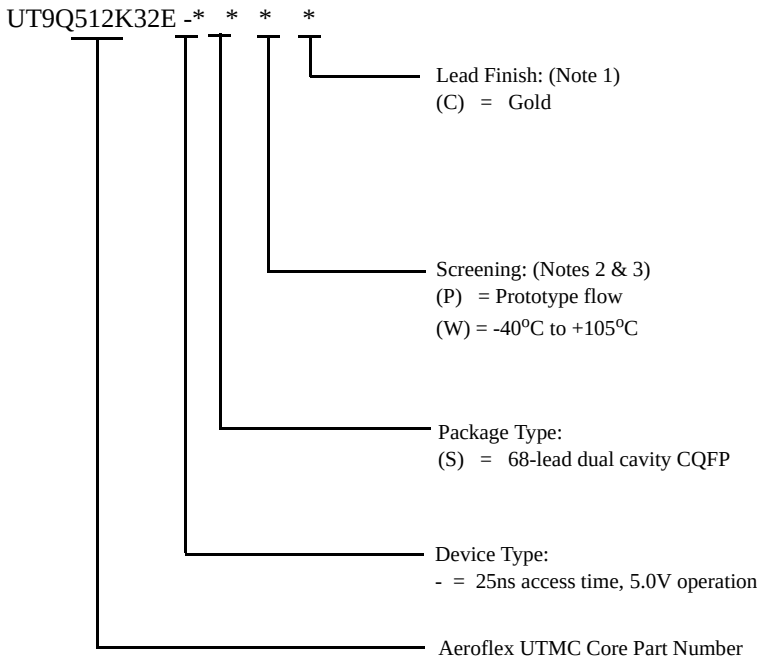
NOTES:
1. ALL EXPOSED METALIZED AREAS ARE GOLD PLATED OVER NICKEL PLATING PER MIL-PRF-38535.
2. BOTH LIDS ARE ELECTRICALLY CONNECTED TO VSS.
3. PACKAGES MAY BE SHIPPED WITH REPAIRED LEADS AS SHOWN.
4. COPLANARITY REQUIREMENTS DO NOT APPLY IN REPAIRED AREA.
5. LETTER DESIGNATIONS ARE TO CROSS REFERENCE TO MIL-STD-1835.
6. LEAD TRUE POSITION TOLERANCES AND COPLANARITY ARE NOT MEASURED.
7. CAPACITOR PADS ARE SIZED TO FIT CDR32 (1206) CAPACITORS.
8. PACKAGE CAN BE SOLDER OR SEAM SEALED. THE TABLE BELOW PROVIDES DIMENSIONS FOR THESE LID TYPES:

SEAL TYPE	5X	5Y
SOLDER SEAL	0.580	0.780
SEAM SEAL	0.638	0.840

Figure 8. 68-Lead Ceramic Quad Flatpack

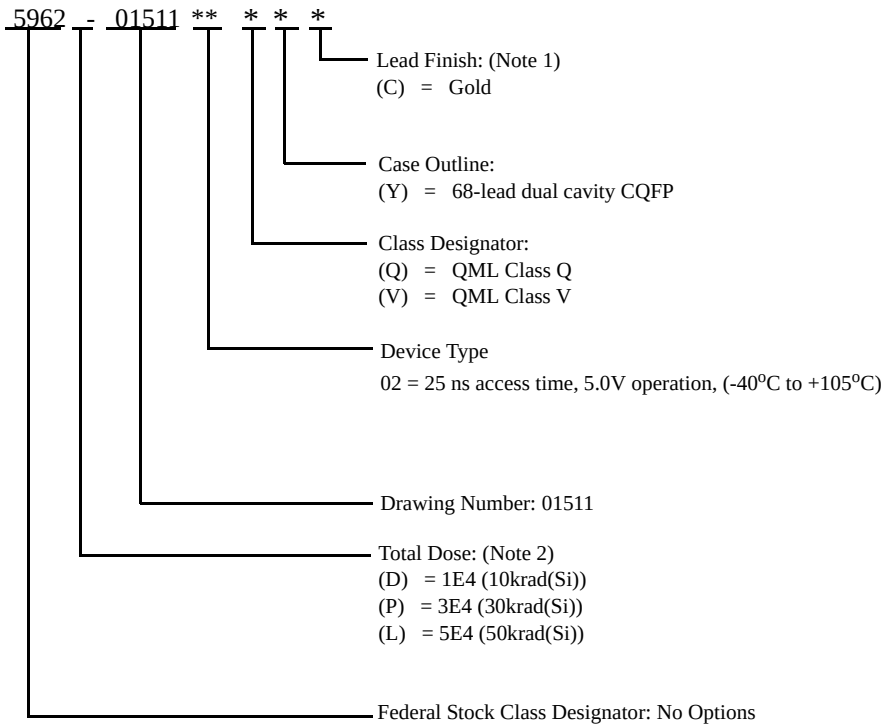
ORDERING INFORMATION

512K32 16Megabit SRAM MCM:



Notes:
1. Gold lead finish only.
2. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at 25°C. Radiation neither tested nor guaranteed.
3. Extended Industrial Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C to +105°C. Radiation neither tested nor guaranteed.

512K32E 16Megabit SRAM MCM: SMD



Notes:
1. Lead finish is "C" (Gold) only..
2. Total dose radiation must be specified when ordering.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

COLORADO
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Fax: 321-951-4254

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Fax: 949-362-2266

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Fax: 719-594-8468

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AEROFLEX
A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused

Low Power SRAM Read Operations

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number:*
4M Asynchronous SRAM	UT8R128K32	5962-03236	01 & 02	WC03
4M Asynchronous SRAM	UT8R512K8	5962-03235	01 & 02	WC01
16M Asynchronous SRAM	UT8CR512K32	5962-04227	01 & 02	MQ08
16M Asynchronous SRAM	UT8ER512K32	5962-06261	05 & 06	WC04/05
4M Asynchronous SRAM	UT8Q512E	5962-99607	05 & 06	WJ02
4M Asynchronous SRAM	UT9Q512E	5962-00536	05 & 06	WJ01
16M Asynchronous SRAM	UT8Q512K32E	5962-01533	02 & 03	QS04
16M Asynchronous SRAM	UT9Q512K32E	5962-01511	02 & 03	QS03
32M Asynchronous SRAM	UT8ER1M32	5962-10202	01 - 04	QS16/17
64M Asynchronous SRAM	UT8ER2M32	5962-10203	01 - 04	QS09/10
128M Asynchronous SRAM	UT8ER4M32	5962-10204	01 - 04	QS11/12
40M Asynchronous SRAM	UT8R1M39	5962-10205	01 & 02	QS13
80M Asynchronous SRAM	UT8R2M39	5962-10206	01 & 02	QS14
160M Asynchronous SRAM	UT8R4M39	5962-10207	01 & 02	QS15

* PIC = Aeroflex's internal Product Identification Code

1.0 Overview

The purpose of this application note is to discuss the Aeroflex SRAMs low power read architecture and to inform users of the affects associated with the low power read operations.

2.0 Low Power Read Architecture

The aforementioned Aeroflex designed SRAMs all employ an architecture which reduces power consumption during read accesses. The architecture internally senses data only when new data is requested. A request for new data occurs anytime the chip enable device pin is asserted, or any of the device address inputs transition states while the chip enable is asserted. A trigger is generated and sent to the sensing circuit anytime a request for new data is observed. Since several triggers could occur simultaneously, these triggers are wire-ORed to result in a single sense amplifier activity for the read request. This design method results in less power consumption than designs that continually sense data. Aeroflex's low power SRAMs listed above activate the sensing circuit for approximately 5ns whenever and access is requested, thereby, significantly reducing active power.

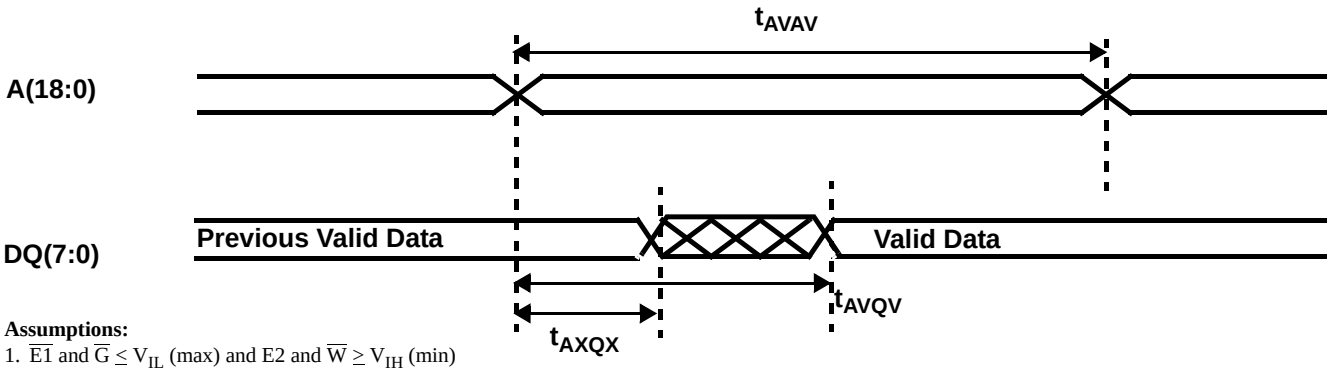
2.1 The SRAM Read Cycles.

The data sheets for all the devices noted in Table #1 discuss three methods for performing a read operation. The two most common methods for reading data are an Address Access and a Chip Enabled-Controlled Access. The third access discussed is the Output Enable-Controlled Access. The sequence at which control lines and address inputs are toggled determines which cycle is considered relevant. As discussed in section 2.0, an assertion of chip enable or any address transition while chip enable is asserted, initiates a read cycle. If the device chip enable is asserted prior to any address input transitions, then the read access is considered an Address Access. By keeping the device enabled and repeatedly switching address locations, the user retrieves all data of interest. A Chip Enable-Controlled Access occurs when the address signals are stable prior to asserting the chip enable. The Output Enabled-Controlled Access requires that either an Address Access or Chip Enable-Controlled Access has already been performed and the data is waiting for the Output Enable pin to assert, driving data to the device I/O pins.

The subsequent read cycle verbiage and diagrams are based on the Aeroflex UT8R512K8 data sheet. The number of control, input, and I/O pins will vary across the products listed in Table 1. The basic design family functionality for read operations is common among all the devices.

2.1.0 Address Access Read Cycle

The Address Access is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).



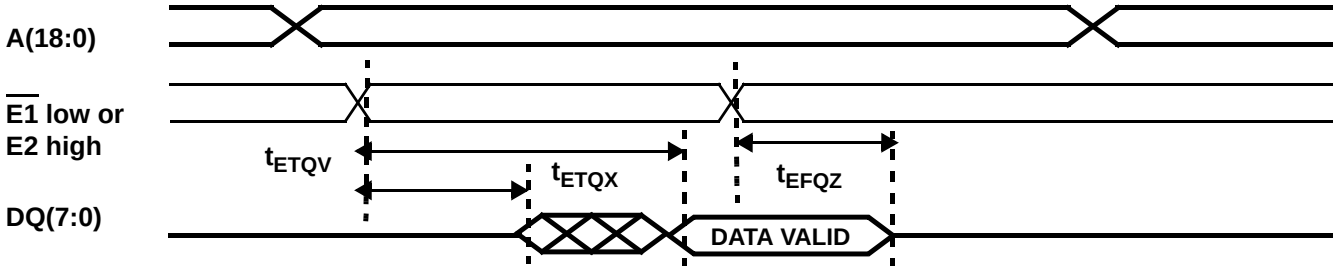
Assumptions:
1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max) and E2 and $\overline{W} \geq V_{IH}$ (min)

Note: No time references are relevant with respect to Chip Enable(s). Chip Enable(s) is assumed to be asserted.

SRAM Read Cycle 1: Address Access

2.1.1 Chip Enable-Controlled Read Cycle

The Chip Enable-controlled Access is initiated by $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).



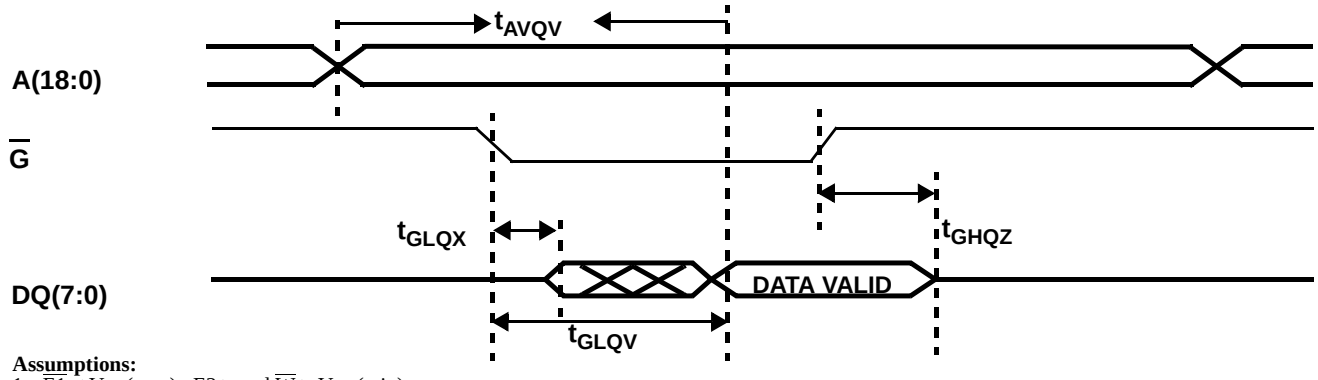
Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Note: No specification is given for address set-up time with respect to chip enable assertion. The read cycle description states that addresses are to remain stable for the entire cycle. Address set-up time relative to chip enable is assumed to be 0ns minimum.

SRAM Read Cycle 2: Chip Enable Access

2.1.1 Output Enabled-Controlled Read Cycle

The Output Enable-controlled Access is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.



Assumptions:
1. $\overline{E1} \leq V_{IL}$ (max) , E2 > and $\overline{W} \geq V_{IH}$ (min)

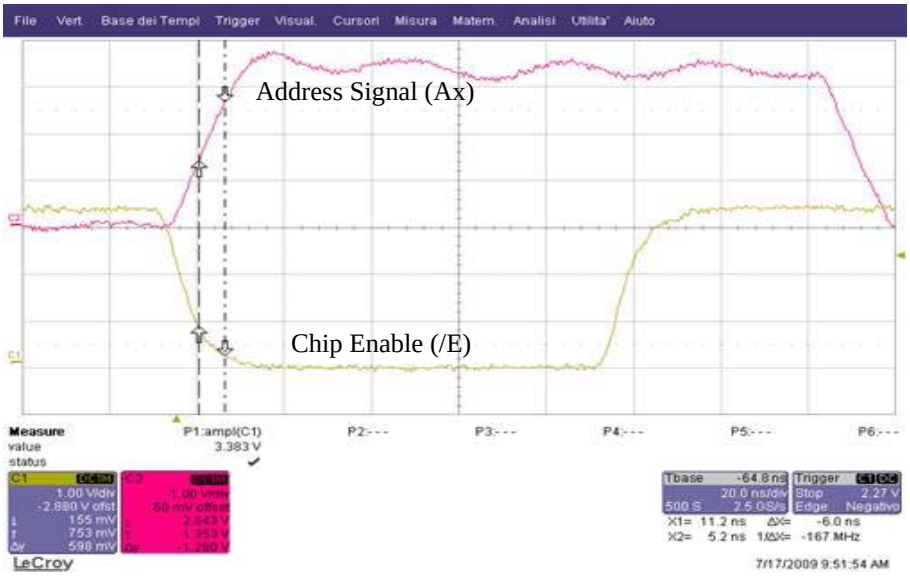
SRAM Read Cycle 3: Output Enable Access

3.0 Low Power Read Architecture Timing Consideration

The low power read architecture employed by Aeroflex designed SRAMs results in significant power reduction, especially in applications with longer than minimum read cycle times. However, this type of architecture is responsive to excessive input signal skew when device addressing and chip enable assertion occur simultaneously. Signal skew of greater than 4-5ns between all of the read triggering activities is sufficient to start another read cycle.

3.1 Simultaneous Control and Address Switching

Simultaneous switching of controls and address pins, alone, is not a problem; excessive skew between them is the concern. Consider the application where several SRAM devices are connected to the same memory bus. The address bus is commonly connected to all the devices, but the chip enable pin is singularly connected to each individual SRAM. This configuration results in a loading difference between the address inputs and the chip enable. This lightly loaded chip enable propagates to the memory more quickly than the heavily loaded address lines. The oscilloscope capture of Figure #1 is the actual timing of an application which had intermittent data errors due to address transitions lagging chip enable.



- Timing shown from VIL (yellow trace /CS) and VIH (pink for address signal) as delta X = 6ns. Even at actual internal gate switching point (~ VDD/2), the skew is still around 6ns.

Figure #1 SRAM Signal Capture

The signal transitions in the scope plot of Figure #1 appear to be fairly coincidental. A closer look however, reveals the chip enable signal actually starts and reaches V_{IL} approximately 6ns before the address signal reaches V_{IH}. Even at one half V_{DD} (closer to actual logical gate switching of the inputs), the delta in signal times is still approximately 6ns.

Simultaneous switching of controls and address inputs is not recommended for a couple of reasons. The first is the previously described signal skew sensitivity between controls and/or address inputs. The second reason is that activating all the controls and address inputs simultaneously results in peak instantaneous current consumption. This condition causes maximum strain to the power decoupling. Chip Enable activates address decoding circuits, address switching introduces input buffer switching current, and output enable assertion turns on all the device output drivers. Peforming all three simultaneously results in worst case transient current demand by the memory.

3.1.0 Technical Overview of Skew Sensitivity

Recall from section 2.0 that any activity requesting new data causes a read trigger. The triggers are wire-ORed together. In order to meet the faster access times demanded by today's applications, the ORed trigger only exists during the first 4-5ns of the read cycle. Since the slowest of the address transitions occurs more than 5ns after the initiation of the read activity, a second read activity is initiated. The sensing circuit does not have time to normalize before the second read activity has started. For this reason a Chip Enable-Controlled read cycle requires that address inputs remain stable for the entire cycle. Infrequent and random sensing errors can result if the bit columns are continually pulled to one state then quickly requested to sense the opposite state. Another effect of the low power read architecture that differs from previous generation designs (those that continually sense for data) is that the bit line will not be sensed again until another read triggering event occurs. If another read trigger event (chip enable assertion and/or address change) does no occur for a particular address, the incorrect data remains at the outputs.

4.0 Summary and Conclusion

The Aeroflex SRAMs in Table #1 all employ a low power consumption read architecture. Power is conserved by sensing data only when new data is requested. A request occurs anytime chip enable is asserted or any address input signal transitions while chip enable is asserted. The data sheets for the SRAMs listed in Table #1 do not explicitly define the case of simultaneous switching of address and control signals during read operations. Data sheet read cycle descriptions indicate that control inputs are established prior to address changes, and address inputs are stable prior to control assertions. Simultaneous switching of addresses and controls is tolerable, when the skew between all input signals is < 4ns. For designs that must employ the simultaneous activation of address and control signals, two important issues should be considered by the designer. The first is the input signal skew sensitivity of the low power read architecture discussed by this application note. The second is the instantaneous current consumption that results from simultaneous access methods. Aeroflex recommends the use of only one read access method at a time. If multiple read accesses (simultaneous chip enable assertion and address switching) cannot be avoided, then Aeroflex recommends that the chip enable signal be delayed until all addresses have completed transitions.