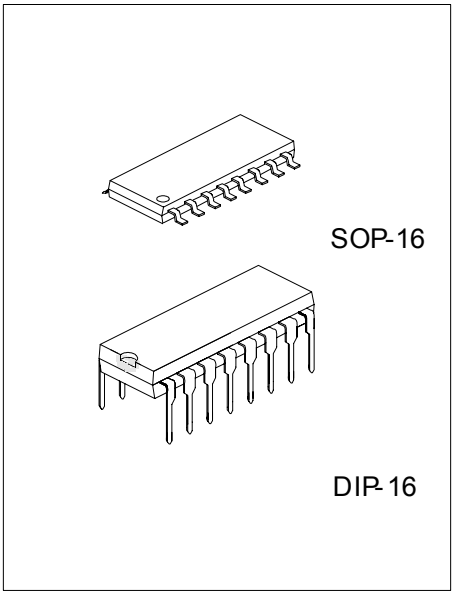
REGULATING PWM IC



*Pb-free plating product number: U3525G

■ DESCRIPTION

The UMW UTC3525 is a pulse width modulator IC and designed for switching power supplies application to improve performance and reduce external parts usage.

A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The output stage features NOR logic, giving a LOW output for an OFF state. An under-voltage lockout circuitry, which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages, includes approximately 500 mV of hysteresis for jitter free operation. The PWM circuits also feature a latch following the comparator. When a PWM pulses has been terminated, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA.

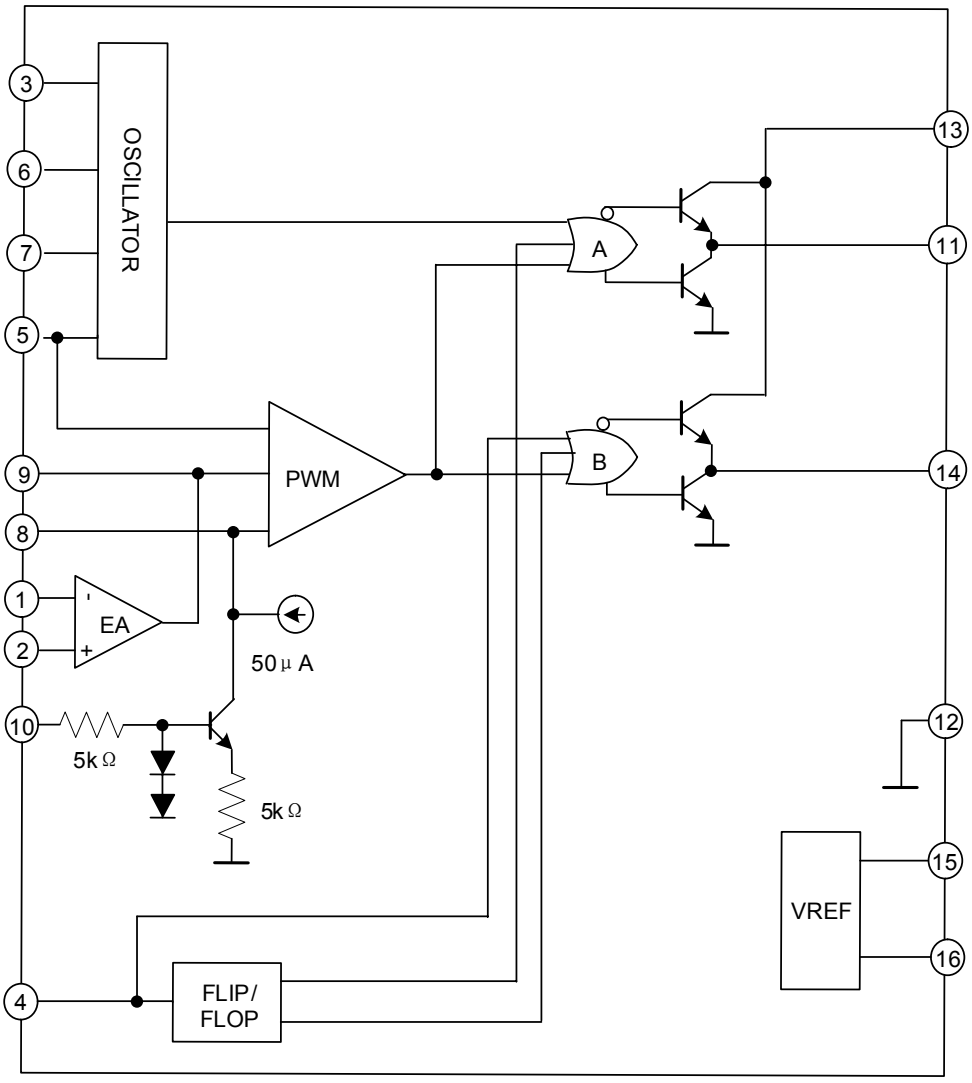
■ FEATURES

* Input Voltage: 8~35V
* On-chip +5.1V reference is trimmed to ±1%
* 100HZ ~ 500KHZ oscillator range
* Separate oscillator sync terminal
* Adjustable dead time control
* Internal soft-start
* Pulse-by-pulse shutdown
* Input under-voltage lockout with hysteresis
* Latching PWM to prevent multiple pulses
* Dual source/sink output drivers

■ ORDERING INFORMATION

Order Number		Package	Packing
Normal	Halogen Free		
U3525	U3525LG	DIP-16	Tube
U3525S	U3525G	SOP-16	Tape Reel
U3525S	U3525G	SOP-16	Tube

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)						
Output Low Level				0.2	0.5	V
Output High Level			3.8	5.6		V
Input Offset Voltage	V_{OS}			2	10	mV
Input Bias Current	I_b			1	10	μA
Input Offset Current	I_{os}				1	μA
Comm. Mode Reject.	CMR	V_{CM} = 1.5 ~ 5.2 V	60	75		dB
Supply Voltage Rejection	PSR	V_{IN} = 8 ~ 35 V	50	60		dB
DC Open Loop Gain		R_L ≥10 MΩ	60	75		dB
DC Transconduct. (Note 1, 3)		30 KΩ ≤R_L≤1 MΩ, T_J = 25℃	1.1	1.5		ms
Gain Bandwidth Product (Note 1)		Gv = 0 dB, T_J = 25℃	1	2		MHz
PWM COMPARATOR						
Input Threshold (Note 2)		Zero Duty-cycle	0.7	0.9		V
		Maximum Duty-cycle		3.3	3.6	V
Input Bias Current (Note 1)				0.05	1	μA
Minimum Duty-cycle					0	%
Maximum Duty-cycle (Note 2)			45	49		%
SHUTDOWN SECTION						
Soft Start Low Level		V_{SD} = 2.5 V		0.4	0.7	V
Shutdown Threshold		To outputs, V_{SS} = 5.1 V, T_J = 25℃	0.6	0.8	1	V
Shutdown Input Current		V_{SD} = 2.5 V		0.4	1	mA
Soft Start Current		V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	μA
Shutdown Delay (Note 1)		V_{SD} = 2.5 V, T_J = 25℃		0.2	0.5	μs
OUTPUT DRIVERS (each output) (V_C = 20 V)						
Output Low Level		I_{SINK} = 20 mA		0.2	0.4	V
		I_{SINK} = 100 mA		1	2	V
Output High Level		I_{SOURCE} = 20 mA	18	19		V
		I_{SOURCE} = 100 mA	17	18		V
Under-Voltage Lockout		V_{COMP} and V_{SS} = High	6	7	8	V
Collector Leakage	I_C	V_C = 35 V			200	μA
Rise Time (Note 1)	t_R	C_L = 1 nF, T_J = 25 °C		100	600	ns
Fall Time (Note 1)	t_F	C_L = 1 nF, T_J = 25 °C		50	300	ns
TOTAL STANDBY CURRENT						
Supply Current	I_S	V_{IN} = 35 V		14	20	mA

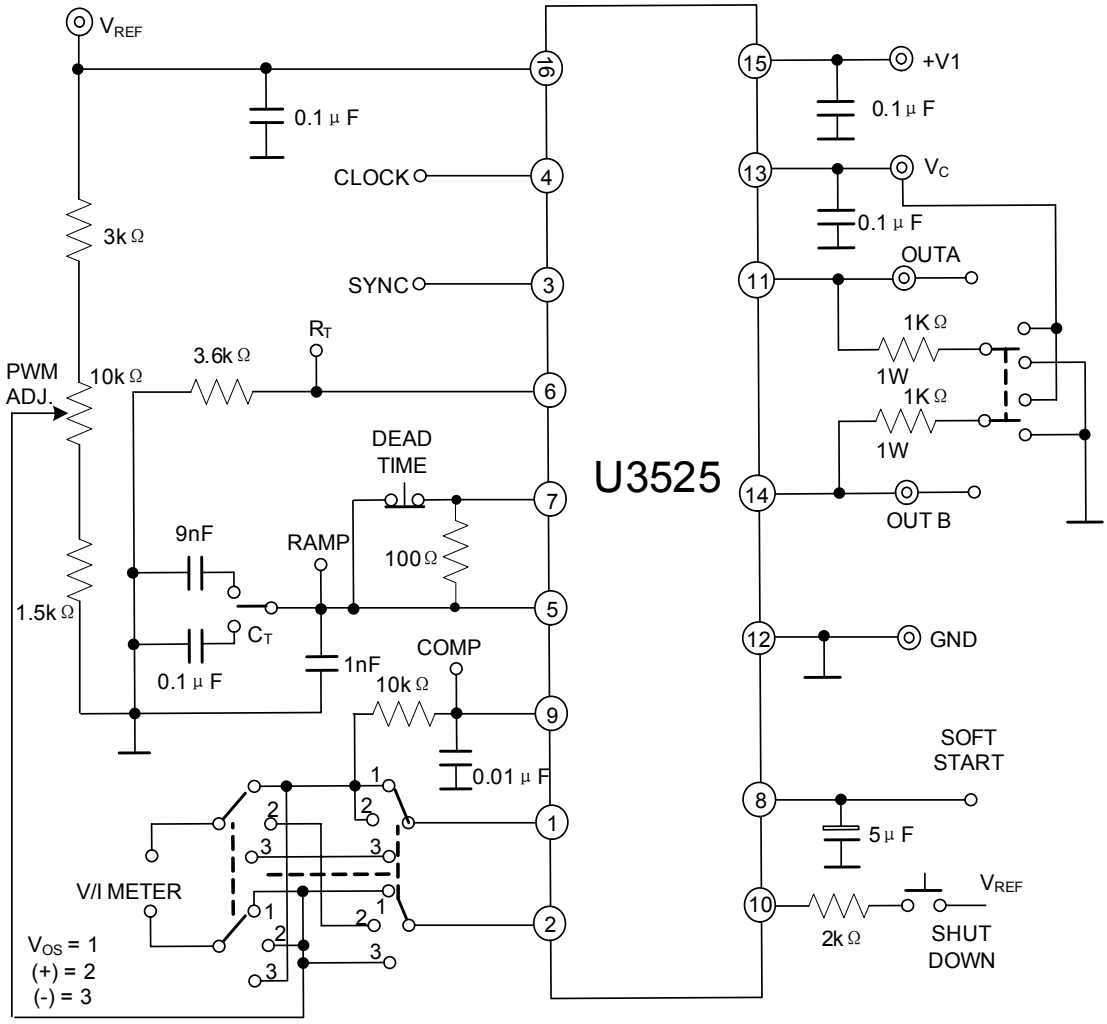
Note:1.The parameters are not 100% tested in production.

2.Tested at fosc=40 KHz (R_T=3.6 KΩ, C_T=10nF, R_D=0 Ω). Approximate oscillator frequency is defined by :

$$f = \frac{1}{C_T(0.7R_T + 3R_D)}$$

3.DC transconductance (g_M) relates to DC open-loop voltage gain (G_V) according to the following equation: G_V=g_M R_L where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_V when the error amplifier output is loaded.

■ TEST CIRCUIT



■ APPLICATION INFORMATION AND CIRCUIT

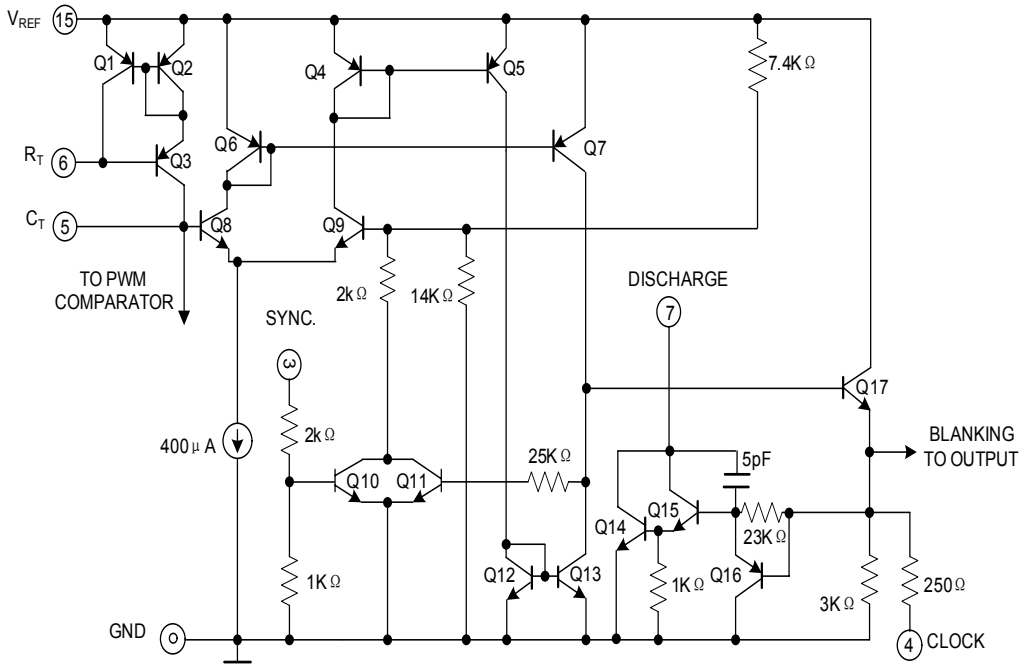
SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

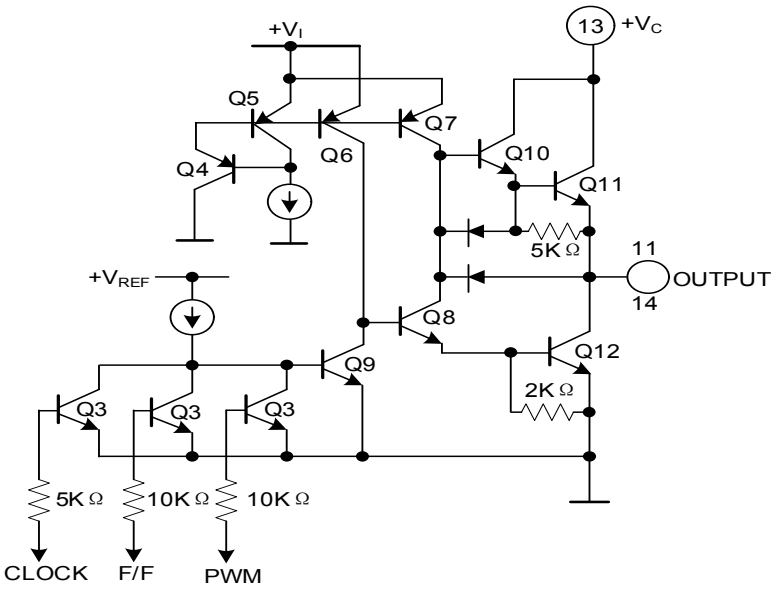
Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

OSCILLATOR SCHEMATIC

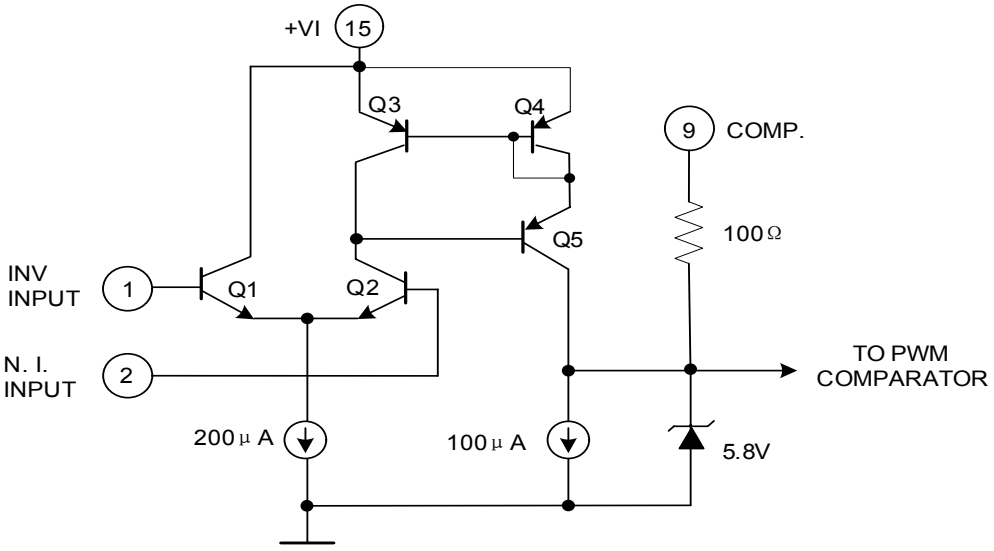


■ APPLICATION INFORMATION AND CIRCUIT(Cont.)

OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)

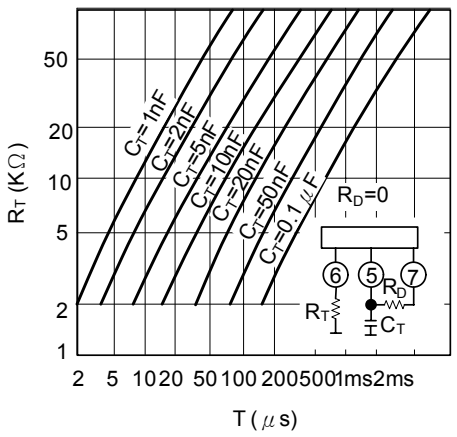


ERROR AMPLIFIER

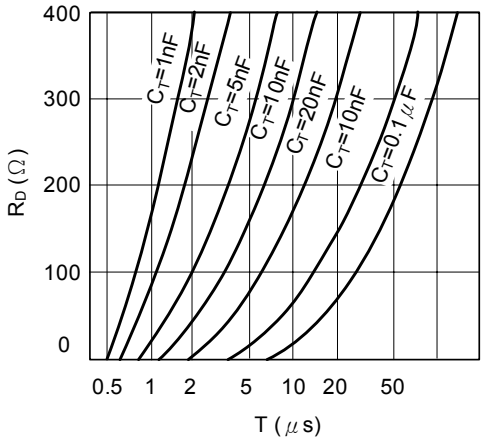


■ TYPICAL CHARACTERISTICS

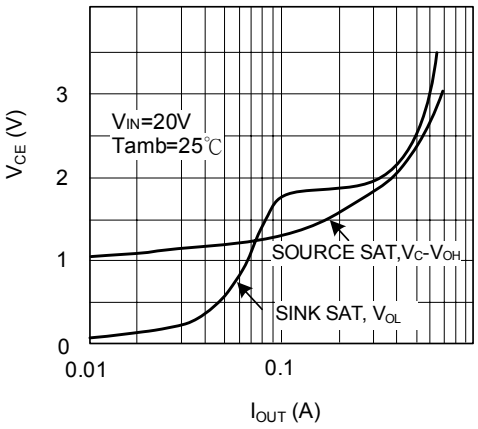
Oscillator Charge Time vs. R_T and C_T



Oscillator DisCharge Time vs. R_D and C_T



Output Saturation Characteristics



Error Amplifier Voltage Gain and Phase vs Frequency