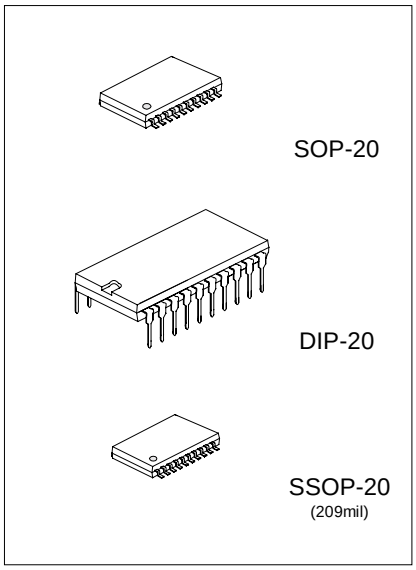
UTC 75232 LINEAR INTEGRATED CIRCUIT

MULTIPLE RS-232 DRIVERS AND RECEIVERS



DESCRIPTION

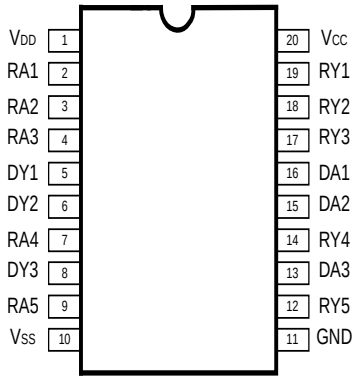
The UTC 75232 complies with the requirements of the TIA/EIA232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20kbit/s. The switching speeds of the UTC 75232 are fast enough to support rates up to 120kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates to 120kbit/s, use of ANSI ITA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards are recommended.

The UTC 75232 is Characterized for operation over the temperature range of 0°C to 70°C.

FEATURES

*Single chip with easy interface between UART and Serial-Port Connector of IBM™, PC/AT™ and Compatibles.
*Meets or Exceeds the Requirements of ANSI Standard TIA/EIA-232-F and ITU Recommendation V.28
*Designed to support data rates up to 120 kbit/s
*ESD Protection to 2kV on Bus Terminals

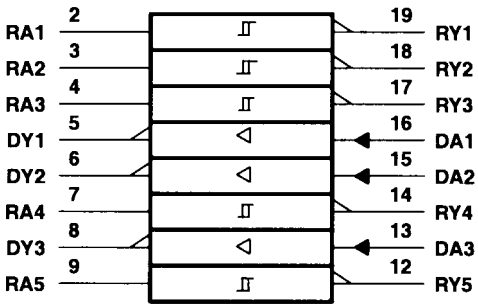
PIN CONFIGURATIONS



PIN DESCRIPTION

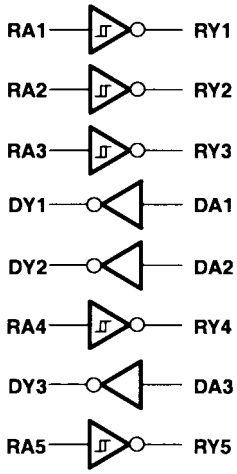
PIN NO	SYMBOL	NAME AND FUNCTION
1	V_{DD}	Supply Voltage
2	RA1	First Receiver Input
3	RA2	Second Receiver Input
4	RA3	Third Receiver Input
5	DY1	First Driver Output
6	DY2	Second Driver Output
7	RA4	Fourth Receiver Input
8	DY3	Third Driver Output
9	RA5	Fifth Receiver Input
10	V_{SS}	Supply Voltage
11	GND	Ground
12	RY5	Fifth Receiver Output
13	DA3	Third Driver Input
14	RY4	Fourth Receiver Output
15	DA2	Second Driver Input
16	DA1	First Driver Input
17	RY3	Third Receiver Output
18	RY2	Second Receiver Output
19	RY1	First Receiver Output
20	V_{CC}	Supply Voltage

LOGIC SYMBOL AND LOGIC DIAGRAM

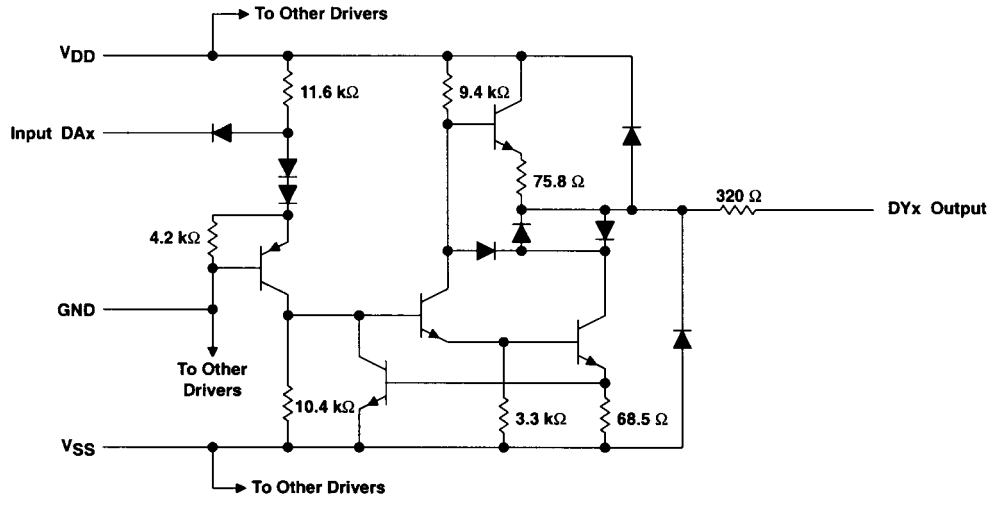


This symbol is in accordance with ANSI/IEEE std 91-1984

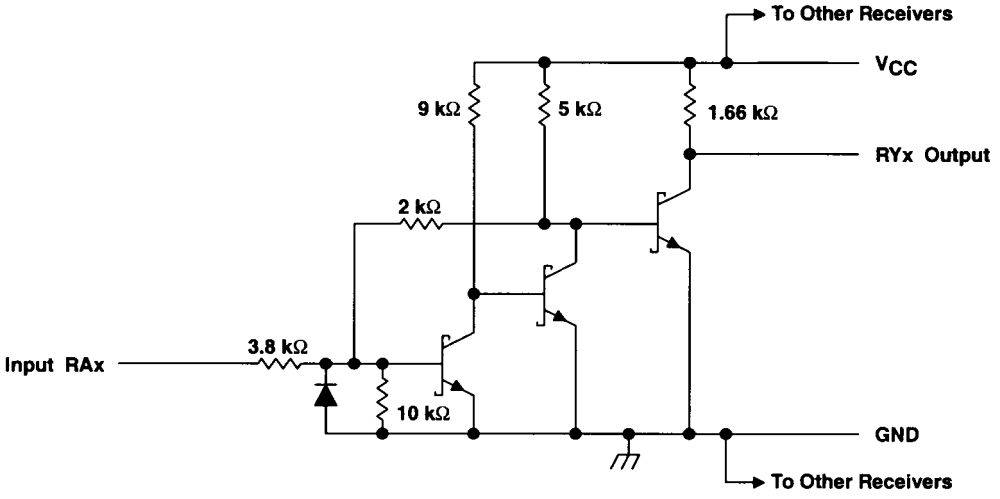
and IEC Publication 617-12



CIRCUIT OF DRIVERS (Resistor value shown are nominal.)



CIRCUIT OF EACH RECEIVER (Resistor value shown are nominal.)



ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage (Note 1)	V_{DD}	15	V
Supply voltage (Note 1)	Vss	-15	V
Supply voltage (Note 1)	Vcc	10	V
Input voltage range (DRIVER)	V_I	-15 to 7	V
Input voltage range (RECEIVER)	V_I	-30 to 30	V
Driver output voltage range	Vo	-15 to 15	V
Receiver low level output current	Io	20	mA
Thermal impedance (note 2) SSOP-20 SOP-20 DIP-20	θ_{JA}	 115 97 67	°C/W
Storage temperature range	Tstg	-65 to +150	°C
Lead temperature 1.6mm from case for 10 sec	T_L	260	°C

Note 1: All voltage are with respect to the network ground terminal.

Note 2: The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{DD}	7.5	9	15	V
Supply voltage	V_{SS}	-7.5	-9	-15	V
Supply voltage	V_{CC}	4.5	5	5.5	V
High level input voltage (driver only)	V_{IH}	1.9			V
Low level input voltage (driver only)	V_{IL}			0.8	V
High level output current DRIVER RECEIVER	I_{OH}			 -6.0 -0.5	mA
Low level output current DRIVER RECEIVER	I_{OL}			 6 16	mA
Operating free-air temperature	T_A	0		70	°C

SUPPLY CURRENTS

PARAMETER	SYMBOL	TEST CONDITIONS	V_{DD}	Vss	MIN	MAX	UNIT
Supply current from V_{DD}	I_{DD}	No load. All inputs at 1.9V	9	-9		15	mA
			12	-12		19	
			15	-15		25	mA
		No load. All inputs at 0.8V	9	-9		4.5	
			12	-12		5.5	
			15	-15		9	
Supply current from Vss	Iss	No load. All inputs at 1.9V	9	-9		-15	mA
			12	-12		-19	
			15	-15		-25	
		No load. All inputs at 0.8V	9	-9		-3.2	mA
			12	-12		-3.2	
			15	-15		-3.2	
Supply current from Vcc	Icc	No load. All inputs at 5V, Vcc=5V				30	mA

DRIVER ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (V_{DD}=9V, Vss=-9V, Vcc=5V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High level output voltage	V_{OH}	V_{IL}=0.8V, R_L=3 kΩ (Figure 1)	6	7.5		V
Low level output voltage (note 3)	V_{OL}	V_{IH}=1.9V, R_L=3 kΩ (Figure 1)		-7.5	-6	V
High level input current	I_{IH}	V_I=5V (Figure 2)			10	μA
Low level input current	I_{IL}	V_I=0V (Figure 2)			-1.6	mA
High level short circuit output current (note 4)	$I_{OS(H)}$	V_{IL}=0.8V, V_O=0V(Figure 1)	-4.5	-12	-19.5	mA
Low level short circuit output current	$I_{OS(L)}$	V_{IH}=2V, Vo=0V(Figure 1)	4.5	12	19.5	mA
Output resistance (note 5)	r_O	V_{DD}=Vss=Vcc=0V Vo=-2 to 2V	300			Ω

Note 3: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this datasheet for logic levels only (e.g. if -10V is a maximum, the typical value is a more negative voltage).
Note 4: Output short circuit conditions must maintain the total power dissipation below absolute maximum ratings.
Note 5: Test conditions are those specified by TIA/EIA232-F and as listed above.

DRIVER SWITCHING CHARACTERISTICS (V_{DD}=12V, Vss=-12V, Vcc=5V, T_A=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time, low to high level output	t_{PLH}	R_L=3 to 7 kΩ, C_L=15pF (Figure 3)		315	500	ns
Propagation delay time, high to low level output	t_{PHL}	R_L=3 to 7 kΩ, C_L=15pF (Figure 3)		75	175	ns
Transition time, low to high level output	t_{TLH}	R_L=3 to 7 kΩ, C_L=15pF (Figure 3)		60	100	ns
		R_L=3 to 7 kΩ, C_L=2500pF (Note 6, Figure 3)		1.7	2.5	μs
Transition time high to low level output	t_{THL}	R_L=3 to 7 kΩ, C_L=15pF (Figure 3)		40	75	ns
		R_L=3 to 7 kΩ, C_L=2500pF (Note 7, Figure 3)		1.5	2.5	μs

Note 6: Measured between -3V and 3V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied.
Note 7: Measured between 3V and -3V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied.

RECEIVER ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (T_A=25°C, Vcc=5V, V_{DD}=9V, Vss=-9V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Positive going threshold voltage	V_{T+}	(Figure 5) T_A=25°C T_A=0°C to 70°C		 1.75 1.55	 1.9	 2.3 2.3	V
Negative going threshold voltage	V_{T-}			0.75	0.97	1.25	V
Input hysteresis(V_{T+} - V_{T-})	Vhys			0.5			V
High level output voltage	V_{OH}	I_{OH}=-0.5mA	V_{IH}=0.75V	2.6	4	5	V
			Inputs Open	2.6			
Low level output voltage	V_{OL}	V_I=3V, I_{OL}=10mA			0.2	0.45	V
High level input current	I_{IH}	V_I=25V (Figure 5)		3.6		8.3	mA
		V_I=3V (Figure 5)		0.43			
Low level input current	I_{IL}	V_I=-25V (Figure 5)		-3.6		-8.3	mA
		V_I=-3V (Figure 5)		-0.43			
Short-circuit output current	Ios	(Figure 4)			-3.4	-12	mA

RECEIVER SWITCHING CHARACTERISTICS (V_{DD}=12V, Vss=-12V, Vcc=5V, T_A=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time, low to high level output	t_{PLH}	R_L=5 kΩ, C_L=50pF (Figure 6)		107	250	ns
Propagation delay time, high to low level output	t_{PHL}			42	150	ns
Transition time low to high level output	t_{TLH}			175	350	ns
Transition time high to low level output	t_{THL}			16	60	ns
Propagation delay time, low to high level output	t_{PLH}	R_L=1.5 kΩ, C_L=15pF (Figure 6)		100	160	ns
Propagation delay time, high to low level output	t_{PHL}			60	100	ns
Transition time low to high level output	t_{TLH}			90	175	ns
Transition time high to low level output	t_{THL}			15	50	ns

Figure 1. Driver test circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, $I_{OS(L)}$

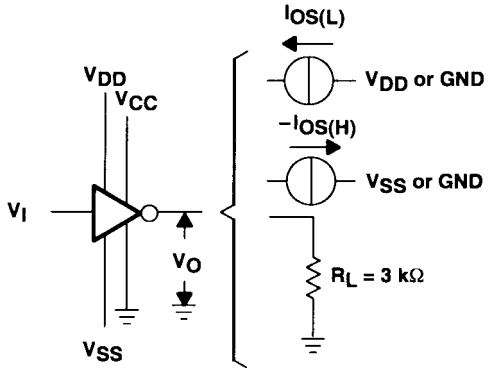


Figure 2. Driver test circuit for I_{IH}, I_{IL}

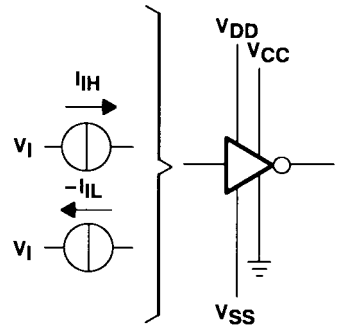
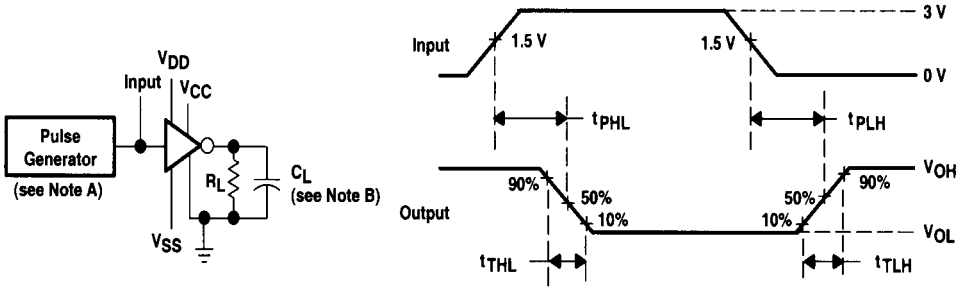


Figure 3. Driver test circuit and voltage waveforms



Note 1. The pulse generator has the following characteristics: tw=25μs, PRR=20kHz, Zo=50Ω, tr=tf<50ns.
Note 2. C_L includes probe and jig capacitance.

Figure 4. Receiver test circuit for I_{OS}

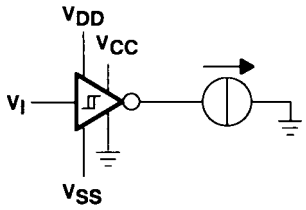


Figure 5. Receiver test circuit for V_T, V_{OH}, V_{OL}

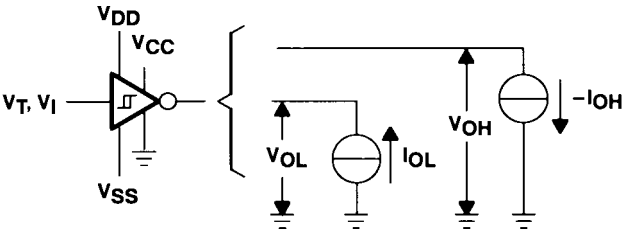
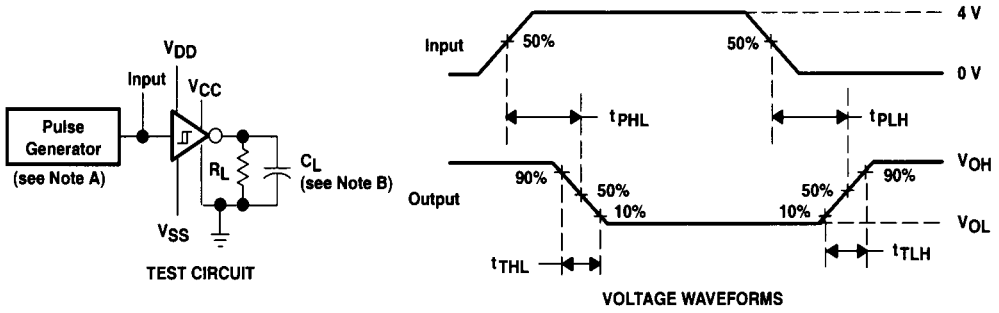


Figure 6. Receiver propagation and transition times



Note 1. The pulse generator has the following characteristics: tw=25μs, PRR=20kHz, Zo=50Ω, tr=tf<50ns.
Note 2. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS (DRIVER)

VOLTAGE TRANSFER CHARACTERISTICS

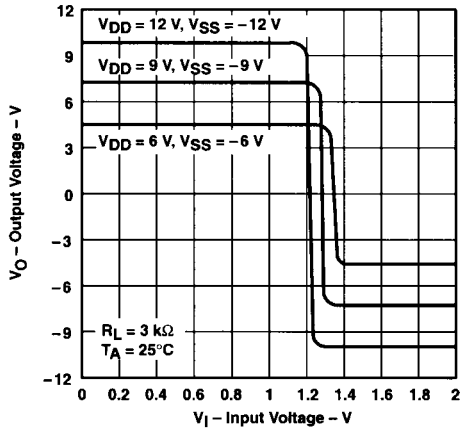


Figure 7

OUTPUT CURRENT vs OUTPUT VOLTAGE

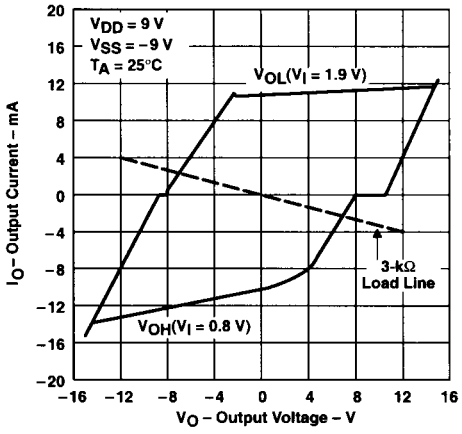


Figure 8

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

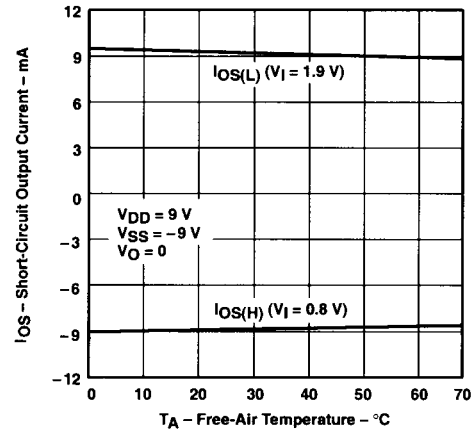


Figure 9

SLEW RATE vs LOAD CAPACITANCE

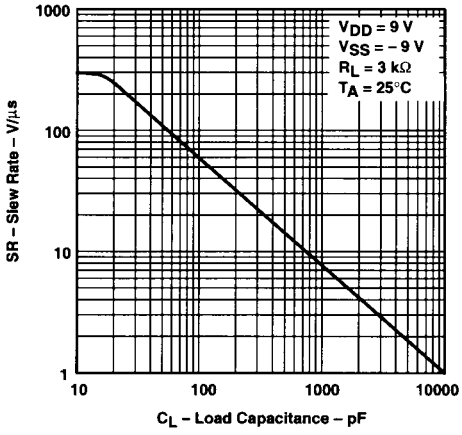


Figure 10

TYPICAL CHARACTERISTICS (RECEIVER)

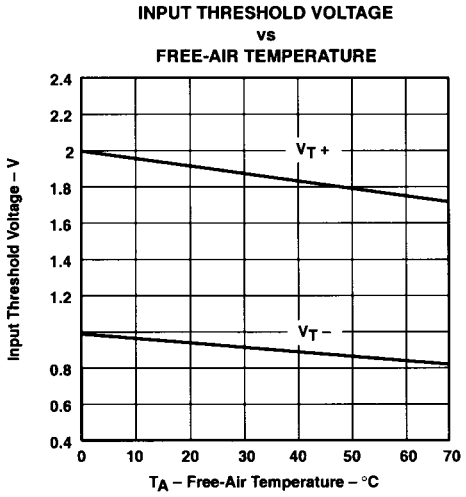


Figure 11

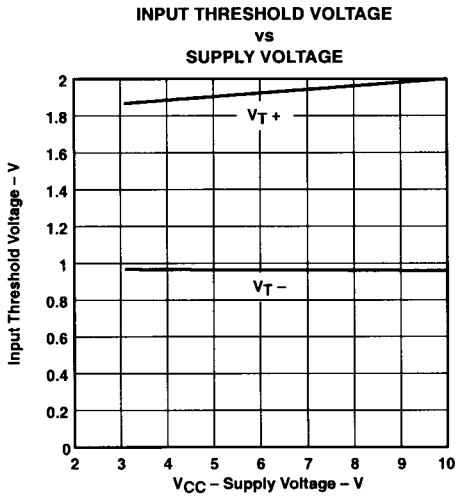
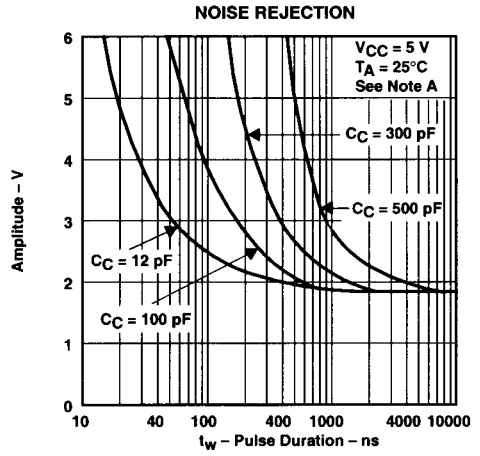


Figure 12



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 13

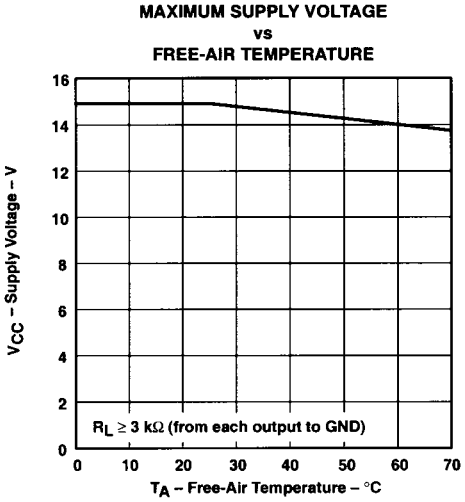


Figure 14

APPLICATION INFORMATION

Figure 15. Power-Supply protection to meet Power-Off fault conditions of TIA/TIA-232-F

Diodes placed in series with the V_{DD} and V_{SS} leads protect the UTC 75185 in the fault condition in which the device outputs are shorted to ±15V and the power supplies are at low and provide low-impedance paths to ground.

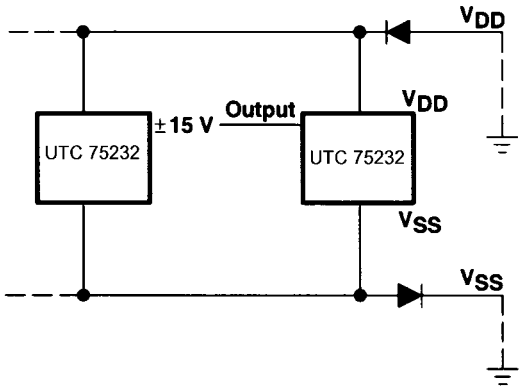


Figure 16. Typical Connection

"†" : See Figure 10 to select the correct values for the loading capacitors (C1, C2, and C3), which are required to meet the RS-232 maximum slew-rate requirement of 30V/μs. The value of the loading capacitors required depends upon the line length and desired slew rate, but typically is 330 pF.