



UTN6266

Power MOSFET

30A, 60V N-CHANNEL TRENCH MOSFET

DESCRIPTION

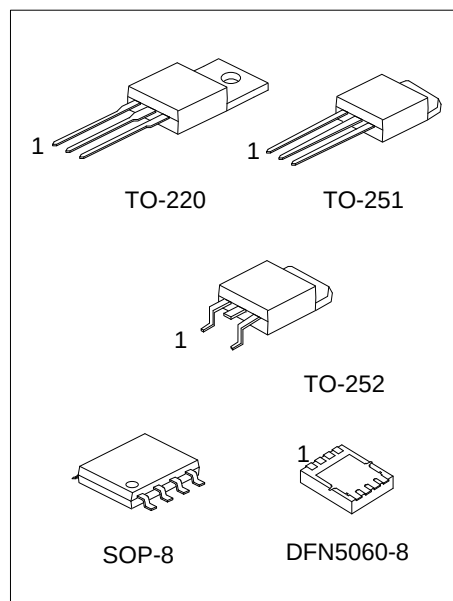
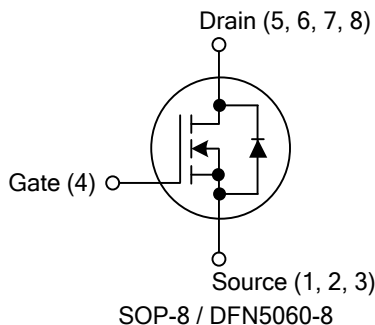
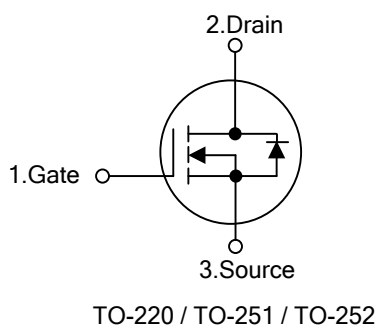
The UTC **UTN6266** is a N-Channel trench mosfet, it uses UTC's advanced technology to provide customers with a minimum on-state resistance, high switching speed and low gate charge.

The UTC **UTN6266** is suitable for Synchronous Rectification in DC/DC and AC/DC Converters and industrial and Motor Drive applications.

FEATURES

- * $R_{DS(ON)} \leq 15 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=20\text{A}$
- * $R_{DS(ON)} \leq 19 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=18\text{A}$
- * Low gate charge
- * Low $R_{DS(ON)}$
- * High switching speed

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTN6266L-TA3-T	UTN6266G-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
UTN6266L-TM3-T	UTN6266G-TM3-T	TO-251	G	D	S	-	-	-	-	-	Tube
UTN6266L-TN3-R	UTN6266G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UTN6266L-S08-R	UTN6266G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UTN6266L-K08-5060-R	UTN6266G-K08-5060-R	DFN5060-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTN6266G-TA3-T (1) Packing Type (2) Package Type (3) Green Package		(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TM3: TO-251, TN3: TO-252 S08: SOP-8, K08-5060: DFN5060-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

Package	Marking
TO-220 TO-251 TO-252	UTC UTN6266 Lot Code 1 L: Lead Free G: Halogen Free Date Code
SOP-8	8765 UTC UTN6266 1234 Date Code L: Lead Free G: Halogen Free Lot Code
DFN5060-8	UTC UTN 6266 Lot Code Date Code

■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$, unless otherwise noted)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_{D}	30	A
	Pulsed	I_{DM}	90	A
Avalanche Current (Note 3)		I_{AS}	20	A
Avalanche Energy (Note 2, 3)		E_{AS}	280	mJ
Power Dissipation	TO-220	P_{D}	2	W
	TO-251/TO-252		1.2	W
	SOP-8		1.5	W
	DFN5060-8		1.92	W
Junction Temperature		T_{J}	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Single pulse width by junction temperature $T_{\text{J(max)}}=150^{\circ}\text{C}$.

3. $L = 1.4\text{mH}$, $I_{\text{AS}} = 20\text{A}$, $V_{\text{DD}} = 50\text{V}$, $R_{\text{G}} = 25\ \Omega$, Starting $T_{\text{J}} = 25^{\circ}\text{C}$

■ THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^{\circ}\text{C/W}$
	TO-251		110	$^{\circ}\text{C/W}$
	TO-252 (Note 2)		60	$^{\circ}\text{C/W}$
	SOP-8 (Note 2)		85	$^{\circ}\text{C/W}$
	DFN5060-8 (Note 2)		65	$^{\circ}\text{C/W}$
Junction-to-Case	TO-220	θ_{JC}	1.4	$^{\circ}\text{C/W}$
	TO-251/TO-252		2.6	$^{\circ}\text{C/W}$
	SOP-8		24	$^{\circ}\text{C/W}$
	DFN5060-8		12	$^{\circ}\text{C/W}$

Notes: 1. The θ_{JA} is the sum of the thermal impedance from junction to case θ_{JC} and case to ambient.

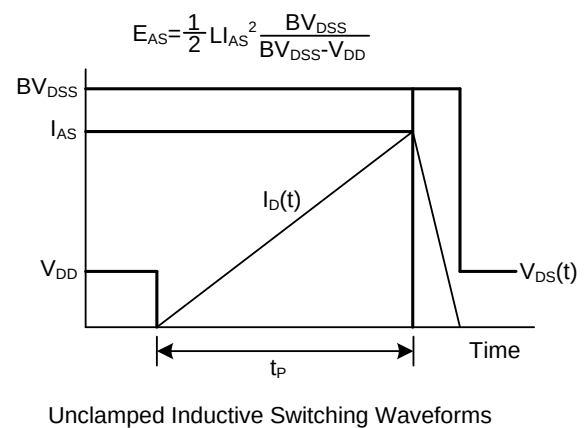
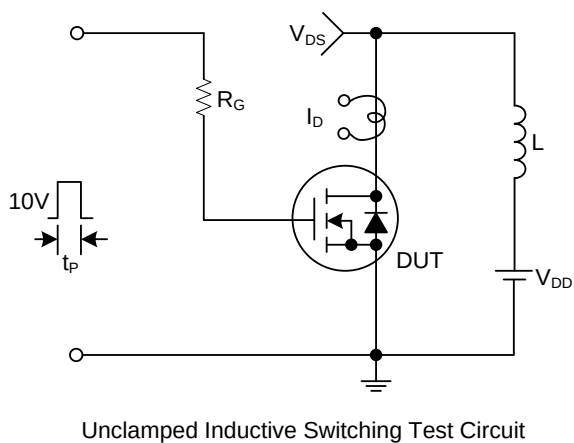
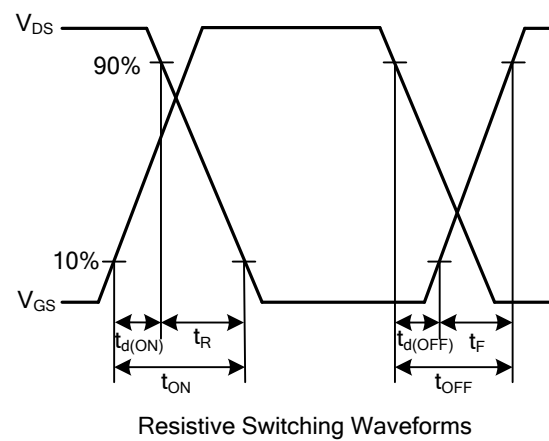
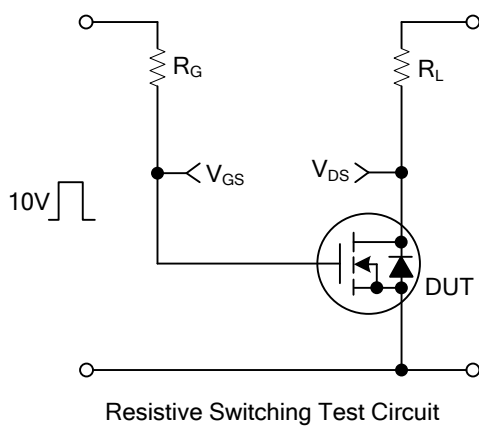
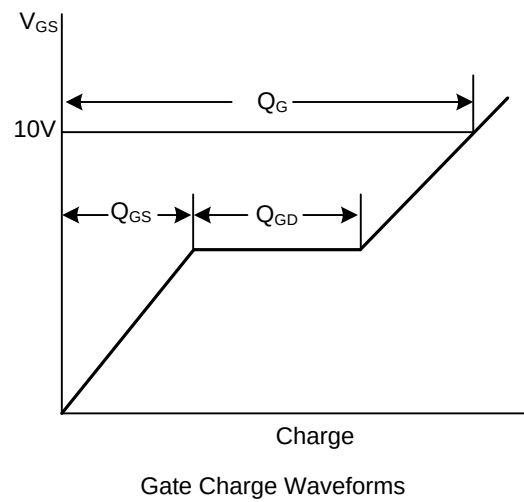
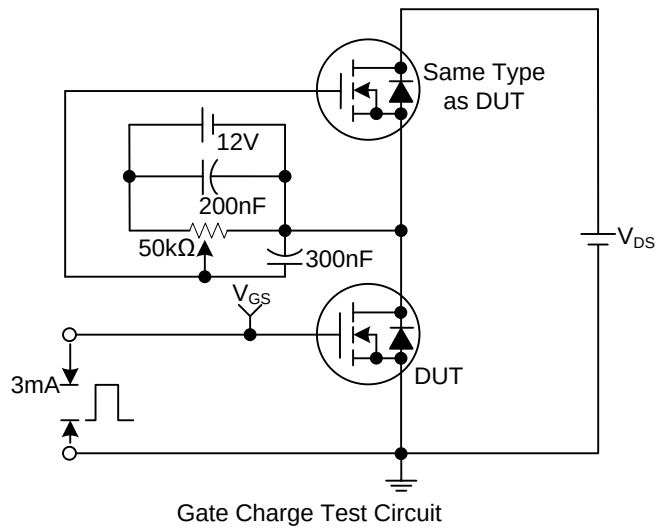
2. The value of θ_{JA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper.

ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

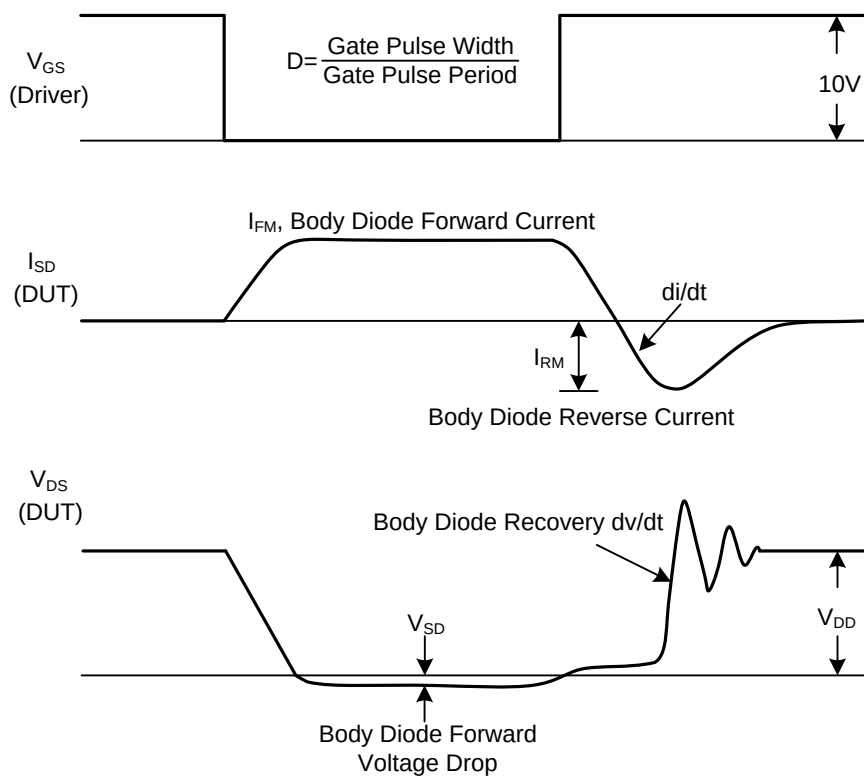
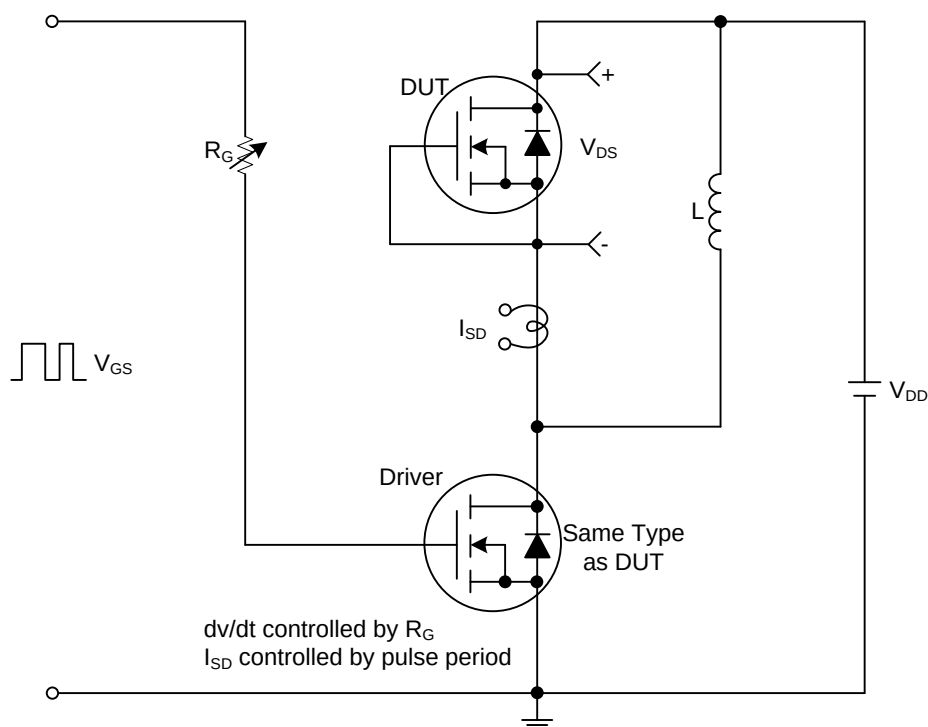
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	60			V
Zero Gate Voltage Drain Current		I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
			V _{DS} =60V, V _{GS} =0V, T _J =55°C			5	μA
Gate-Body Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.5	2.0	2.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A		12	15	mΩ
			V _{GS} =10V, I _D =20A, T _J =125°C		20.5	25	mΩ
			V _{GS} =4.5V, I _D =18A		15	19	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =30V, f=1.0MHz		2800		pF
Output Capacitance		C _{OSS}			190		pF
Reverse Transfer Capacitance		C _{RSS}			140		pF
Gate Resistance		R _G	f=1.0MHz		2.4		Ω
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{GS} =10V, V _{DS} =30V, I _D =20A		62		nC
Gate to Source Charge		Q _{GS}			8		nC
Gate to Drain Charge		Q _{GD}			10		nC
Turn-ON Delay Time		t _{D(ON)}	V _{GS} =10V, V _{DS} =30V, R _L =1.5Ω, R _{GEN} =3Ω		12		ns
Rise Time		t _R			16		ns
Turn-OFF Delay Time		t _{D(OFF)}			52		ns
Fall-Time		t _F			22		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				30	A
Drain-Source Diode Forward Voltage (Note2)		V _{SD}	I _S =1A, V _{GS} =0V		0.72	1	V

Notes: 1. Pulse width limited by $T_{J(MAX)}$
 2. Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
 3. Surface Mounted on 1in^2 pad area.

■ TEST CIRCUITS AND WAVEFORMS

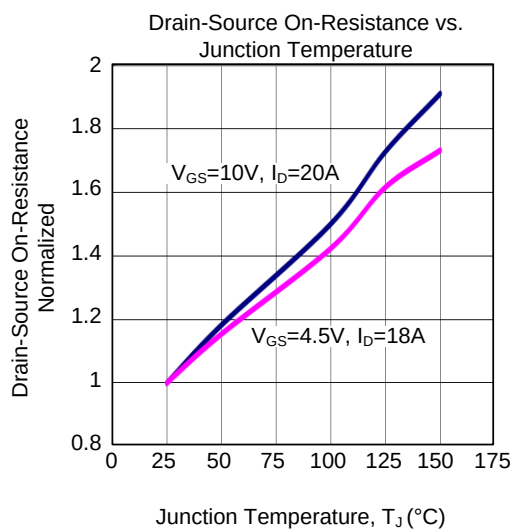
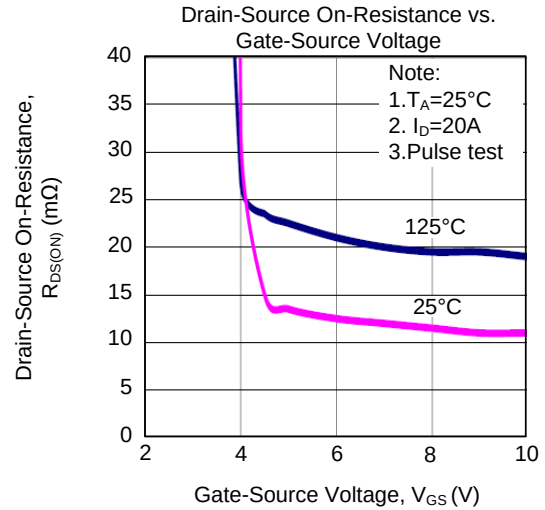
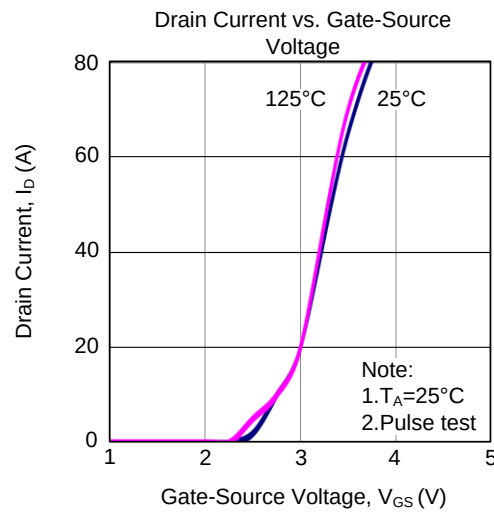
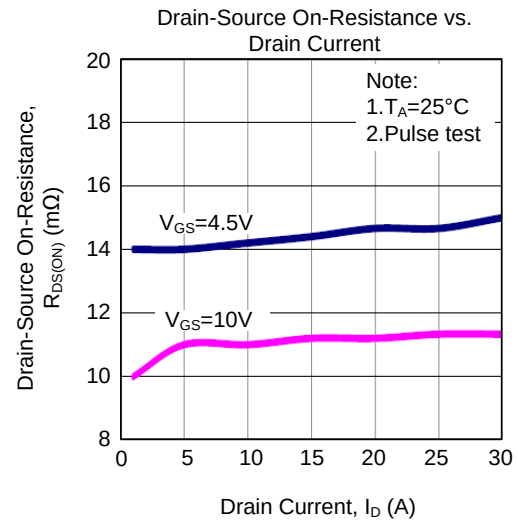
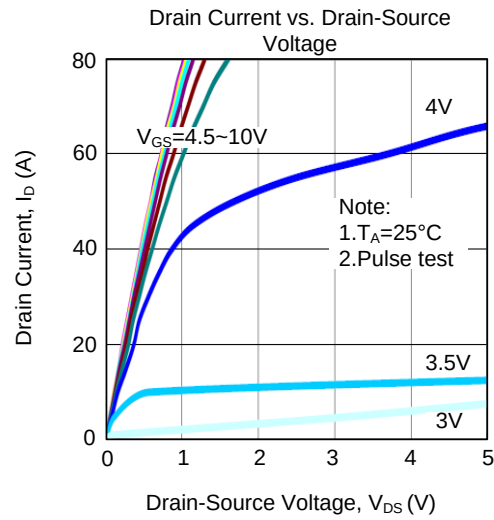


■ TEST CIRCUITS AND WAVEFORMS (Cont.)



Peak Diode Recovery dv/dt Test Circuit and Waveforms

TYPICAL CHARACTERISTICS



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