



UTT45N03

Power MOSFET

45A, 30V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **UTT45N03** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

The UTC **UTT45N03** is generally applied in low power switching mode power appliances and electronic ballast.

FEATURES

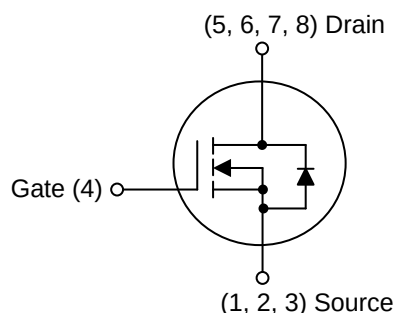
* $R_{DS(ON)} \leq 10m\Omega$ @ $V_{GS}=10V$, $I_D=25A$

$R_{DS(ON)} \leq 18m\Omega$ @ $V_{GS}=4.5V$, $I_D=15A$

* High Switching Speed

* Improved dv/dt capability

SYMBOL

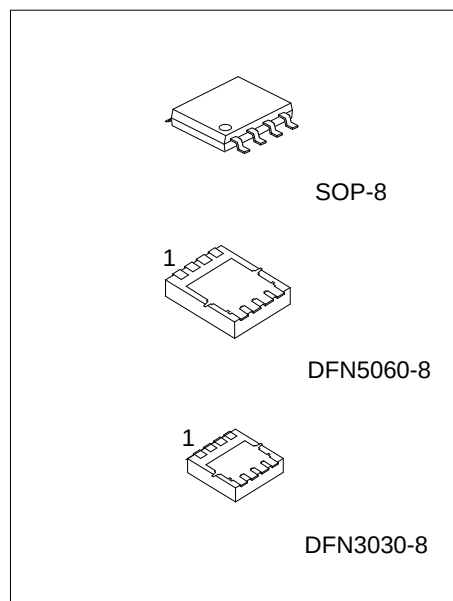


ORDERING INFORMATION

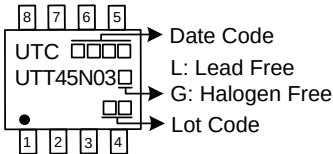
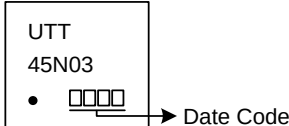
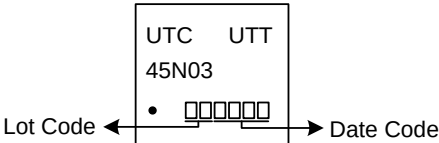
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT45N03L-S08-R	UTT45N03G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UTT45N03L-K08-3030-R	UTT45N03G-K08-3030-R	DFN3030-8	S	S	S	G	D	D	D	D	Tape Reel
UTT45N03L-K08-5060-R	UTT45N03G-K08-5060-R	DFN5060-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT45N03G-S08-R (1)Packing Type (2)Package Type (3)Green Package		(1) R: Tape Reel (2) S08: SOP-8, DFN3030-8: DFN3030-8 K08-5060: DFN5060-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING

PACKAGE	MARKING
SOP-8	 Diagram of SOP-8 package marking. The package is shown with pins 1-8. Markings include: UTC (top left), UTT45N03 (top center), a date code (top right, 4 digits), L: Lead Free (middle right), G: Halogen Free (bottom right), and a lot code (bottom center, 4 digits).
DFN3030-8	 Diagram of DFN3030-8 package marking. The package is shown with markings: UTT (top left), 45N03 (top center), a date code (top right, 4 digits), and a lot code (bottom center, 4 digits).
DFN5060-8	 Diagram of DFN5060-8 package marking. The package is shown with markings: UTC (top left), UTT (top center), 45N03 (top right), a date code (bottom right, 4 digits), and a lot code (bottom left, 4 digits).

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current		I_D	45	A
Pulsed Drain Current (Note 2)		I_{DM}	90	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	38	mJ
Peak Diode Recovery dv/dt		dv/dt	4.4	V/ns
Power Dissipation	SOP-8	P_D	1.8	W
	DFN3030-8		15	W
	DFN5060-8		30	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Operation and Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=27.6\text{A}$, $V_{DD}=20\text{V}$, $R_G=20\Omega$, Starting $T_J=25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $V_{DS}=0\text{V}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	90	$^{\circ}\text{C/W}$
	DFN3030-8		75	$^{\circ}\text{C/W}$
	DFN5060-8		70	$^{\circ}\text{C/W}$
Junction to Case	SOP-8	θ_{JC}	69	$^{\circ}\text{C/W}$
	DFN3030-8		8.3	$^{\circ}\text{C/W}$
	DFN5060-8		4.2	$^{\circ}\text{C/W}$

Note: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

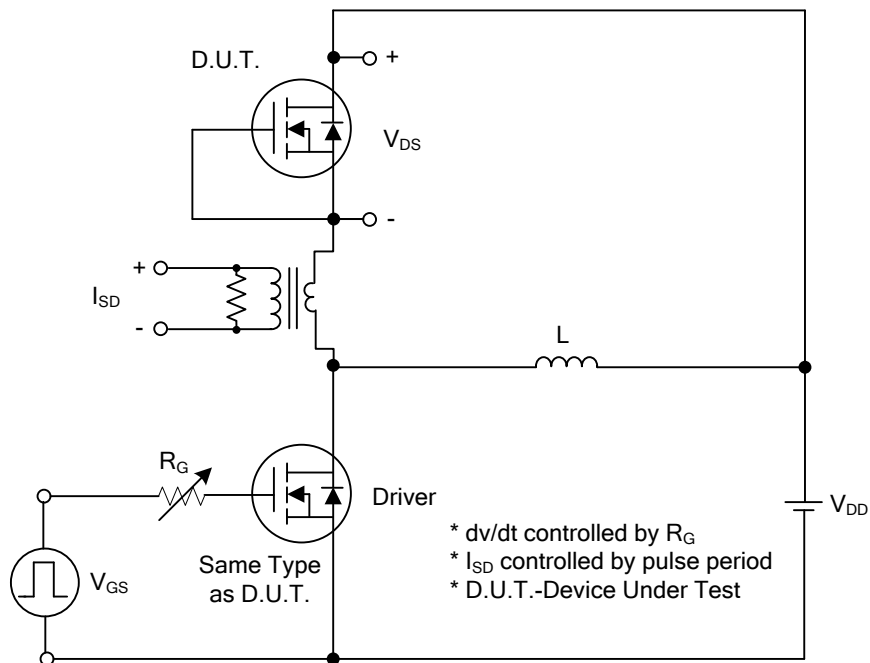
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =20V, V _{DS} =0V			100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	0.9		2.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =25A			10	mΩ
			V _{GS} =4.5V, I _D =15A			18	mΩ
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =15V, f=1MHz		920		pF
Output Capacitance		C _{OSS}			238		pF
Reverse Transfer Capacitance		C _{RSS}			210		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge		Q _G	V _{DS} =15V, V _{GS} =10V, I _D =45A I _G =1mA (Note1,2)		25.7		nC
Gate-Source Charge		Q _{GS}			2.6		nC
Gate-Drain Charge		Q _{GD}			6		nC
Turn-On Delay Time		t _{D(ON)}	V _{DS} =15V, V _{GS} =10V, I _D =45A, R _G =3.3Ω (Note1,2)		6		ns
Turn-On Rise Time		t _R			16.5		ns
Turn-Off Delay Time		t _{D(OFF)}			25		ns
Turn-Off Fall Time		t _F			22		ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Maximum Body-Diode Continuous Current		I _S				45	A
Maximum Body-Diode Pulsed Current		I _{SM}				90	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =45A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =30A, V _{GS} =0V,		182		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dI _S /dt=100A/μs		294		nC

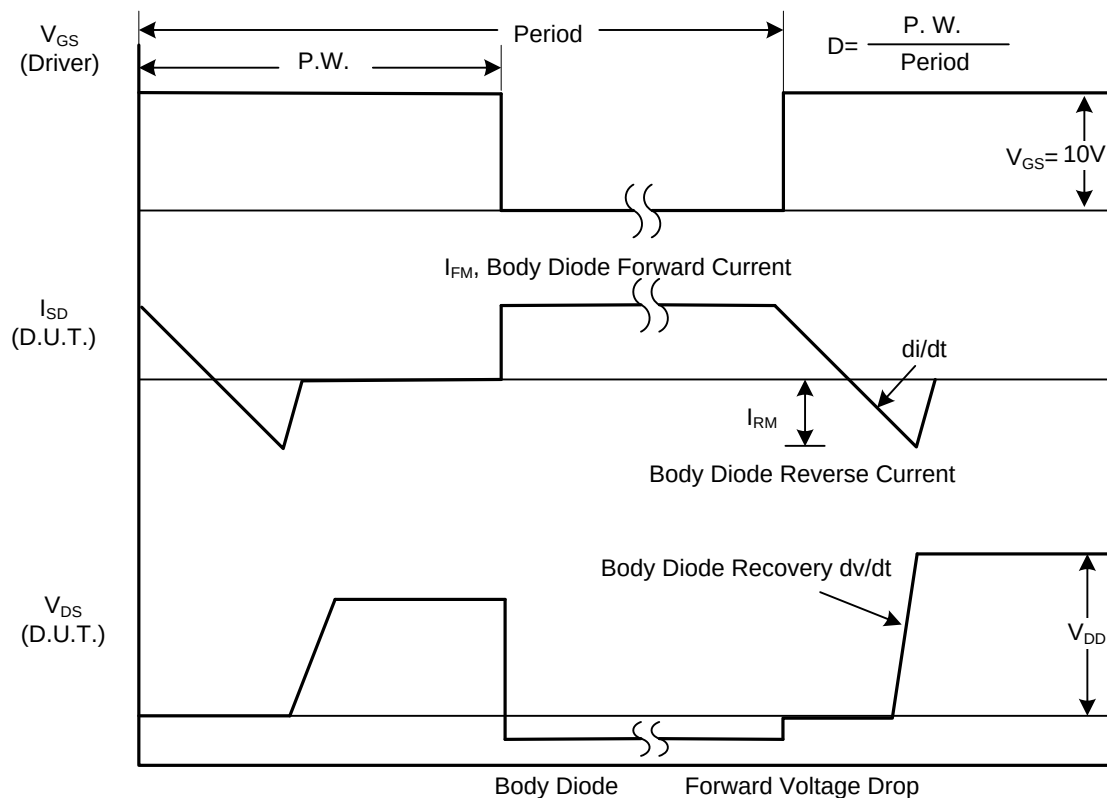
Notes: 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

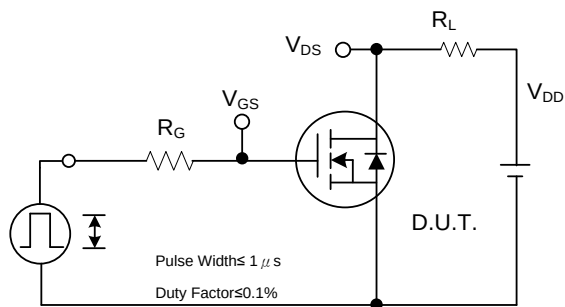


Fig. 2A Switching Test Circuit

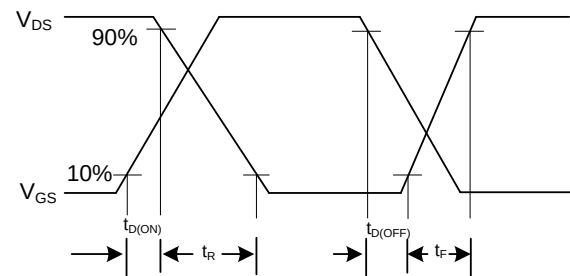


Fig. 2B Switching Waveforms

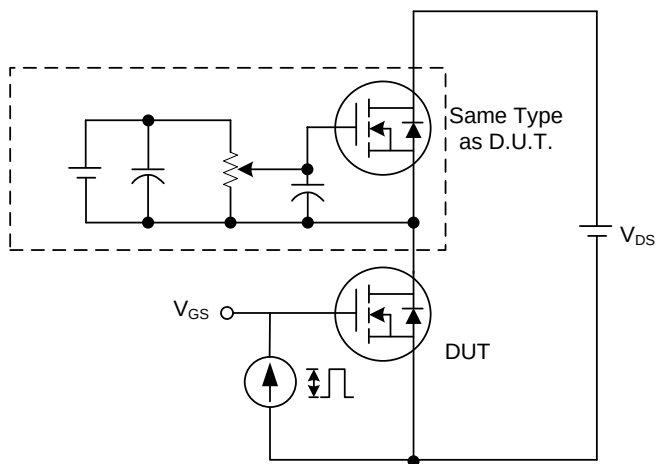


Fig. 3A Gate Charge Test Circuit

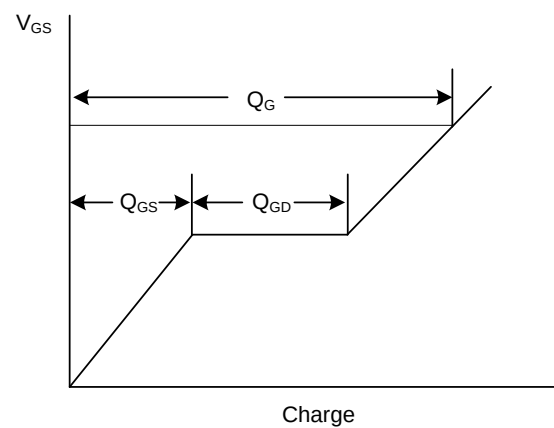


Fig. 3B Gate Charge Waveform

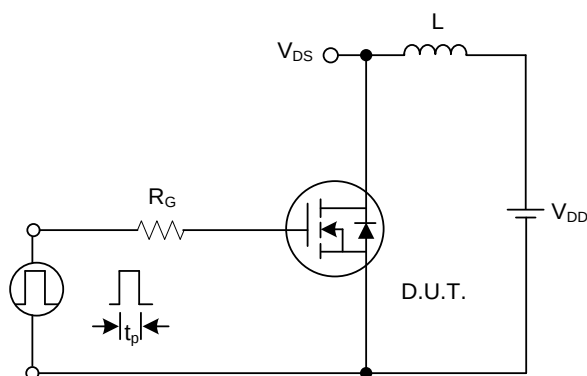


Fig. 4A Unclamped Inductive Switching Test Circuit

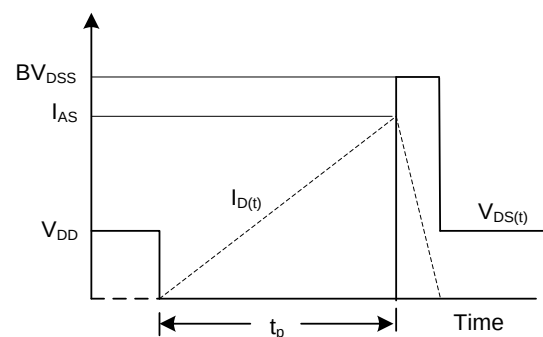
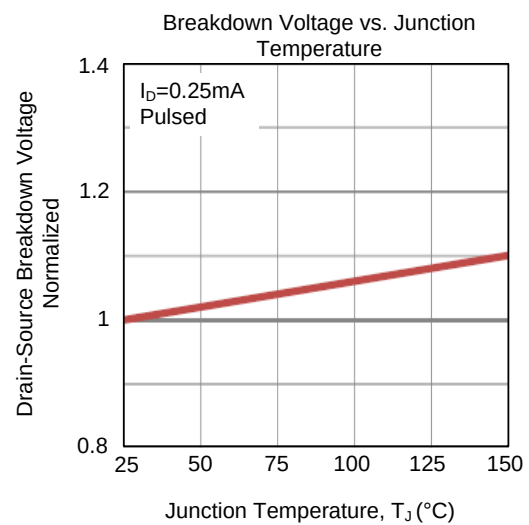
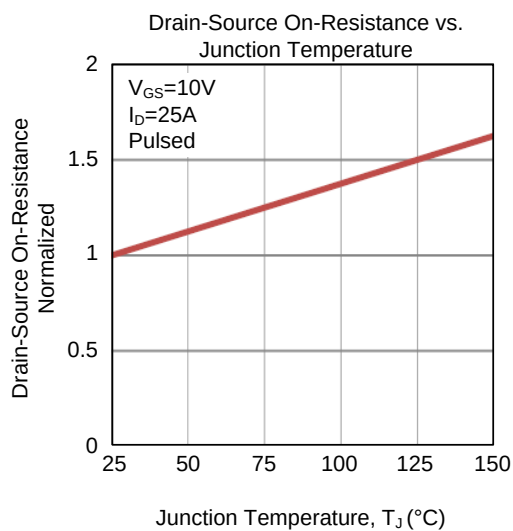
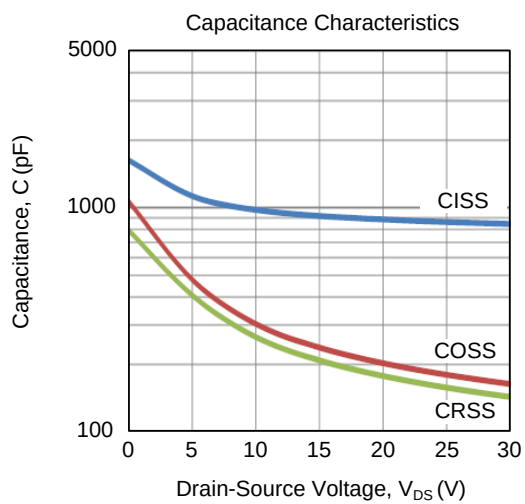
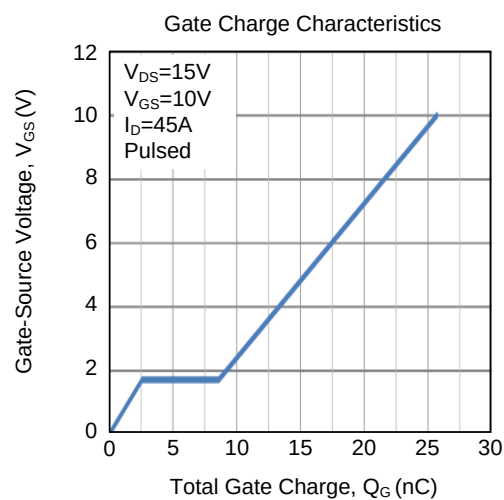
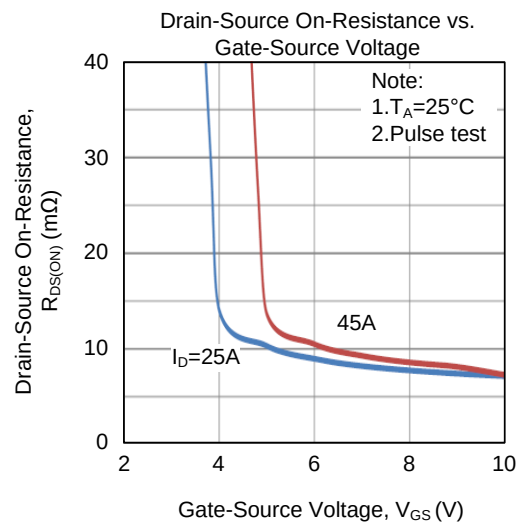
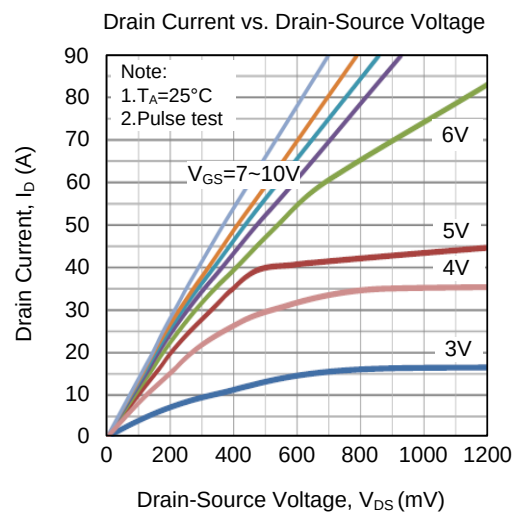
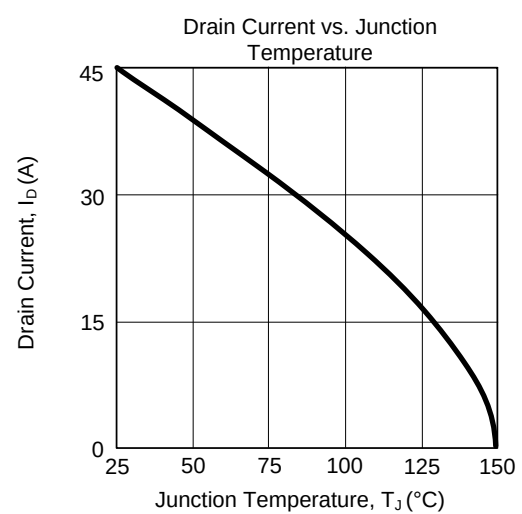
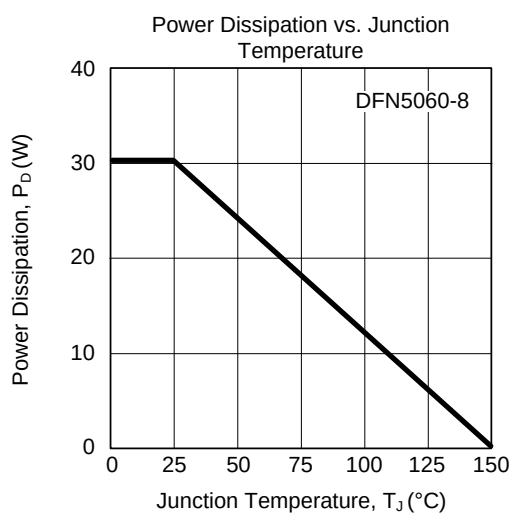
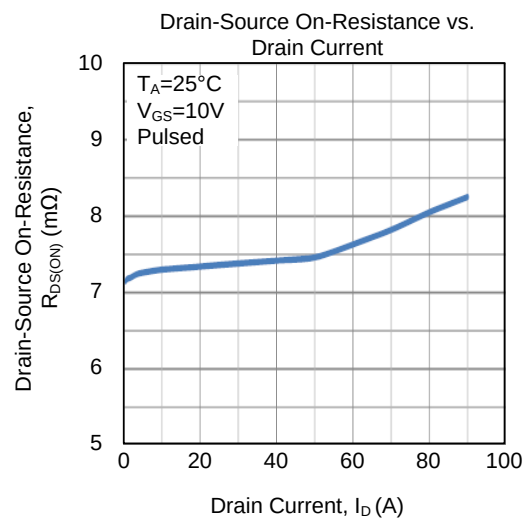
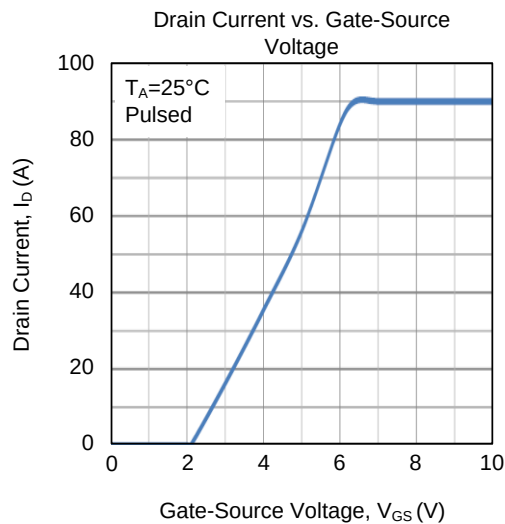
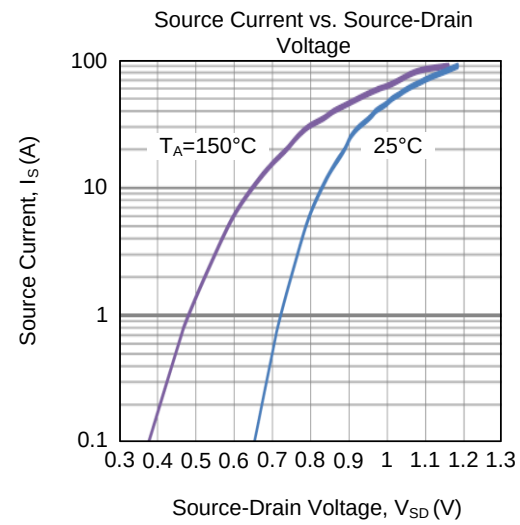
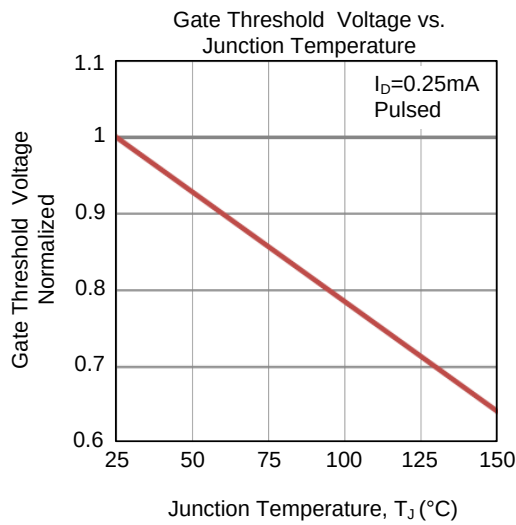


Fig. 4B Unclamped Inductive Switching Waveforms

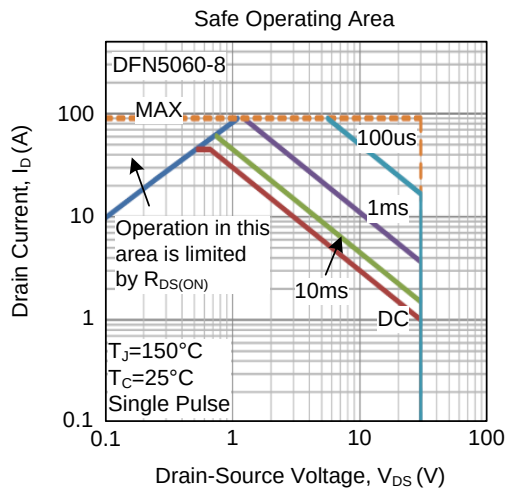
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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