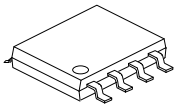
UWD706

CMOS IC

MICROPROCESSOR UP WATCH DOG TIMER



SOP-8

■ DESCRIPTION

The UTC **UWD706** microprocessor supervisory circuit reduces the complexity and number of components required to monitor power-supply and monitor microprocessor activity. It significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The UTC **UWD706** provides power-supply monitoring circuitry that generates a reset output during power-up, power-down and brownout conditions. The reset output remains operational with VCC as low as 1V. Independent watchdog monitoring circuitry is also provided. This is activated if the watchdog input has not been toggled within 1.6 seconds.

In addition, there is a 1.25V threshold detector for power-fail warning, low-battery detection, or monitoring an additional power supply. An active-low manual-reset input ($\overline{MR}$) is also included.

■ FEATURES

* Precision supply- Voltage Monitor
* Valid $\overline{RESET}$ remains with V_{CC} as low as 1V
* 200ms Reset Pulse Width
* Independent Watchdog Timer (1.6sec) Timeout
* Voltage Monitor for Power-Fail or Low-Battery Warning
* With Manual reset input

■ ORDERING INFORMATION

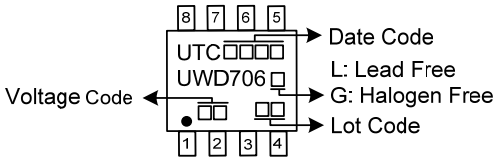
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UWD706L-x-S08-R	UWD706G-x-S08-R	SOP-8	Tape Reel

Note: Pin Assignment : x: Output Voltage, refer to Marking Information.

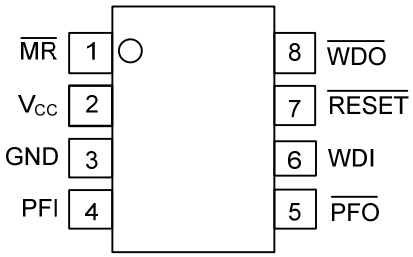
UWD706G-x-S08-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) S08: SOP-8
(3)Output Voltage Code	(3) x: refer to Marking Information
(4)Green Package	(4) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOP-8	A : 2.63V B : 2.93V C : 3.08V D: 4.00V H: 4.40V G: 4.65V	

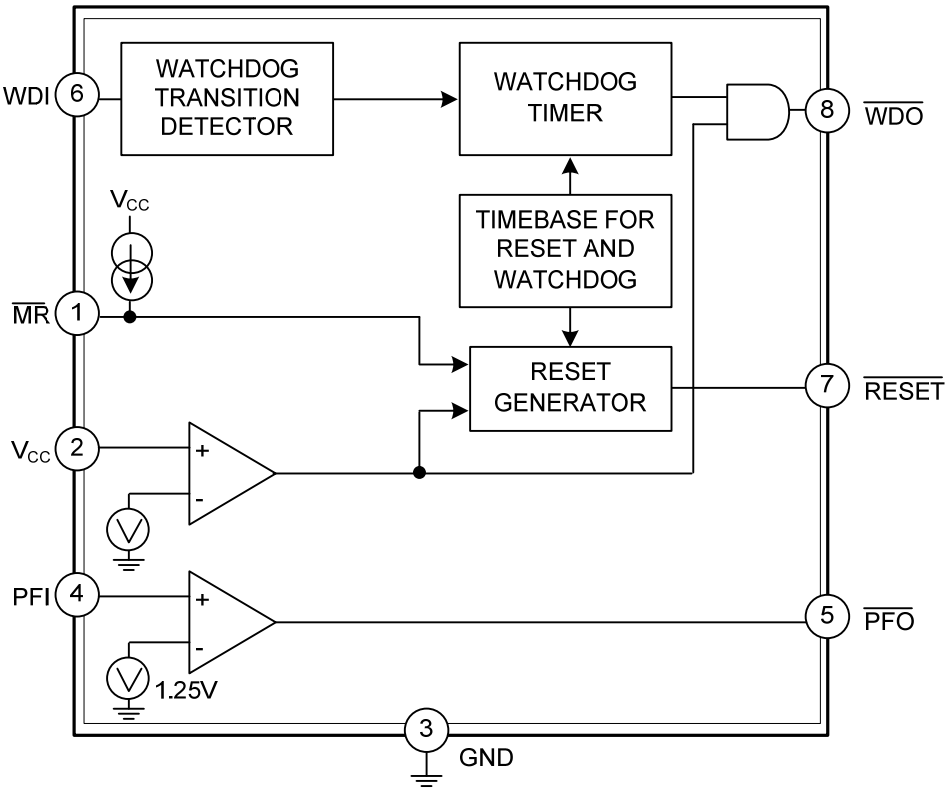
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{MR}$	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 500μA (V_{CC}= +5V) pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	V_{CC}	Power Supply Voltage that is monitored.
3	GND	0V Ground Reference for all signals.
4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and WDO goes low (BLOCK DIAGRAM). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
7	$\overline{RESET}$	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold. It remains low for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	$\overline{WDO}$	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, $\overline{WDO}$ goes high with no delay.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Terminal Voltage (with respect to GND)	V_{CC}	-0.3 ~ 6.0	V
All Other Inputs	V_{IN}	-0.3 ~ (V_{CC}+0.3V)	V
Input Current, V_{CC}, GND	I_{CC}	20	mA
Output Current, (all outputs)	I_{OUT}	20	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_J =-40~+85°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		V_{CC}		1.0		5.5	V
Supply Current		I_{SUPPLY}			50	150	μA
Reset Threshold	UWD706-A	V_{RT}		2.56	2.63	2.68	V
	UWD706-B			2.85	2.93	2.95	V
	UWD706-C			3.02	3.08	3.14	V
	UWD706-D			3.91	4.0	4.07	V
	UWD706-H			4.25	4.4	4.5	V
	UWD706-G			4.5	4.65	4.75	V
Reset Threshold Hysteresis					60		mV
Reset Pulse Width		t_{RS}		120	200	280	ms
$\overline{RESET}$ Output Voltage			I_{SOURCE} = 800μA	V_{CC}-1.5			V
			I_{sink}=3.2mA			0.4	V
			V_{CC}=1V, I_{sink}=50μA			0.3	V
Watchdog Timeout Period		t_{WD}		1.0	1.6	2.25	sec
WDI Pulse Width		t_{WP}	V_{IL}=0.4V, V_{IH} = V_{CC}		70		ns
WDI Input Threshold	Low		V_{CC}=5V			0.5	V
	High		V_{CC}=5V	3.5			V
	Low		$V_{RST(MAX)}$< V_{CC}< 3.6V			0.5	V
	High		$V_{RST(MAX)}$< V_{CC}< 3.6V	0.7×V_{CC}			V
WDI Input Current			WDI=V_{CC}		50	150	μA
			WDI=0V	-150	-50		μA
$\overline{WDO}$ Output Voltage			I_{SOURCE}=800μA	V_{CC}-1.5			V
			I_{sink}=1.2mA			0.4	V
$\overline{MR}$ Pull-Up Current			$\overline{MR}$ = 0V		500		μA
$\overline{MR}$ Pulse Width		t_{MR}		250			ns
$\overline{MR}$ Input Threshold	Low		T_A = +25°C			0.8	V
	High			2			V
$\overline{MR}$ to Reset Out Delay		t_{MD}				350	ns
PFI Input Threshold				1.18	1.25	1.3	V
PFI Input Current			V_{CC}= 5V		0.2		nA
$\overline{PFO}$ Output Voltage			I_{SOURCE}= 800μA	V_{CC}-1.5			V
			I_{sink}=3.2mA			0.4	V

■ APPLICATION NOTES

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to V_{CC}=0V

When V_{CC} falls below 1V, the **UWD706** $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the $\overline{\text{RESET}}$ pin as shown in Figure 1, any stray charge or leakage currents will be drained to ground, holding $\overline{\text{RESET}}$ low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

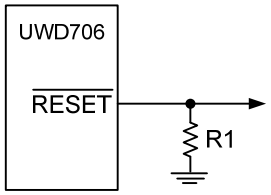


Figure 1. $\overline{\text{RESET}}$ Valid to Ground Circuit

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{\text{PFO}}$. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{\text{RESET}}$ can be asserted on other voltages in addition to the +5V V_{CC} line. Connect $\overline{\text{PFO}}$ to MR to initiate a $\overline{\text{RESET}}$ pulse when PFI drops below 1.25V. Figure 2 shows the **UWD706** configured to assert $\overline{\text{RESET}}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

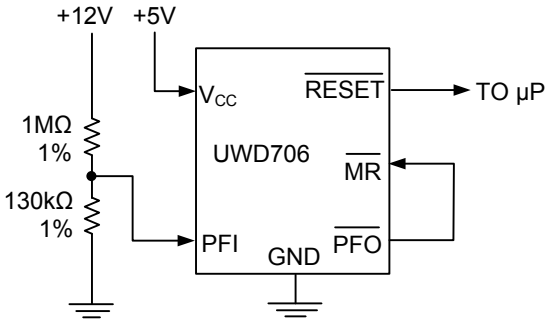
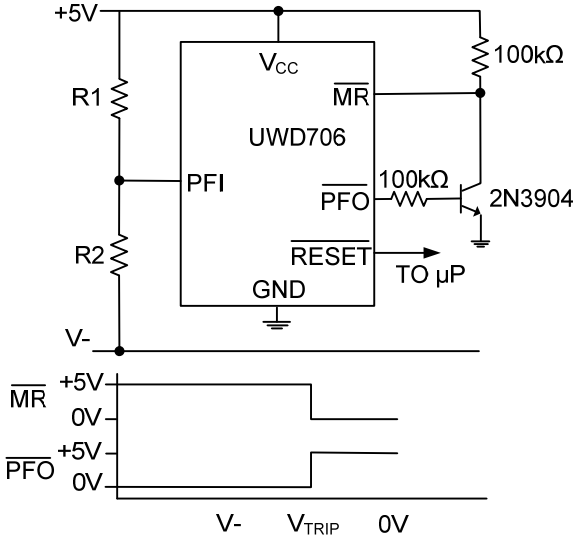


Figure 2.Monitoring Both +5V and +12V

■ APPLICATION NOTES (Cont.)

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 3). When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{PFO}$ is high. By adding the resistors and transistor as shown, a high $\overline{PFO}$ triggers reset. As long as $\overline{PFO}$ remains high, the **UWD706** will keep reset asserted ($\overline{RESET}$ = low, $\overline{RESET}$ = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.



$$\frac{5-1.25}{R1}=\frac{1.25-V_{TRIP}}{R2} \qquad V_{TRIP}<0$$

Figure 3.Monitoring a Negative Voltage

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins can contend with the **UWD706** $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the Microprocessor wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as in Figure 4. Buffer the $\overline{RESET}$ output to other system components.

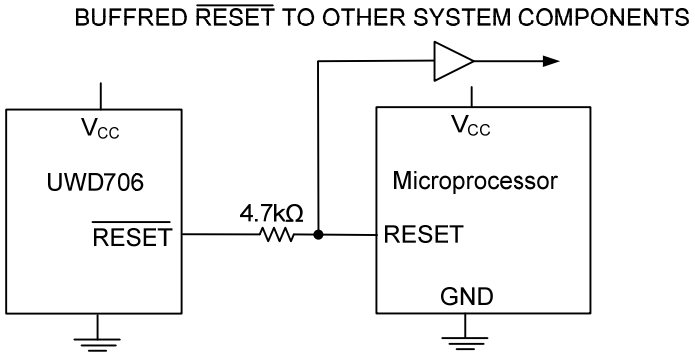
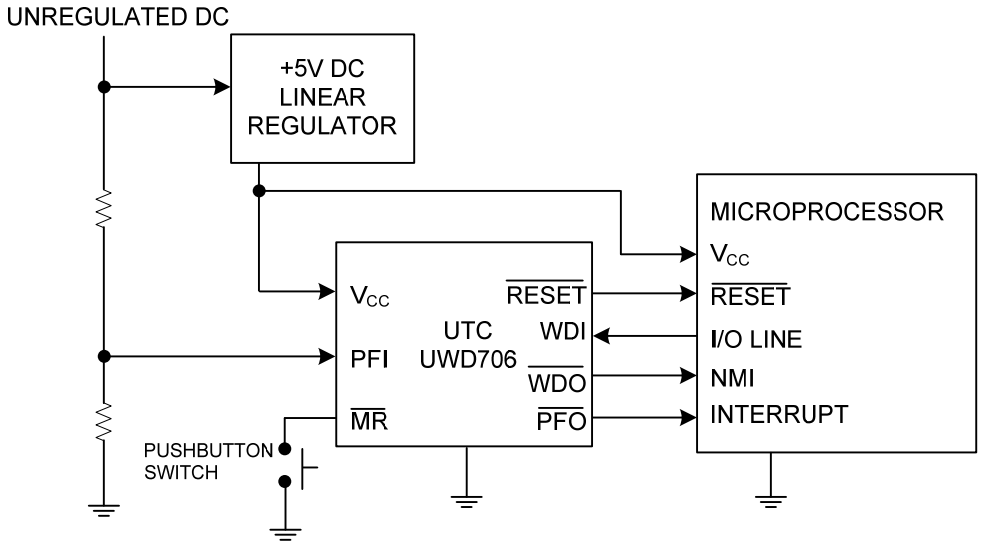


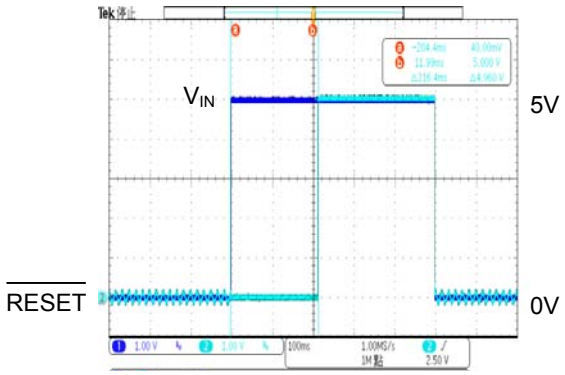
Figure 4. Interfacing to Microprocessors with Bidirectional Reset I/O

■ TYPICAL APPLICATION CIRCUIT

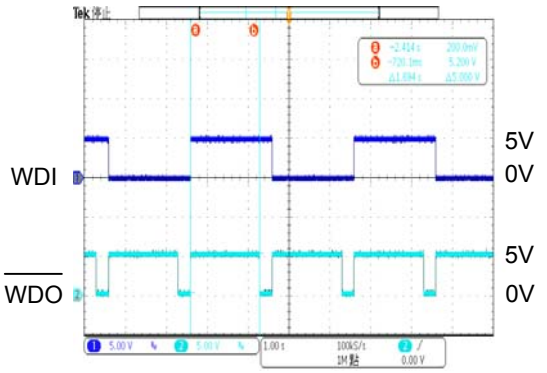


■ TYPICAL CHARACTERISTICS

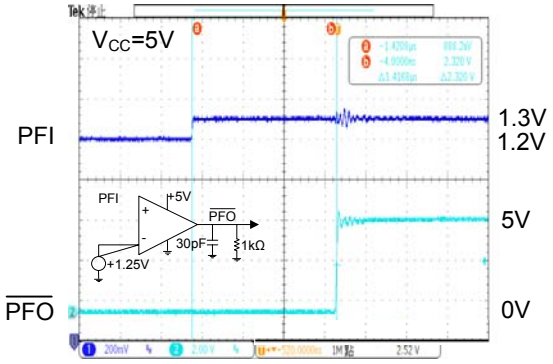
Reset Pulse Width (T_{RS})



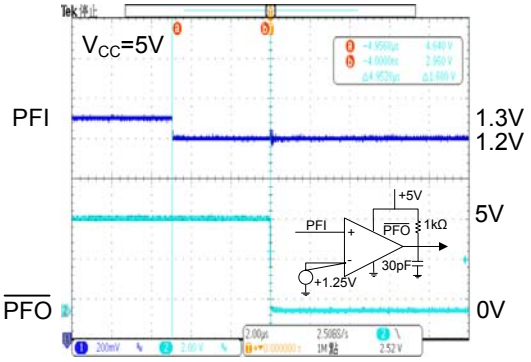
Watch Dog Timeout Period (T_{WD})



Power-Fail Comparator De-assertion Response Time



Power-Fail Comparator Assertion Response Time



$\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ Timing