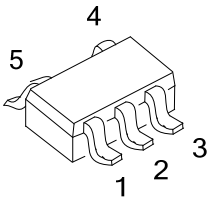
# MICROPOWER µP WATCH DOG TIMER




SOT-25

## ■ DESCRIPTION

The UTC **UWD817** families are groups of high-precision, low current consumption voltage detectors with manual reset input and watchdog functions based on CMOS process. The series consist of a reference voltage source, delay circuit, comparator, and output driver. With the built-in delay circuit, the UTC **UWD817** series do not require any external components to output signals with release delay time. The user can choose detect voltage thresholds.

The WDI pin in the UTC **UWD817** can be left open if the watchdog function is not used. Whenever the watchdog pin is opened, the internal counter clears before the watchdog timeout occurs. Since the manual reset pin is internally pulled up to the $V_{IN}$ pin voltage level, the ICs can be used by leaving the manual reset pin unconnected if the pin is unused.

## ■ FEATURES

* Precision Supply-Voltage Monitor
* Operating Voltage Range: 1.0V~5.5V
* Output Configuration: CMOS
* Watchdog Function: Watchdog input WD
* Wide Temperature Range: -40°C to +85°C

## ■ ORDERING INFORMATION

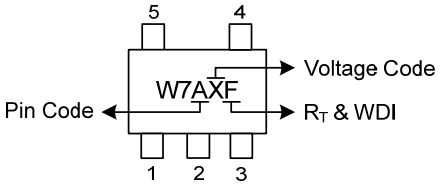
| Ordering Number | | Reset Time | Watch Dog Interval | UNIT | Code | Package | Packing |
|---|---|---|---|---|---|---|---|
| Lead Free | Halogen Free | | | | | | |
| UWD817XL-x-x-AF5-R | UWD817XG-x-x-AF5-R | 210 | 1760 | ms | F | SOT-25 | Tape Reel |

UWD817XG-x-x-AF5-R

(1)Packing Type
(2)Package Type
(3)$R_T$ & WDI
(4)Output Voltage Code
(5)Green Package
(6)Pin Code

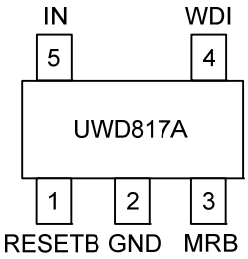
(1) R: Tape Reel
(2) AF5: SOT-25
(3) refer to Reset Time & Watch Dog Interval
(4) x: Refer to Marking Information
(5) G: Halogen Free and Lead Free, L: Lead Free
(6) refer to PIN CONFIGURATION

## ■ MARKING INFORMATION

| PACKAGE | VOLTAGE CODE | MARKING |
|---|---|---|
| SOT-25 | A: 2.63V<br>B: 2.93V<br>C: 3.08V<br>D: 4.00V<br>H: 4.40V<br>G: 4.65V |  |



## ■ PIN CONFIGURATION

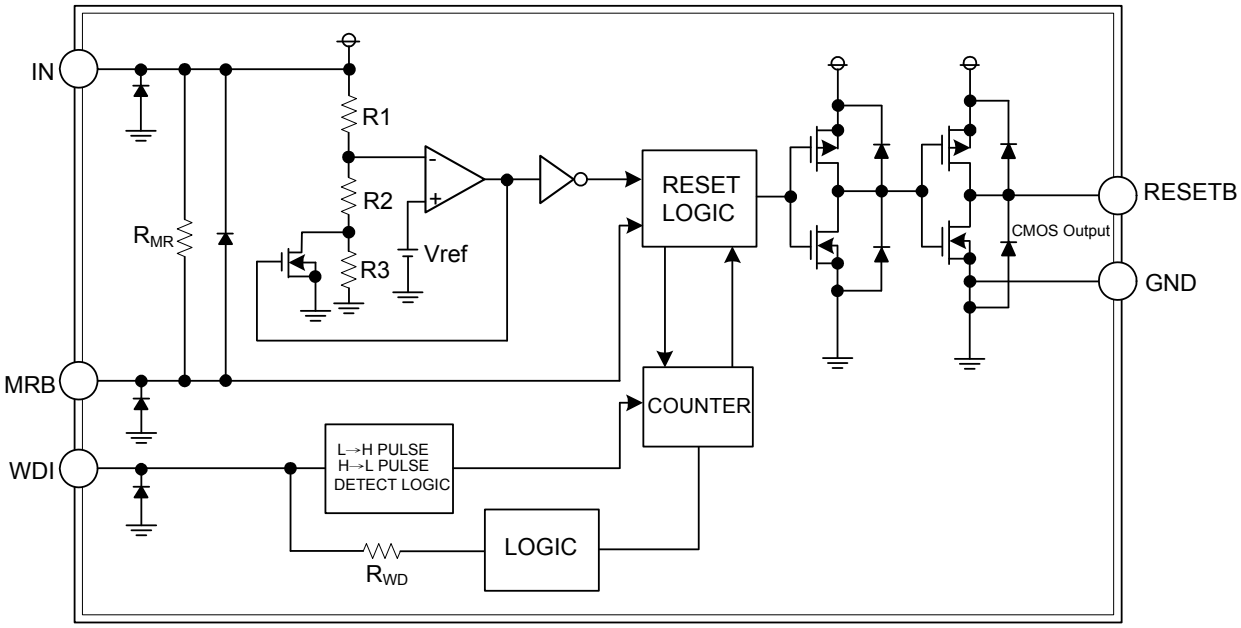




## ■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | RESETB | RESETB is active low. This pin can be push/pull. |
| 2 | GND | Ground |
| 3 | MRB | Manual Reset. Active low. Pulling this pin low forces a reset. After a low to high transition reset remains asserted for exactly one reset timeout period. This pin is internally pulled high. If this function is unused then float this pin or tie it to $V_{IN}$. |
| 4 | WDI | Watch Dog Input. Any transition on this pin will reset the watch dog timer. If this pin remains high or low for longer than the watch dog interval then a reset is asserted. Float or tristate this pin to disable the watch dog feature. |
| 5 | IN | Positive power supply. A reset is asserted after this voltage drops below a predetermined level. After $V_{IN}$ rises above that level reset remains asserted until the end of the reset timeout period. |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{IN}$ | 5.5 | V |
| Power Dissipation | $P_D$ | 400 | mW |
| Junction Temperature | $T_J$ | +150 | °C |
| Ambient Temperature | $T_A$ | -40 ~ +85 | °C |
| Storage Temperature | $T_{STG}$ | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ THERMAL DATA

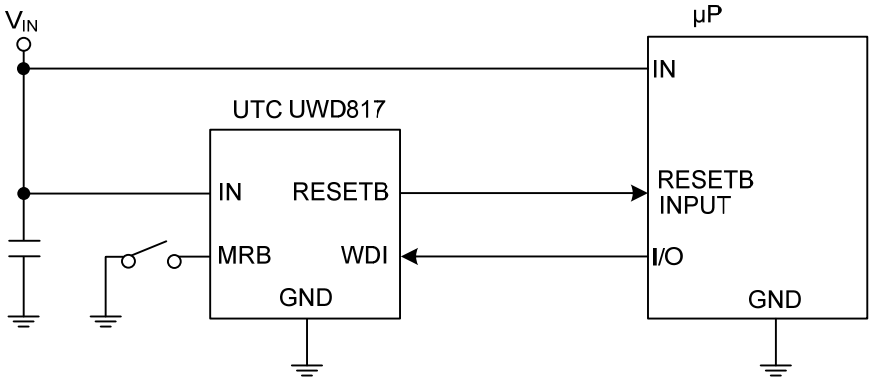
| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Junction to Ambient | $\theta_{JA}$ | 310 | °C/W |
| Junction to Case | $\theta_{JC}$ | 90 | °C/W |

## ■ ELECTRICAL CHARACTERISTICS ($T_A$=25°C, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ Range | $V_{IN}$ | | 1.0 | | 5.5 | V |
| Supply Current | $I_{IN}$ | | | | 50 | μA |
| Reset Threshold | $V_{TH}$ | | $V_{TH}$ -2% | | $V_{TH}$ +2% | V |
| Reset B Output Voltage High | $V_{OH}$ | $V_{IN}>V_{DF}$ Max. $I_{SOURCE}$=0.5mA, $T_A$=-40~+85°C | 0.8$V_{IN}$ | | | V |
| Reset B Output Voltage Low | $V_{OL}$ | $V_{IN}<V_{DF}$ Min. $I_{SNK}$=1.2mA, $T_A$=-40~+85°C | | | 0.5 | V |
| $V_{IN}$ to Reset Delay | $T_{D1}$ | $V_{IN}=V_{DF}$ -100mV | | 40 | | μS |
| Release Delay Time (Note 1) | $t_{DR}$ | | 140 | 210 | 280 | mS |
| Watch Dog Timeout Period (Note 2) | $T_{WD}$ | | 1120 | 1760 | 2400 | mS |
| WDI Pulse Width | $T_{WDI}$ | | | 300 | | nS |
| WDI Input Threshold | $W_{DI\ IL}$ | $V_{IN}=V_{TH}$ x 1.2 | | | 0.7 | V |
| | $W_{DI\ IH}$ | | 0.8$V_{IN}$ | | | V |
| WDI Input Current | $I_{IL}$ | WDI=0V | -15 | -8 | | μA |
| | $I_{IH}$ | WDI=$V_{IN}$=6.0V | | 8 | 15 | μA |
| MRB Input Threshold | $M_{RB\ IL}$ | $V_{IN}=V_{DF}$ x 1.2 | | | 0.7 | V |
| | $M_{RB\ IH}$ | | 0.8$V_{IN}$ | | | V |
| MRB Pulse Width | $T_{WMRB}$ | | 1 | | | μS |
| MRB to Reset Delay | $T_{DMRB}$ | | | 500 | | nS |
| MRB Pull Up Resistance | | | 80 | | 160 | KΩ |

Notes: 1. Release delay time (TWD) watchdog timeout period settings are available in 1.7s.
2. Watchdog timeout period settings are available in 1.7s.

## ■ TYPICAL APPLICATION CIRCUIT



## ■ OPERATIONAL EXPLANATION

The UTC **UWD817** series compare the voltage of the internal reference source with the voltage divided by R1, R2 and R3 connected to the $V_{IN}$ pin. The resulting signal activates the watchdog logic, manual reset logic, delay circuit and the output driver. When the $V_{IN}$ voltage gradually falls and finally reaches the detect voltage, the RESETB goes from high to low in the case of the $V_{DFL}$ type ICs.

**Reset Output**

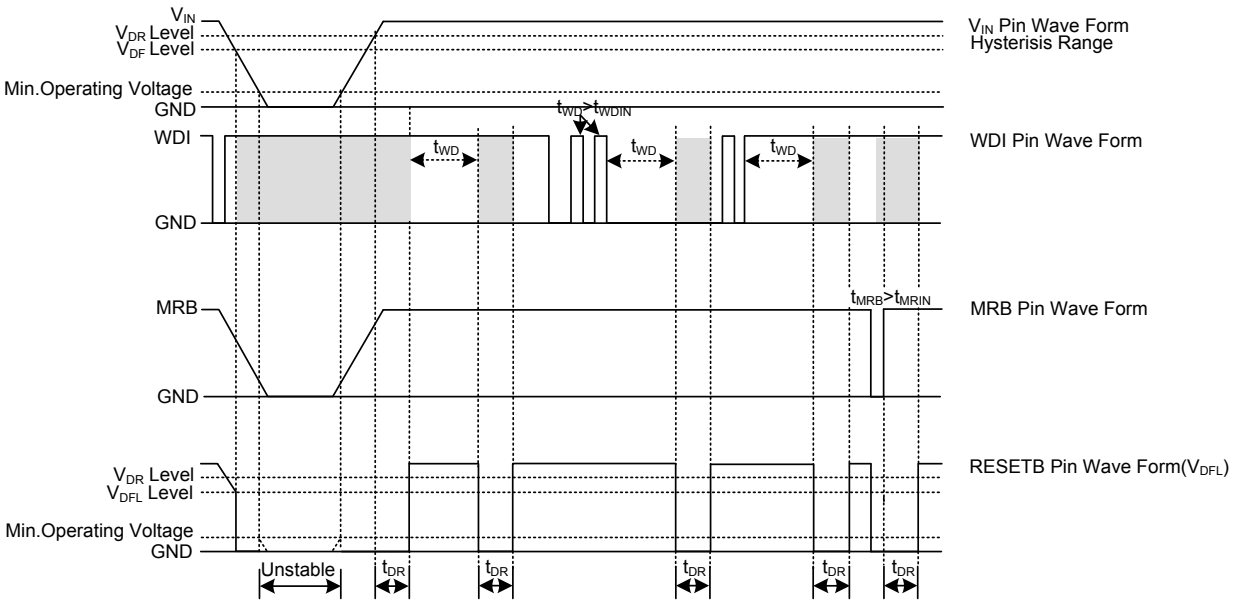
Each output pin in the series can be configured to be either CMOS. In addition each output may be either active high or active low. Active low reset outputs are denoted as RESETB.

When 3 things below are happen, the output will be reseted:

1. $V_{IN}$ drops below the threshold ($V_{TH}$)
2. The MRB pin is pulled low.
3. The WDI pin does not detect a transition signal within the watch dog interval ($T_{WD}$).

The reset will remain asserted for the prescribed reset interval after:

1. $V_{IN}$ rises above the threshold ($V_{TH}$)
2. MRB goes high
3. The watch dog timer has timed out causing the reset to assert.




**Manual Reset Input**

Using the MRB pin input, the RESETB pin signal can be forced to the detection state. When the MRB pin is driven from high to low, the RESETB pin output goes from high to low level in the case of the $V_{DFL}$ type ICs. Even after the MRB pin is driven back high, the RESETB pin output maintains the detection state for the release delay time ($t_{DR}$). Because of internally pulled up for the MRB pin, so leave the MRB pin open if unused. A diode, which is an input protection element, is connected between the MRB pin and $V_{IN}$ pin. Therefore, when the MRB pin voltage exceeds $V_{IN}$, the current will flow to $V_{IN}$ through the diode. Please use this IC within the stated maximum ratings ($V_{SS}$-0.3~$V_{IN}$+0.3≤6.0V) on the MRB pin.

## ■ OPERATIONAL EXPLANATION (Cont.)

**Watchdog Input**

The UTC **UWD817** series use a watchdog timer to detect malfunction or “runaway” of the microprocessor. If neither rising nor falling signals are applied from the microprocessor within the watchdog timeout period, the RESETB pin output maintains the detection state for the release delay time ($t_{DR}$), and thereafter the RESETB pin output returns to the release state. The timer in the watchdog is then restarted. Watchdog timeout period settings are available in 1.7s

**Release Delay Time**

Release delay time ($t_{DR}$) is the time that elapses from when the $V_{IN}$ pin reaches the release voltage, or when the watchdog timeout period expires with no rising signal applied to the WDI pin, until the RESETB pin output is released from the detection state.