UZ2400

Silicon Version D

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

U-Power1000D Module

AN-2400-64

Version: 0.0
Released Date:2009/10/26

The content of this technical document is subject to change without notice. Please contact UBEC for further information.

UZ2400

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

1. General Information

The U-Power1000D module is an IEEE 802.15.4 compliant solution that satisfies the requirements of low-cost and long-range wireless applications. The module, containing UBEC's UZ2400D, UP2206, UA2725 and other necessary components, operates in the ISM 2.4 GHz frequency band. The corresponding MCU can accesses to various UZ2400D internal subunits, such as registers, FIFOs, and security key table, via a 4-wire SPI bus. Its small form factor saves valuable board spaces and provides a reliable delivery of critical data between the devices.

2. Features

- 2.4GHz IEEE 802.15.4 compliant
- 3.0 ~ 3.6V Operation
- Effective Distance: 1000 meters (line of sight, environment dependent, typical)
- SMA Connector
- Additional 2 GSG (ground-signal-ground) Interfaces Provided
- RX Sensitivity: -100dBm, typical
- TX Output Power: 18dBm, typical
- TX Current Consumption: 210mA, typical
- RX Current Consumption: 34mA, typical
- Dimension: 35.9mm x 14mm x 3.6mm(without SMA connector)
- Shielding case optional

3. Pin Configuration

3.1. Pin Assignment

Top view of a U-Power1000D Module and its pin allocation map are shown in Figures 1 and 2 respectively.

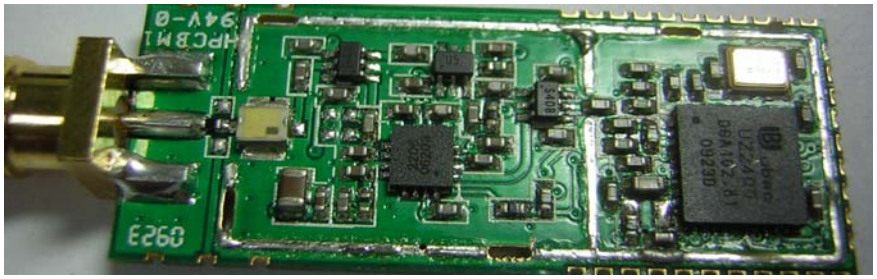

Figure 1. Top View of U-Power1000D Module

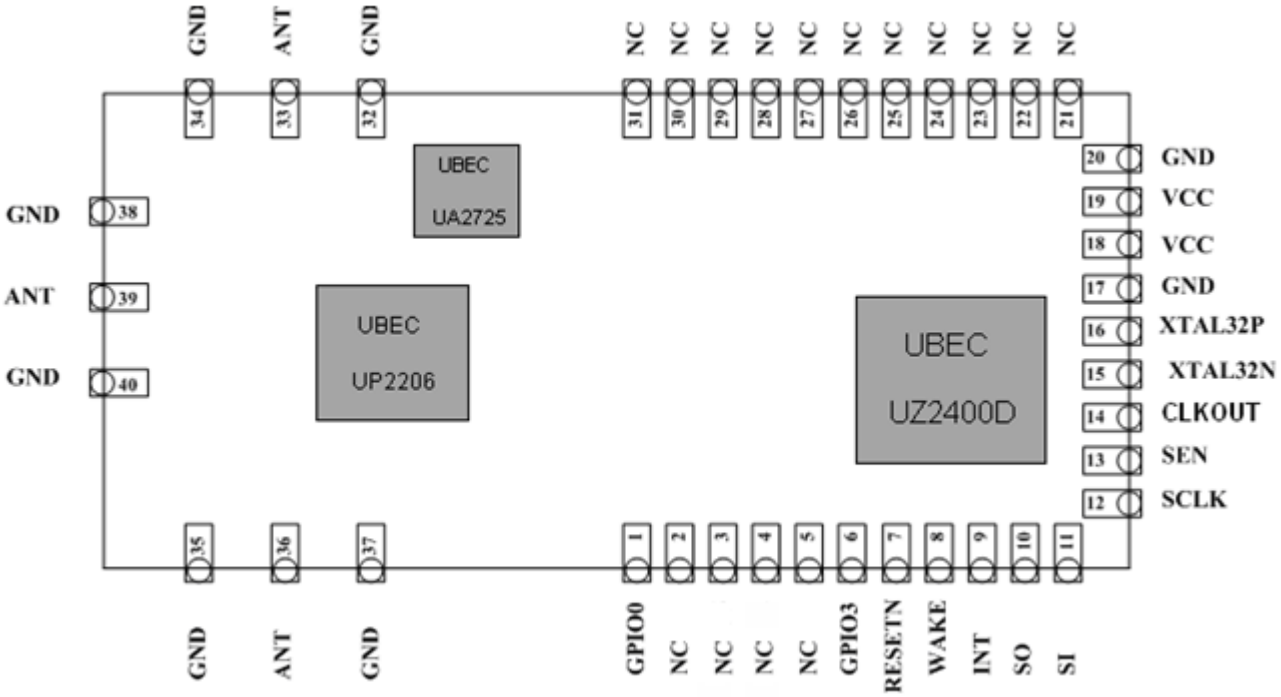

Figure 2. Pin Allocation

3.2. Pin Description

Pin type abbreviation: A = Analog, D = Digital, I = Input, O = Output, P = Power, G = Ground

Pin Number	Pin Name	Type	Description
1	GPIO0	DIO	General purpose digital I/O, also used as an external PA enable
2	NC		No connection
3	NC		No connection
4	NC		No connection
5	NC		No connection
6	GPIO3	DIO	General purpose digital I/O
7	RESETN	DI	Global hardware reset pin, active low
8	WAKE	DI	External wake up trigger, active high / low can be programmable.
9	INT	DO	Interrupt pin to microprocessor : Level trigger, Hi / Low programmable
10	SO	DO	Serial interface data output from UZ2400 or I2C clock
11	SI	DIO	Serial interface data input to UZ2400 or I2C data in/out
12	SCLK	DI	Serial interface clock
13	SEN	DI	Serial interface enable
14	CLKOUT	DO	32 / 16 / 8 / 4 / 2 / 1 MHz clock output
15	XTAL32N	AI	32 kHz Crystal input (-) for internal RTC used
16	XTAL32P	AI	32 kHz Crystal input (+) for internal RTC used
17	GND	G	Ground
18	VCC	P	Power Supply
19	VCC	P	Power Supply
20	GND	G	Ground
21~31	NC		No connection
32	GND	G	Ground
33	ANT	AIO	Antenna Port
34	GND	G	Ground
35	GND	G	Ground
36	ANT	AIO	Antenna Port
37	GND	G	Ground
38	GND	G	Ground
39	ANT	AIO	Antenna Port
40	GND	G	Ground

Table 1. Pin Assignment

4. Electrical Specifications

Test conditions: T_A = 25°C, VDD = 3.3 V, (P_{out},UZ2400=-10dBm

ITEM	Condition	Specification			Unit
		Min.	Typ.	Max.	
Frequency		2405		2480	MHz
Supply voltage		3.0	3.3	3.6	V
TX Current consumption	(P_{out} =18 dBm)		210		mA
RX Current consumption			34		mA
TX Output power	P_{out}(UZ2400)=-10dBm		18		dBm
TX EVM	P_{out}(UZ2400)=-10dBm		14		%
RX sensitivity	PER<=1% O-QPSk 250kbps		-100		dBm
Communication Range	Throughput >120kbps at 250kbps data rate, LOS		1000		m

Table 2. Electrical Specifications

For detailed electrical characteristics of the UZ2400 chip, please refer to UZ2400 datasheet.

4.1. TX Output Power

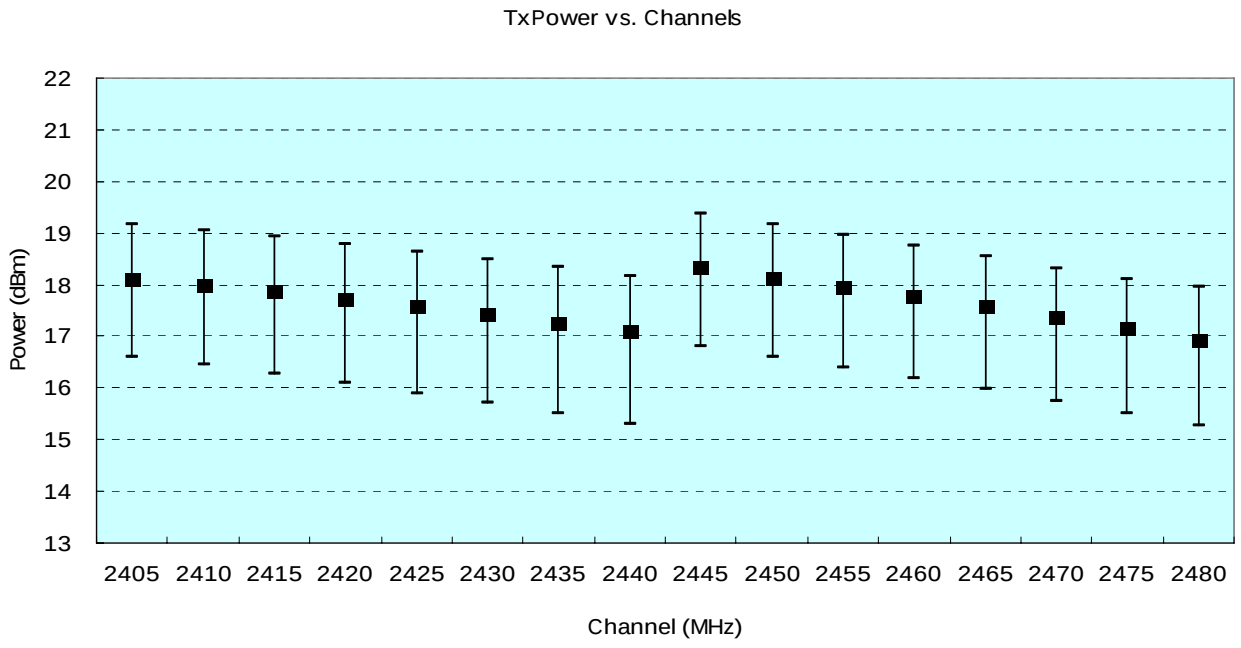

Figure 3. Typical TX Output Power

*Note. Set LREG0x274=0xc6 between channel 2445MHz to 2480MHz.

4.2. TX EVM

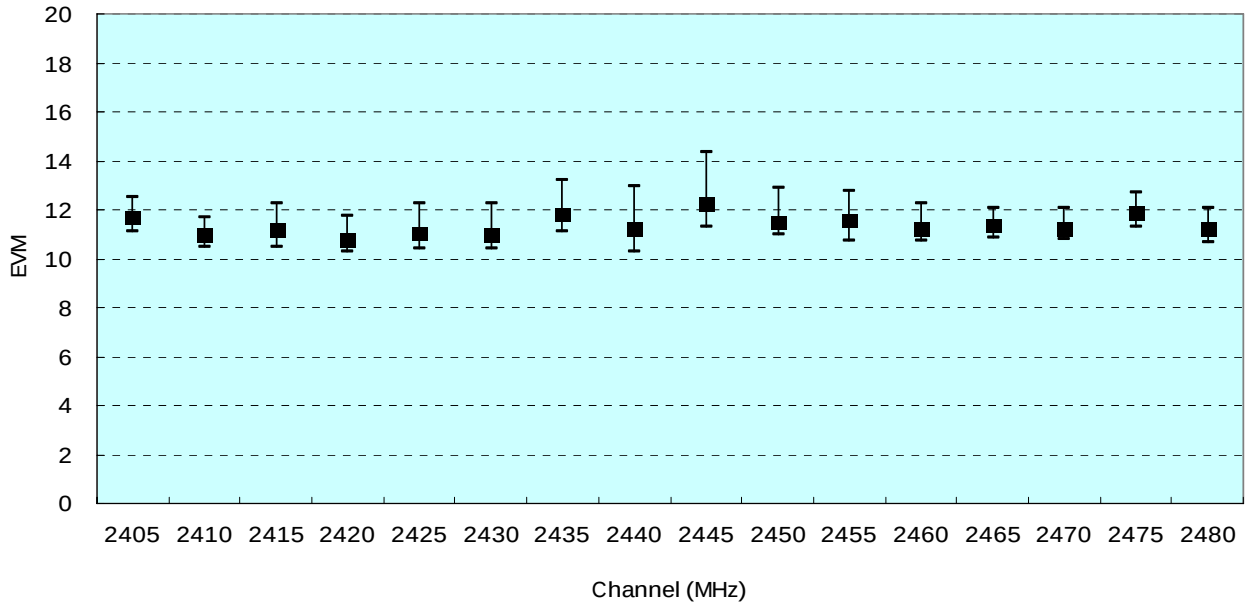

Figure 4. Typical TX EVM

4.3. RX Sensitivity

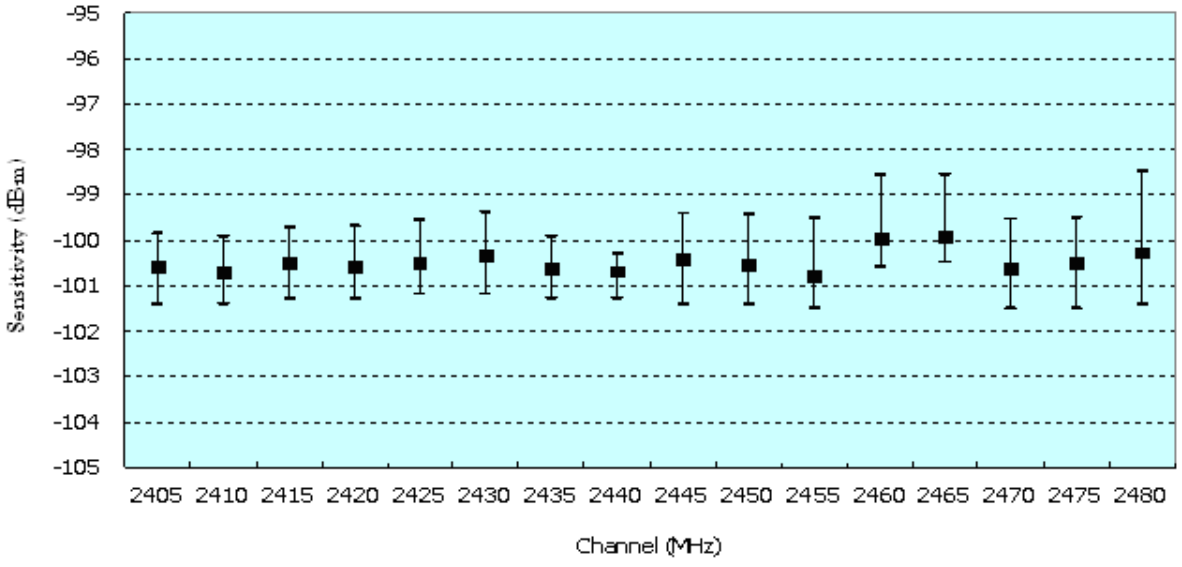

Figure 5. Typical RX Sensitivity

5. Register Initial Settings

The procedure to configure the initial settings is described as below.

Sep 1. Initialization

Refer to UZ2400 datasheet section 4.3.1 to initialize this module.

Step 2. Set Channel

The module operates in the 2.4 GHz ISM unlicensed band. The operating frequency is divided into 16 channels. RFCTL0 (LREG0x200) should be configured for the selected channel.

Address mode	Address	Register Name	Descriptions	Setting Value(hex)	Note	
					Channel	Frequency
LREG	0x200	RFCTL0	Set RF operation channel	03	11	2405 MHz
				13	12	2410 MHz
				23	13	2415 MHz
				33	14	2420 MHz
				43	15	2425 MHz
				53	16	2430 MHz
				63	17	2435 MHz
				73	18	2440 MHz
				83	19	2445 MHz
				93	20	2450 MHz
				A3	21	2455 MHz
				B3	22	2460 MHz
				C3	23	2465 MHz
				D3	24	2470 MHz
				E3	25	2475 MHz
				F3	26	2480 MHz

Step 3. Reset

After the operation channel is set, RF state machine should be reset by setting RFCTL (SREG0x36) to “0x04” and then setting RFCTL(SREG0x36) to “0x00”. After reset, 192us delay is required for the VCO calibration to calibrate the PLL block to the correct frequency.

Address mode	Address	Register Name	Descriptions	Setting Value(hex)
SREG	0x36	RFCTL	Reset RF state machine	0x04
SREG	0x36	RFCTL	Reset RF state machine	0x00

***Step 4.* PA/LNA Control**

Address mode	Address	Register Name	Descriptions	Setting Value(hex)
LREG	0x22F	TESTMODE	GPIO0, GPIO1, GPIO2 are configured to control external PA, LNA or switch	0x29
LREG	0x203	RFCTL3	RF optimized control for U-Power1000D	0xF8
LREG	0x253	RFCTL53	RF optimized control for U-Power1000D	0x0B
LREG	0x274	RFCTL74	RF optimized control for U-Power1000D	0xA6

After finishing all the above four steps, a basic initialization procedure is completed. This configuration procedure should be valid for most of the applications.

*Note. LREG0x203, 0x253, 0x274 control the PA gain. Refer to Appendix A.

6. Schematic

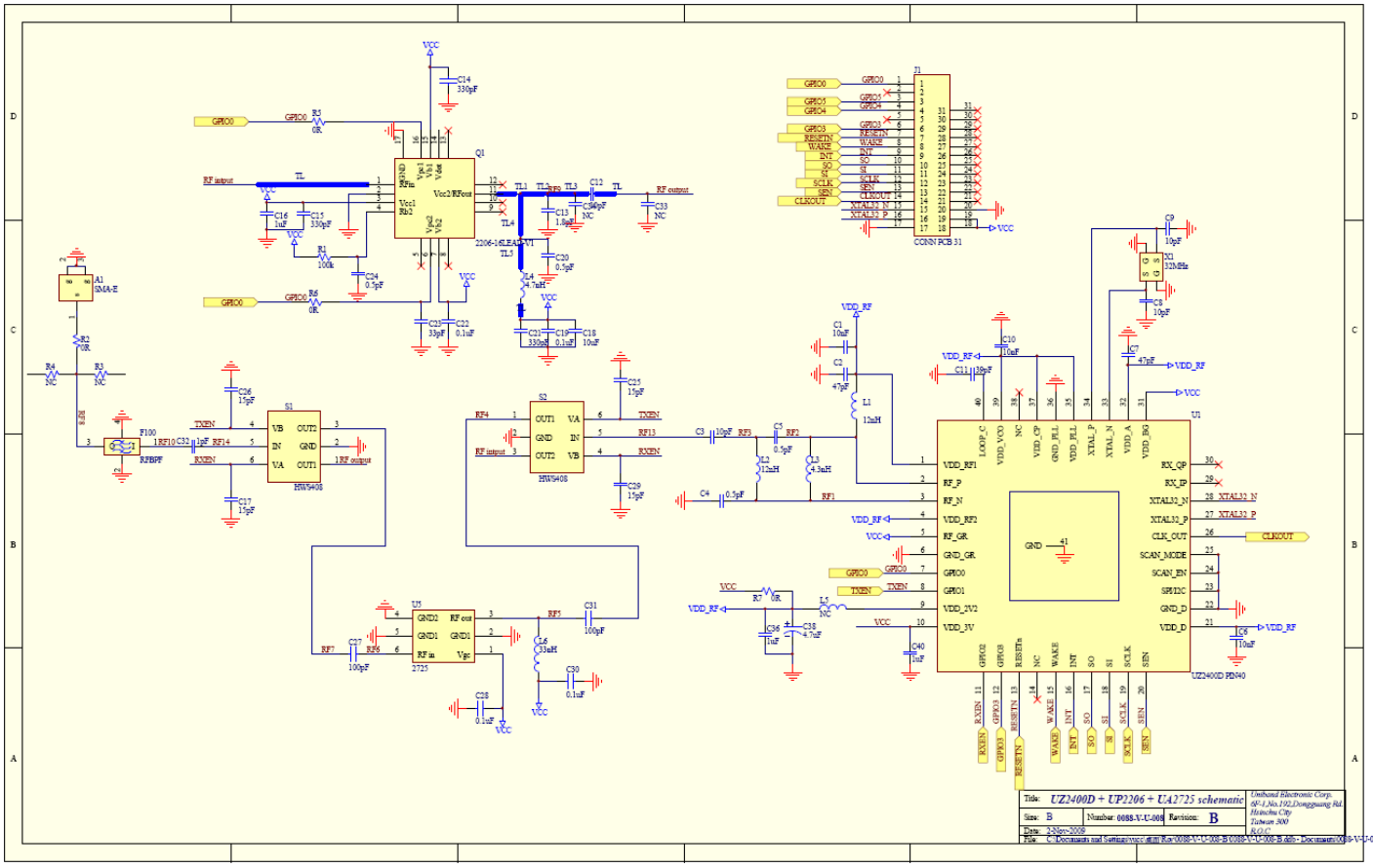

Figure 6. Schematic of U-Power1000D Module

7. PCB Layout

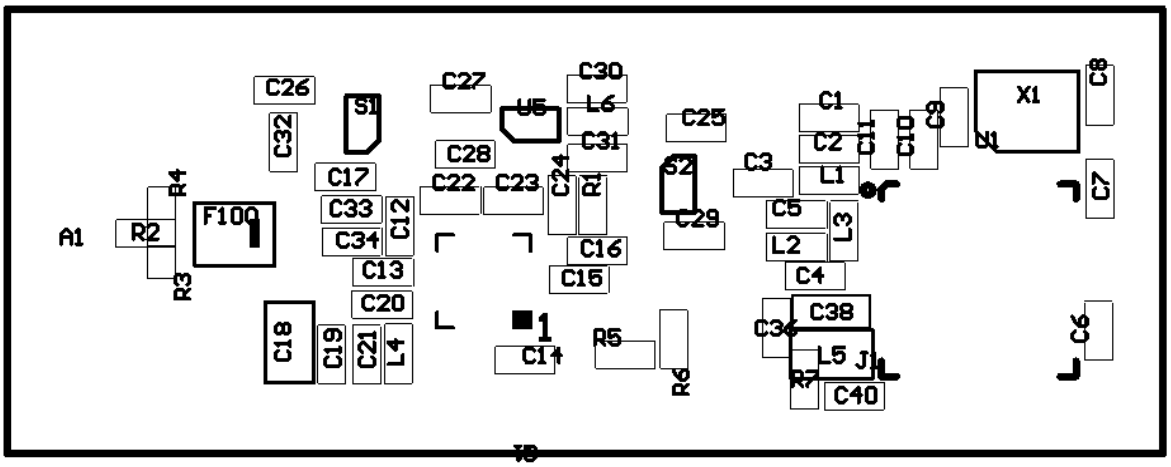

Figure 7. Top Overlay

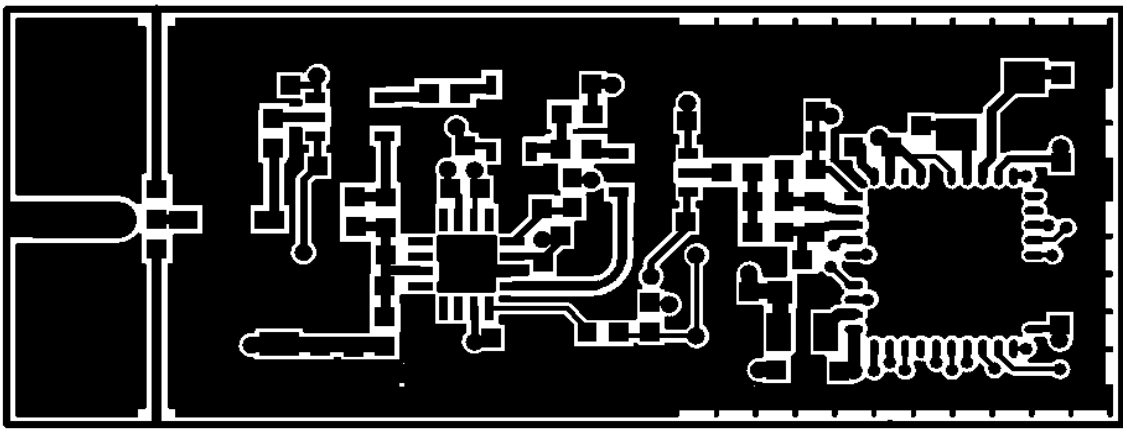

Figure 8. Top Layer (Signals)

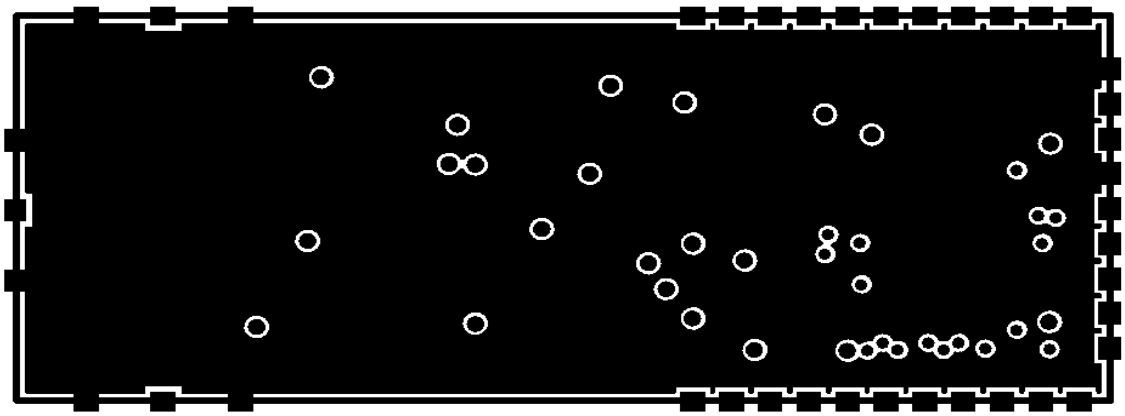

Figure 9. Midlayer2 (GND)

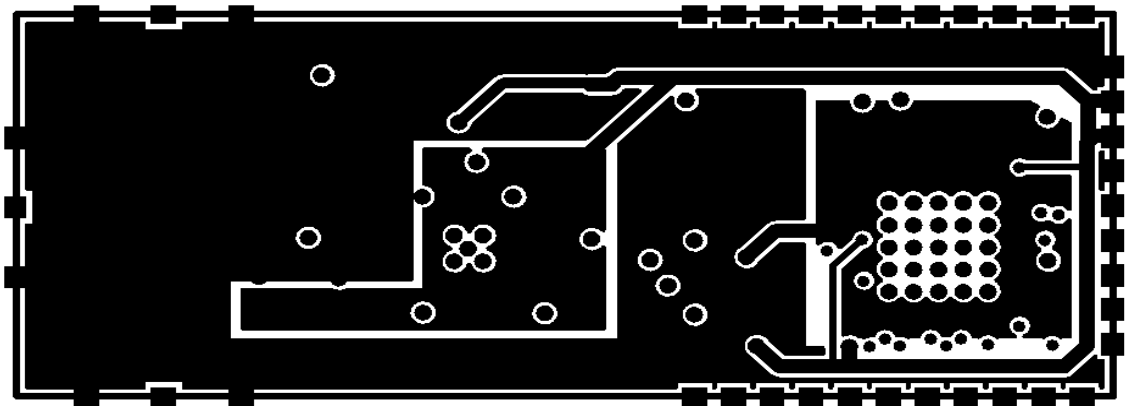

Figure 10. Midlayer3 (Power)

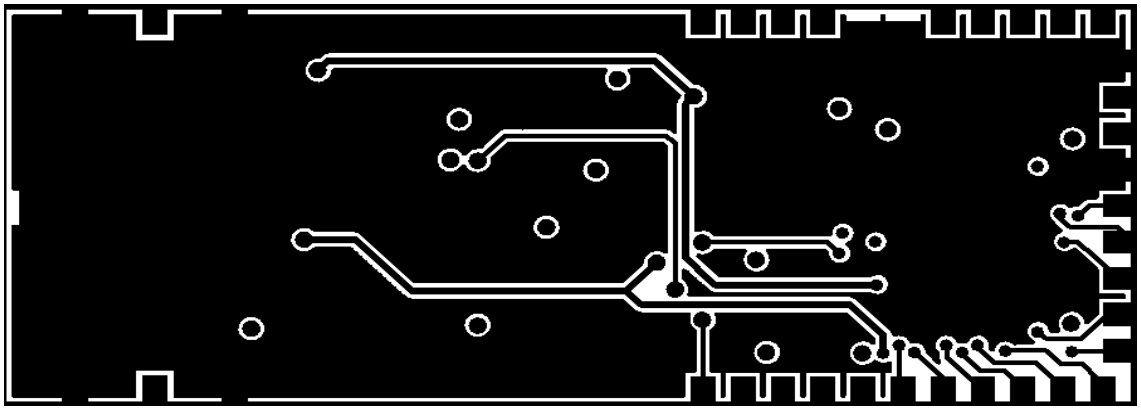

Figure 11. Bottom Layer (Signals and GND)

8. BOM List

Item	Part name	Footprint	Tolerance	Manu-facturer	Vendor Part No.	Qty	Reference
1	100nF	0402	-20~+80%	Yageo	CC0402ZRY5V7BB104	4	C19, C22, C28, C30
2	0.5pF	0402	±0.25pF	Yageo	C0402CRNP09BNR50	4	C4, C5, C20, C24
3	0R	0402	±5%	Yageo	RC0402JR-070R	4	R2, R5, R6, R7
4	1.8pF	0402	±0.25pF	Yageo	CC0402CRNPO9BN1R8	1	C13
5	1pF	0402	±0.25pF	Yageo	CC0402CRNPO9BN1R0	1	C32
6	1uF	0402	-20~+80%	Yageo	C040ZRY5V5BB105	3	C16, C36, C40
7	4.7nH	0402	±0.3nH	Murata	LQG15HN4N7S02	1	L4
8	4.7uF	0603	-20~+80%	Murata	GRM188R61A475K	1	C38
9	4.3nH	0402	±0.3nH	Murata	LQG15HN4N3S02	1	L3
10	12nH	0402	±5%	Murata	LQG15HN12NJ02	2	L1, L2
11	10nF	0402	-20~+80%	Yageo	C0402ZRY5V7BB103	3	C1, C6, C10
12	10pF	0402	±5%	Yageo	CC0402JRNPO9BN100	4	C3, C8, C9, C12
13	10uF	0805	-20~+80%	Yageo	C0805ZKY5V6BB106	1	C18
14	15pF	0402	±5%	Yageo	C0402JRNPO9BN150	4	C17, C25, C26, C29
15	CRYSTAL 32MHz	CX_101F	15ppm/8pF/3.2*2.5mm	NDK	NX3225SA	1	X1
16	33nH	0402	±5%	Murata	LQG15HN33NJ02	1	L6
17	33pF	0402	±5%	Yageo	C0402JRNPO9BN330	1	C23
18	39pF	0402	±5%	Yageo	C0402JRNPO9BN390	1	C11
19	47pF	0402	±5%	Yageo	CC0402JRNPO9BN470	2	C2, C7
20	100k	0402	±5%	Yageo	RC0402JR-07100K	1	R1
21	100pF	0402	±5%	Yageo	C0402JRNPO9BN101	2	C27, C31
22	330pF	0402	±5%	Yageo	CC0402KRX7R9BB331	3	C14, C15, C21
23	SWITCH	SOT363	GaAs/DC-2.5GHz/	Hexawave	HW408	2	S1, S2
24	2.4G_BPF	DEA252450 BT-2031A1	2.4GHz W-LAN	TDK	DEA252450BT-2031A1	1	F100
25	SMA connector	SMA-E	Connector SMA F型 (母頭公PIN)	BO-JIANG	2867LS502BD003R	1	A1
26	UP2206	QFN3*3 16 LEAD		UBEC		1	Q1
27	UA2725	SOT363		UBEC		1	U5
28	UZ2400D	QFN-40		UBEC		1	U1
29	0088-V-U-008-B	PCB	4-L, FR-4, G00033	UBEC		1	
30	RF Shield Cover		Shield Case上蓋	HUN PAI	0019V-C0001	1	
31	RF Shield Frame		Shield Case下蓋	HUN PAI	0019V-F0002	1	

Table 3. BOM List of U-Power1000D Module

9. Mechanical Dimension

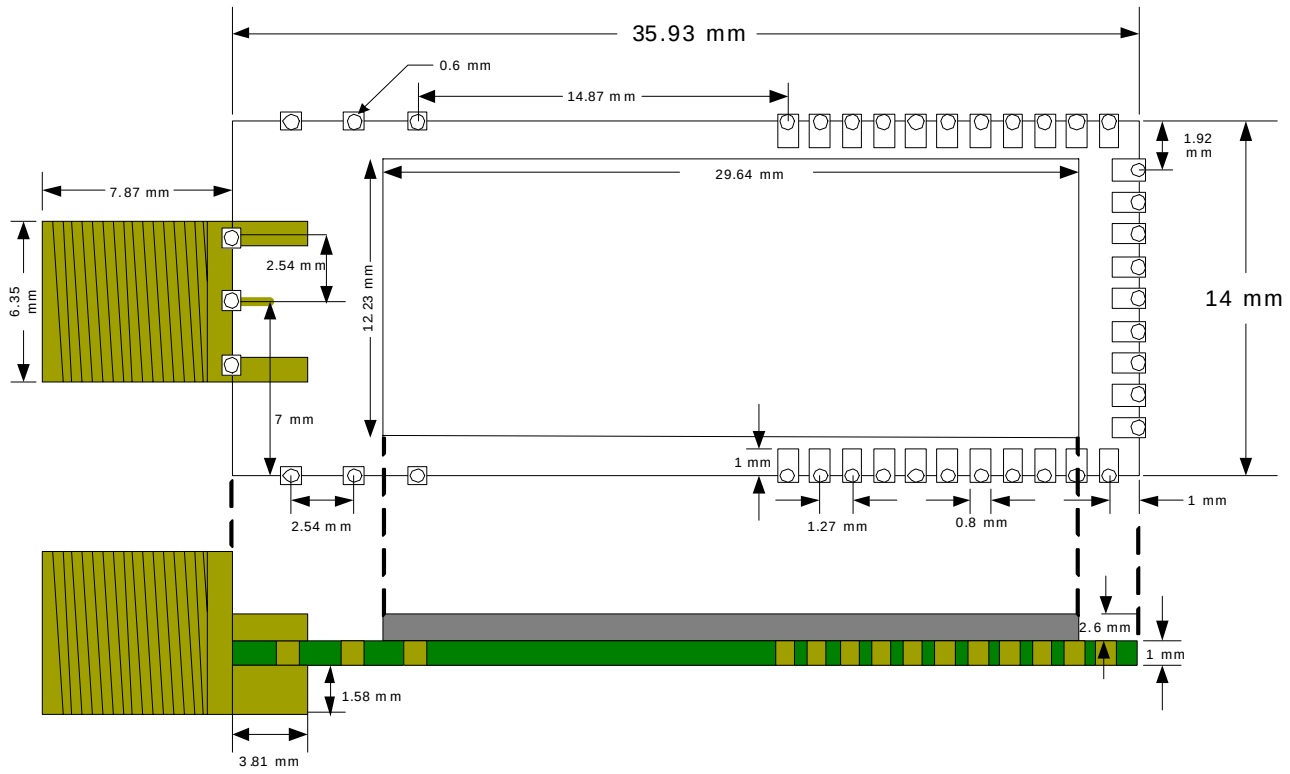

Figure 12. Dimensions of U-Power1000D Module

10. Dot-Power1000D Module

10.1. General Introduction

The Dot-Power1000D module is derived from the U-Power1000D module by attaching a pin-header 2x14 (pitch: 2.54mm) to the interface board. RF connectors including SMA and SMC can be implemented. Through the GSG (ground-signal-ground) interface on the U-Force module, the RF loss is kept to less than 0.3dB. Because of the flexibility offered by the interface boards, Dot-Power1000D module can be readily used for various applications.

Figure 13. Top View of Dot-Power1000D Module with Shielding Case

10.2. Pin Header Information

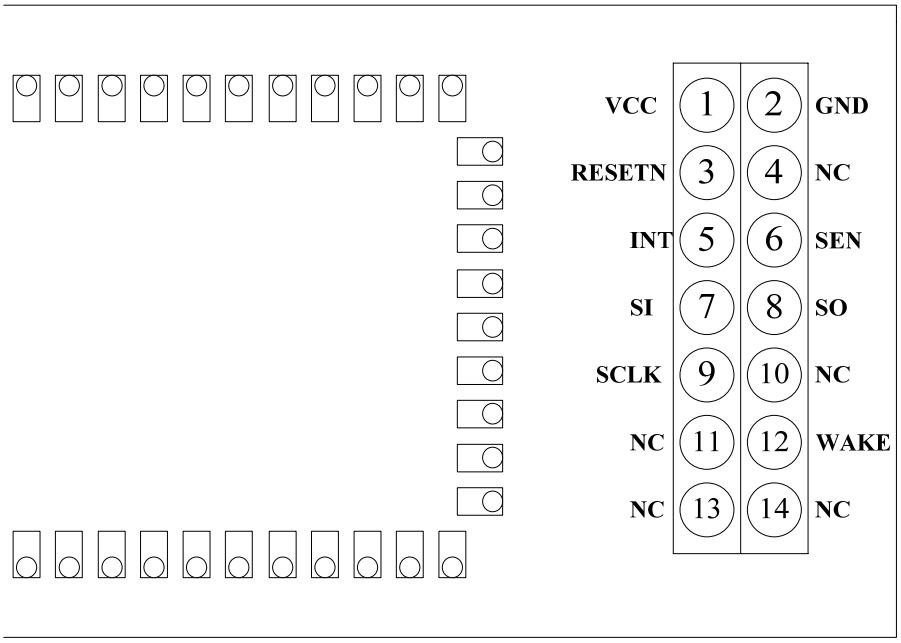

Figure 14. Pin Header Map

10.3. Mechanical Dimension

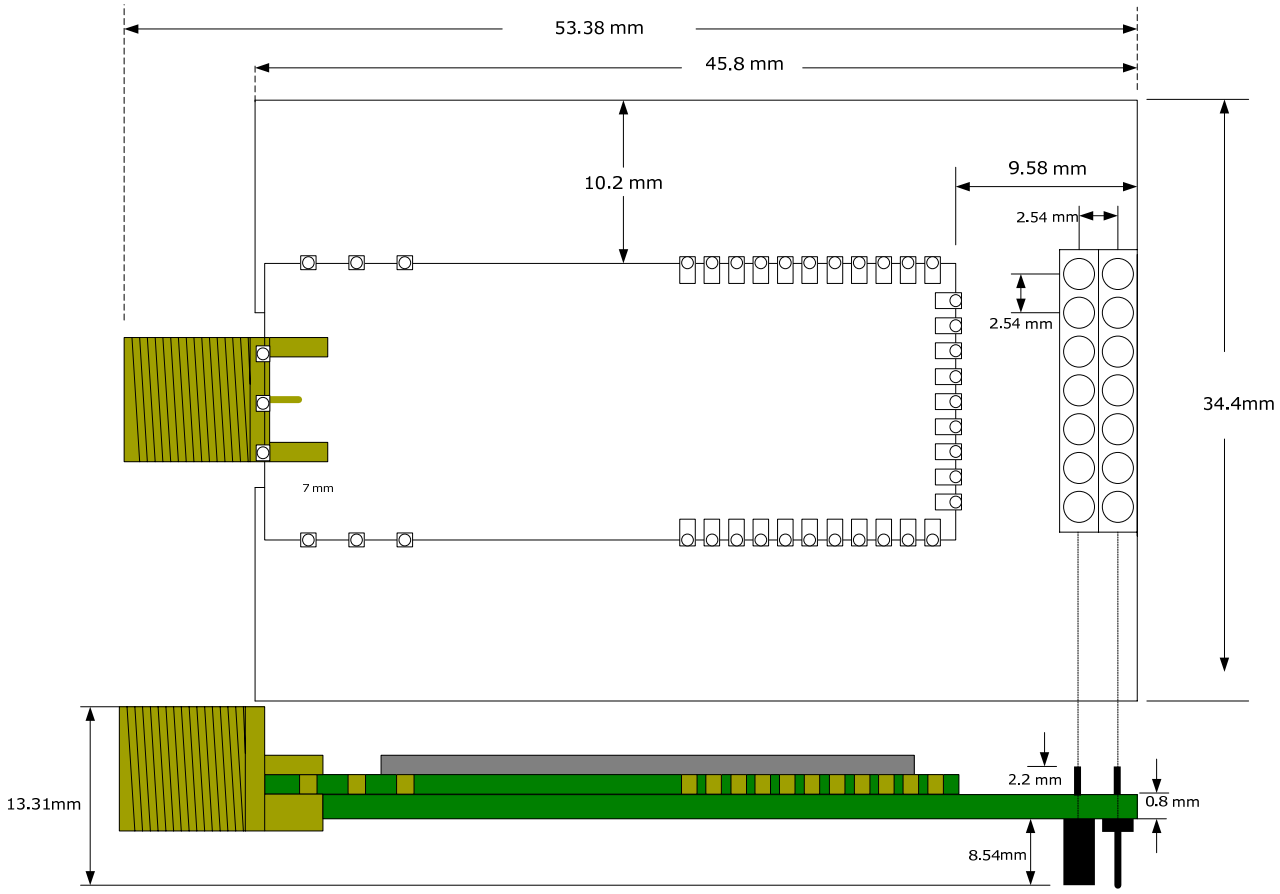

Figure 15. Dimensions of Dot-Power1000D

Appendix A. TX Power Configuration

If the TX power is inadequate for the initial register settings, user can set the PA gain using Table A-1 where different output power offsets are listed.

Tx Output Power Register Control			
LREG0x203<7:3>	**LREG0x253<3:0>**	**LREG0x274<7:0>**	**Tx Output Power offset (dB)**
0xF8	0x0B	0xC6	+2
	0x0B	0xB6	+1
	0x0B	0xA6	0 (initial setting)
	0x0D	0x96	-1
	0x09	0x96	-2
	0x0F	0x8A	-3
	0x0C	0x8A	-4
	0x0A	0x8A	-5
	0x08	0x8A	-6

Table A-1. Gain Table of U-Power1000D

Revision History

Revision	Date	Description of Change
0.0	2009/10/26	Initial release.

Contact UBEC:

Headquarters
Address: 6F-1, No. 192, Dongguang Rd., Hsinchu, 300 Taiwan
Tel: +886-3-5729898
Fax:+886-3-5718599
Website: http://www.ubec.com.tw

Sales Services
Tel: +886-3-5729898
Fax:+886-3-5718599
E-mail: sales@ubec.com.tw

FAE Services
Tel: +886-3-5729898
Fax: +886-3-5718599
E-mail: fae@ubec.com.tw

DISCLAIMER