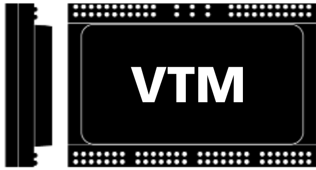
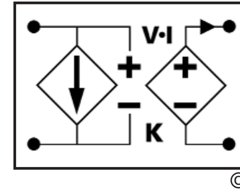


V•I Chip™ – VTM
Voltage Transformation Module

V048K020T080

K indicates BGA configuration. For other mounting options see Part Numbering below.



©

V_f = 26 - 55 V
V_{OUT} = 1.1 - 2.3 V
I_{OUT} = 80 A
K = 1/24
R_{OUT} = 1.5 mΩ max

- 48 V to 2 V V•I Chip Converter
- 80 A (120 A for 1 ms)
- High density – 320 A/in³
- Small footprint – 75 A/in²
- Low weight – 0.5 oz (14 g)
- Pick & Place / SMD
- 125°C operation
- 1 µs transient response
- >3.5 million hours MTBF
- Typical efficiency 94% at 2 V/50 A
- No output filtering required
- BGA or J-Lead packages

Actual size

Product Description

The V048K020T080 V•I Chip Voltage Transformation Module (VTM) breaks records for speed, density and efficiency to meet the demands of advanced DSP, FPGA, ASIC, processor cores and microprocessor applications at the point of load (POL) while providing isolation from input to output. It achieves a response time of less than 1 µs and delivers up to 80 A in a volume of less than 0.25 in³ while providing low output voltages with unprecedented efficiency. It may be paralleled to deliver hundreds of amps at an output voltage settable from 1.1 to 2.3 Vdc.

The VTM V048K020T080's nominal output voltage is 2 Vdc from a 48 Vdc input factorized bus, V_f, and is controllable from 1.1 to 2.3 Vdc at no load, and from 1.1 to 2.2 Vdc at full load, over a V_f input range of 26 to 55 Vdc. It can be operated either open- or closed-loop depending on the output regulation needs of the application. Operating open-loop, the output voltage tracks its V_f input voltage with a transformation ratio, K = 1/24, and an output resistance, R_{OUT} = 1.3 milliohm, to enable applications requiring a programmable low output voltage at high current and high efficiency. Closing the loop back to an input Pre-Regulation Module (PRM) or DC-DC converter can compensate for R_{OUT}.

The 2 V VTM achieves break-through current density of 320 A/in³ in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The V•I Chip BGA package supports in-board mounting with a low profile of 0.16" (4 mm) over the board. A J-lead package option supports on-board surface mounting with a profile of only 0.25" (6 mm) over the board. The VTM's fast dynamic response and low noise eliminate the need for bulk capacitance at the load, substantially increasing the POL density while improving reliability and decreasing cost.

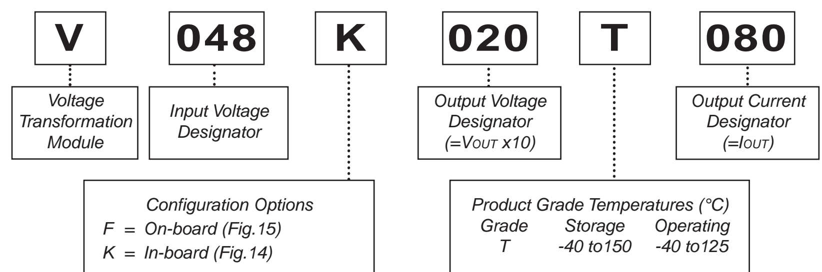
Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60.0	Vdc	
+In to -In	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
TM to -In	-0.3 to 7.0	Vdc	
VC to -In	-0.3 to 19.0	Vdc	
+Out to -Out	-0.1 to 4.0	Vdc	
Isolation voltage	2,250	Vdc	Input to Output
Operating junction temperature	-40 to 125	°C	See Note
Output current	80	A	Continuous
Peak output current	120	A	For 1 ms
Case temperature during reflow	208	°C	
Storage temperature	-40 to 150	°C	
Output power	174	W	Continuous
Peak output power	261	W	For 1 ms

Note: The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by the temperature monitor (TM) signal and by a shutdown comparator.

PRELIMINARY

Part Numbering



Specifications

■ INPUT (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	26	48	55	Vdc	Operable down to zero V with external bias voltage
Input dV/dt			1	V/µs	
Input overvoltage turn-on	56.0			Vdc	
Input overvoltage turn-off			59.5	Vdc	
Input current			3.7	Adc	
Input reflected ripple current		170		mA p-p	Using test circuit in Fig.16; See Fig.1
No load power dissipation		2.50	3.15	W	
Internal input capacitance		4		µF	
Internal input inductance		20		nH	

■ OUTPUT (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Rated DC current	0		80	Adc	
Peak repetitive current			120	A	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
DC current limit	82	99	112	Adc	
Current share accuracy		5	10	%	See Parallel Operation on page 10
Efficiency					
Half load	94.0	94.2		%	See Fig.3, 2 Vout
Full load	93.0	93.2		%	See Fig.3, 2 Vout
Internal output inductance		0.8		nH	
Internal output capacitance		306		µF	Effective value
Load capacitance			56,300	µF	
Output overvoltage setpoint		2.33		Vdc	
Output ripple voltage					
No external bypass		53	65	mV	See Figs.2 and 5
100 µF bypass capacitor		2		mV	See Fig.6
Effective switching frequency	2.52	2.65	2.78	MHz	Fixed, 1.33 MHz per phase
Line regulation					
K	0.0413	1/24	0.0421		$V_{OUT} = K \bullet V_{IN}$ at no load
Load regulation					
R_{OUT}		1.3	1.5	mΩ	See Fig.19
Transient response					
Voltage overshoot		20		mV	80 A load step with 100 µF C_{IN}; See Figs.7 and 8
Response time		200		ns	See Figs.7 and 8
Recovery time		1		µs	See Figs.7 and 8

PRELIMINARY

■ WAVEFORMS

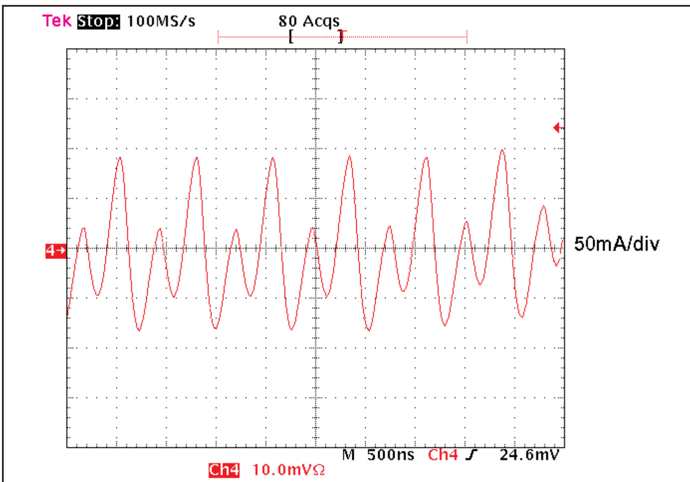


Figure 1— Input reflected ripple current at full load and 48 Vin

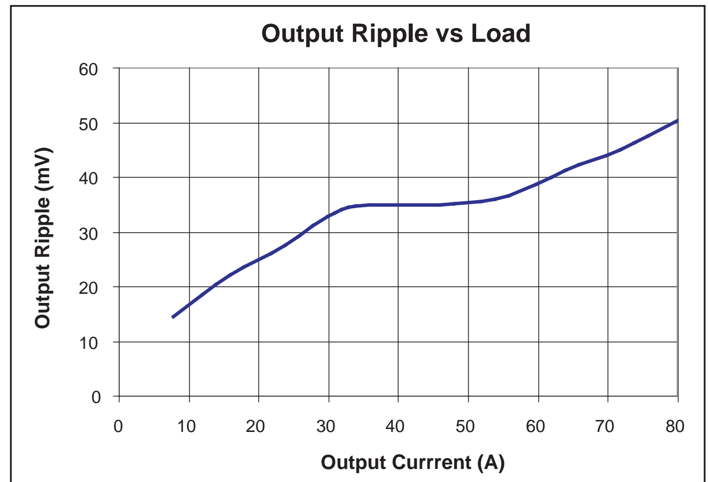


Figure 2— Output voltage ripple vs. output current at 2 Vout with no POL bypass capacitance.

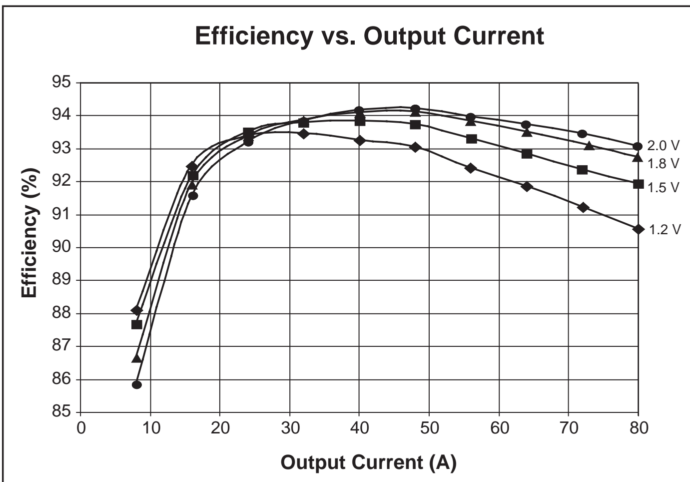


Figure 3— Efficiency vs. output current and output voltage

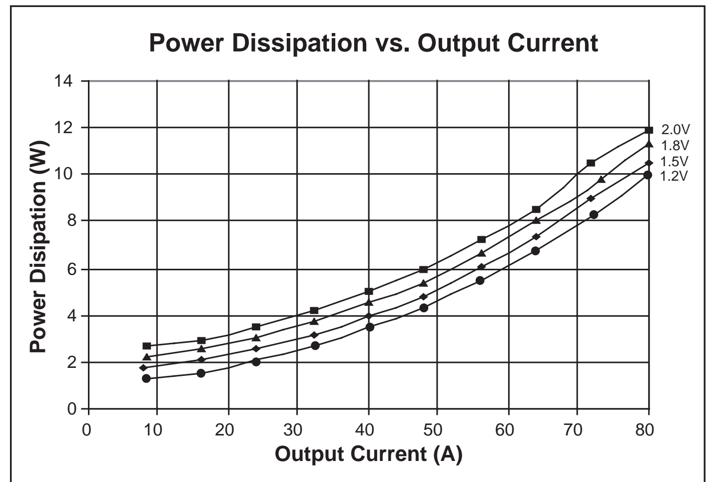


Figure 4—Power dissipation as a function of output current and output voltage

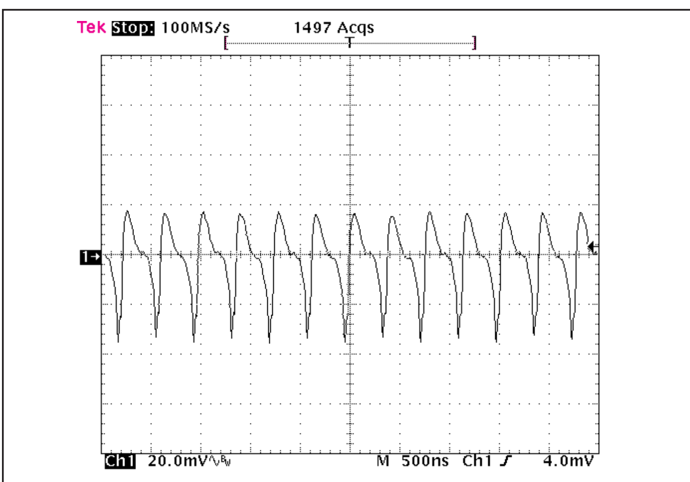


Figure 5— Output voltage ripple at full load and 2 Vout; without any external bypass capacitor.

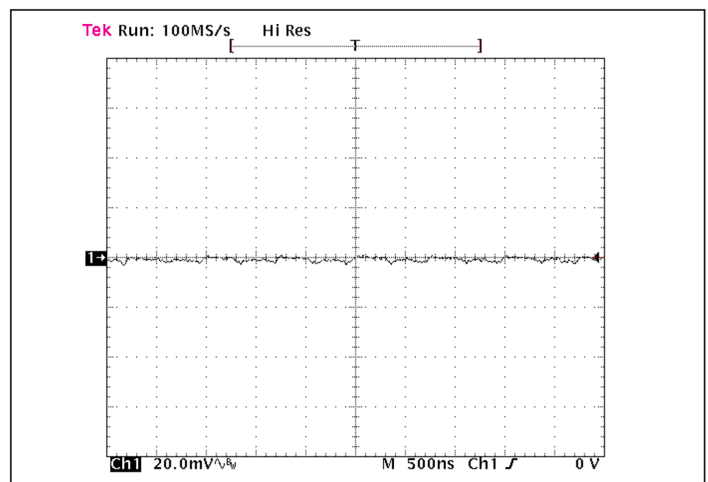


Figure 6—Output voltage ripple at full load and 2 Vout with 100 µF ceramic external bypass capacitance and 20 nH distribution inductance.

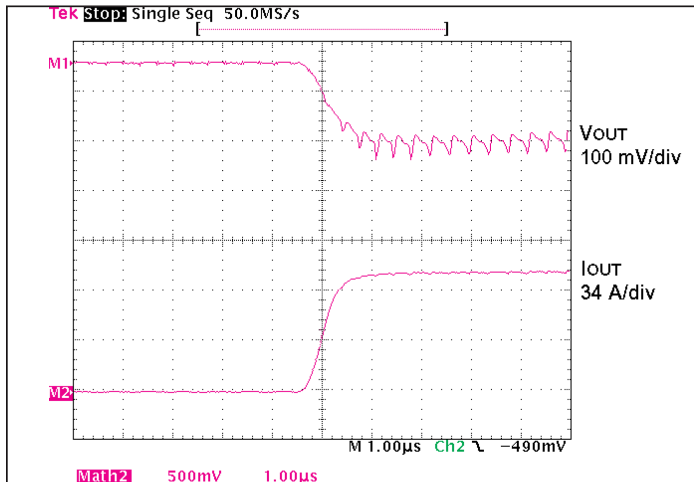


Figure 7— 0-80 A step load change with 100 µF input capacitance and no output capacitance.

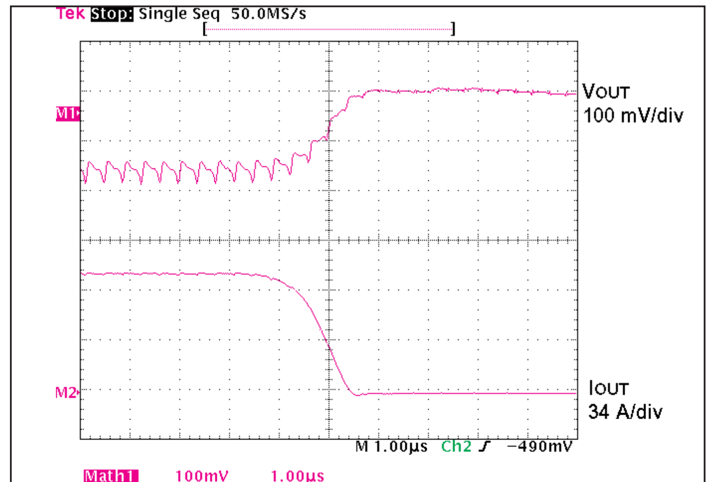


Figure 8— 80-0 A step load change with 100 µF input capacitance and no output capacitance.

GENERAL

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		3.5		Mhrs	25°C, GB
Isolation specifications					
Voltage	2,250			Vdc	Input to Output
Capacitance		2,500		pF	Input to Output
Resistance	10			MΩ	Input to Output
Agency approvals (pending)		cTÜVus			UL/CSA 60950, EN 60950
		CE Mark			Low voltage directive
Mechanical parameters					See mechanical drawing, Figs.10 and 12
Weight		0.5 / 14.0		oz / g	
Dimensions(BGA version)					
Length		1.26 / 32		in / mm	
Width		0.85 / 21.5		in / mm	
Height		0.23 / 5.9		in / mm	

Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary Control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	
Current limit	2.4	2.5	2.9	mA	Source only
Disable delay time		4	10	µs	PC low to Vout low
Temperature Monitor (TM)					
27°C setting		3.00		Vdc	Operating junction temperature
Temperature coefficient		10		mV/°C	
Full range accuracy		±5		°C	Operating junction temperature
Current limit	100			µA	Source only
VTM Control (VC)					
External boost voltage	12.0	14.0	19.0	Vdc	Required for VTM start up without PRM
External boost duration		10		ms	Vin must be >26 V for VTM to remain operating without boost voltage.

THERMAL

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Over temperature shutdown	125	130	135	°C	Junction temperature
	Thermal capacity		0.61		Ws/°C	
$R_{\theta JC}$	Junction-to-case thermal impedance		1.1		°C/W	
$R_{\theta JB}$	Junction-to-BGA thermal impedance		2.1		°C/W	
$R_{\theta JA}$	Junction-to-ambient [1]		6.5		°C/W	
$R_{\theta JA}$	Junction-to-ambient [2]		5.0		°C/W	

Notes

1. V048K020T080 surface mounted in-board to a 2" x 2" FR4 board, 4 layers 2 oz Cu, 300 LFM.
2. V048K020T080 with a 0.25"H heatsink surface mounted on FR4 board, 300 LFM.

V•I CHIP STRESS DRIVEN PRODUCT QUALIFICATION PROCESS

Test	Standard	Environment
High Temperature Operational Life (HTOL)	JESD22-A-108-B	125°C, Vmax, 1,008 hrs
Temperature cycling	JESD22-A-104B	-55°C to 125°C, 1,000 cycles
High temperature storage	JESD22-A-103A	150°C, 1,000 hrs
Moisture resistance	JESD22-A113-B	Moisture sensitivity Level 5
Temperature Humidity Bias Testing (THB)	EIA/JESD22-A-101-B	85°C, 85% RH, Vmax, 1,008 hrs
Pressure cooker testing (Autoclave)	JESD22-A-102-C	121°C, 100% RH, 15 PSIG, 96 hrs
Highly Accelerated Stress Testing (HAST)	JESD22-A-110B	130°C, 85% RH, Vmax, 96 hrs
Solvent resistance/marking permanency	JESD22-B-107-A	Solvents A, B & C as defined
Mechanical vibration	JESD22-B-103-A	20g peak, 20-2,000 Hz, test in X, Y & Z directions
Mechanical shock	JESD22-B-104-A	1,500g peak 0.5 ms pulse duration, 5 pulses in 6 directions
Electro static discharge testing – human body model	EIA/JESD22-A114-A	Meets or exceeds 2,000 Volts
Electro static discharge testing – machine model	EIA/JESD22-A115-A	Meets or exceeds 200 Volts
Highly Accelerated Life Testing (HALT)	Per Vicor Internal Test Specification*	Operation limits verified, destruct margin determined
Dynamic cycling	Per Vicor internal test specification*	Constant line, 0-100% load, -20°C to 125°C

* For details of the test protocols see Vicor's website.

PRELIMINARY

V•I CHIP BALL GRID ARRAY INTERCONNECT QUALIFICATION

Test	Standard	Environment
BGA solder fatigue evaluation	IPC-9701 IPC-SM-785	Cycle condition: TC3 (-40 to +125°C) Test duration: NTC-B (500 failure free cycles)
Solder ball shear test	IPC-9701	Failure through bulk solder or copper pad lift-off

PRELIMINARY

+IN/-IN DC VOLTAGE PORTS

The VTM input should not exceed the high end of the range specified. Be aware of this limit in applications where the VTM is being driven above its nominal output voltage. A 14 V source must be applied to the VC pin and voltage must be present at the +In and -In ports in order for the VTM to process power. If the input voltage exceeds the over voltage lock-out, the VTM will shutdown. The VTM does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

VC – VTM Control

The VC port is multiplexed. It receives the initial Vcc voltage from an upstream PRM, synchronizing the output rise of the VTM with the output rise of the PRM. Additionally, the VC port provides feedback to the PRM to compensate for the VTM output resistance. In typical applications using VTMs powered from PRMs, the PRM's VC port should be connected to the VTM VC port.

In applications where a VTM is being used without a PRM, 14 V must be supplied to the VC port for approximately 10 ms in order for the VTM to startup. The VTM can be operated at input voltages below 26 V as long as the VC voltage is applied.

PC – Primary Control

The Primary Control (PC) pin is a multifunction pin for controlling the VTM as follows:

Disable – If the PC is left floating, the VTM output is enabled. To disable the output, the PC pin must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC pin. Once disabled, 14 V must be re-applied to the VC pin in order to restart the VTM

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5 Vdc.

TM – Temperature Monitor

The Temperature Monitor (TM) provides a linear output proportional to the internal temperature of the VTM. At 300ºK (+27ºC) the TM output is 3.0 V referenced to -In and varies 10 mV/ºC. TM accuracy is +/-5ºC. This feature is useful for validating the thermal design of the system as well as monitoring the VTM temperature in the final application.

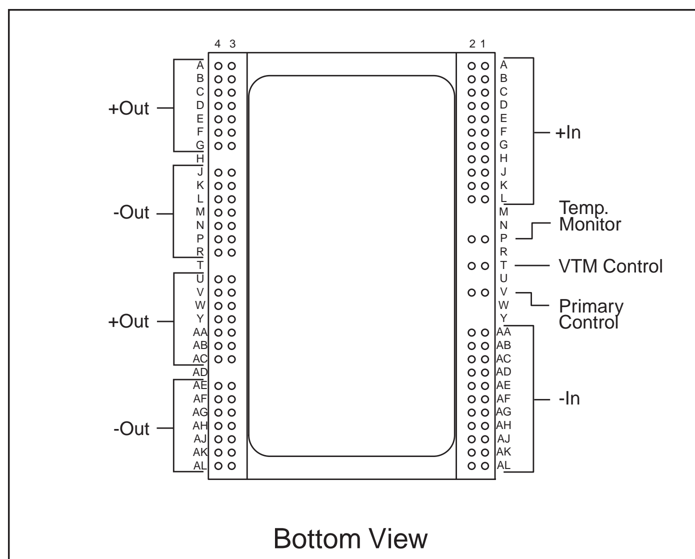


Figure 9—VTM BGA configuration

Signal Name	BGA Designation
+In	A1-L1, A2-L2
–In	AA1-AL1, AA2-AL2
TM	P1, P2
VC	T1, T2
PC	V1, V2
+Out	A3-G3, A4-G4, U3-AC3, U4-AC4
–Out	J3-R3, J4-R4, AE3-AL3, AE4-AL4

+OUT/-OUT DC Voltage Output Ports

The output (+OUT) and output return (-OUT) are through two sets of contact locations. The respective +OUT and –OUT groups must be connected in parallel with as low an interconnect resistance as possible. Within the specified input voltage range, the Level 1 DC behavioral model shown in Figure 19 defines the output voltage of the VTM. The current source capability of the VTM is shown in the specification table.

To take full advantage of the VTM, the user should note the low output impedance of the device. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.

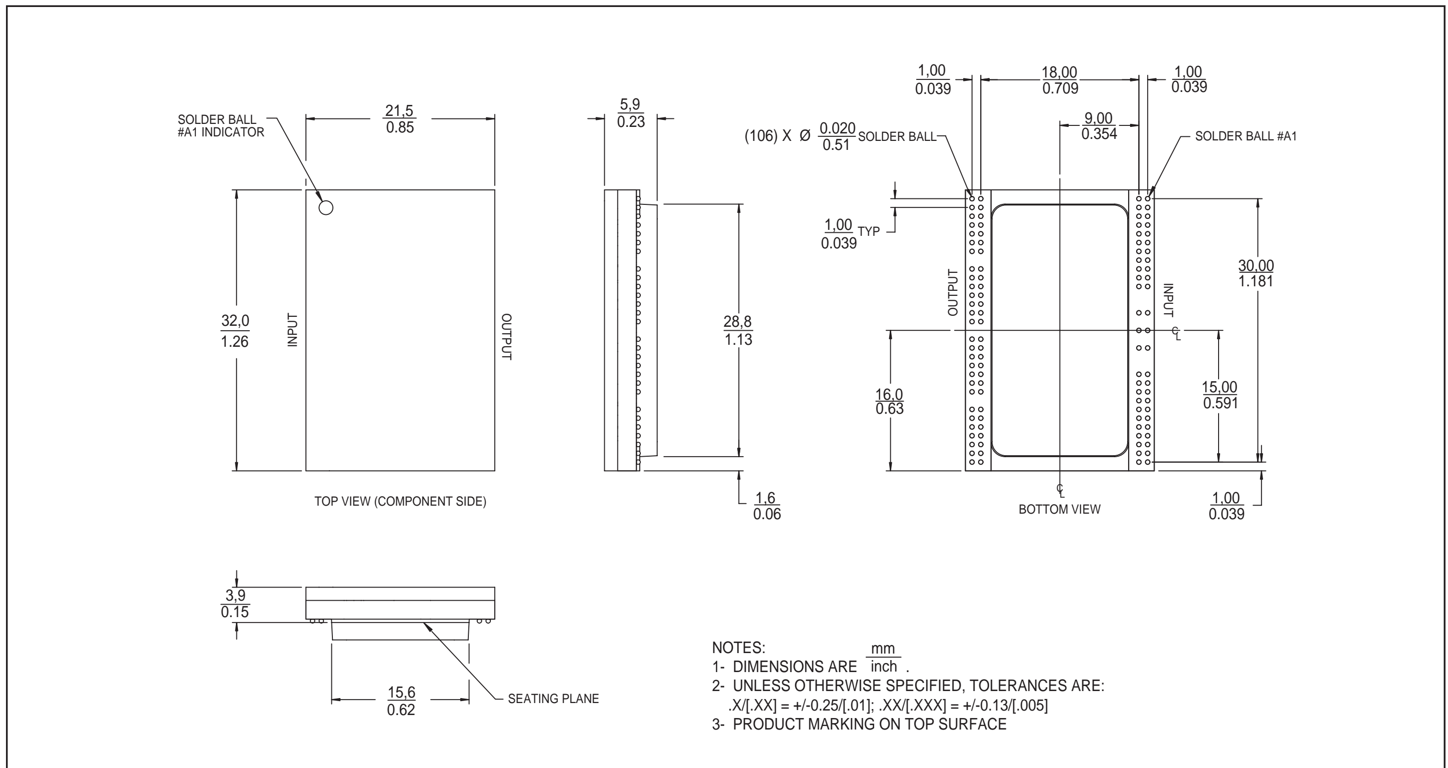


Figure 10—VTM BGA mechanical outline; In-board mounting

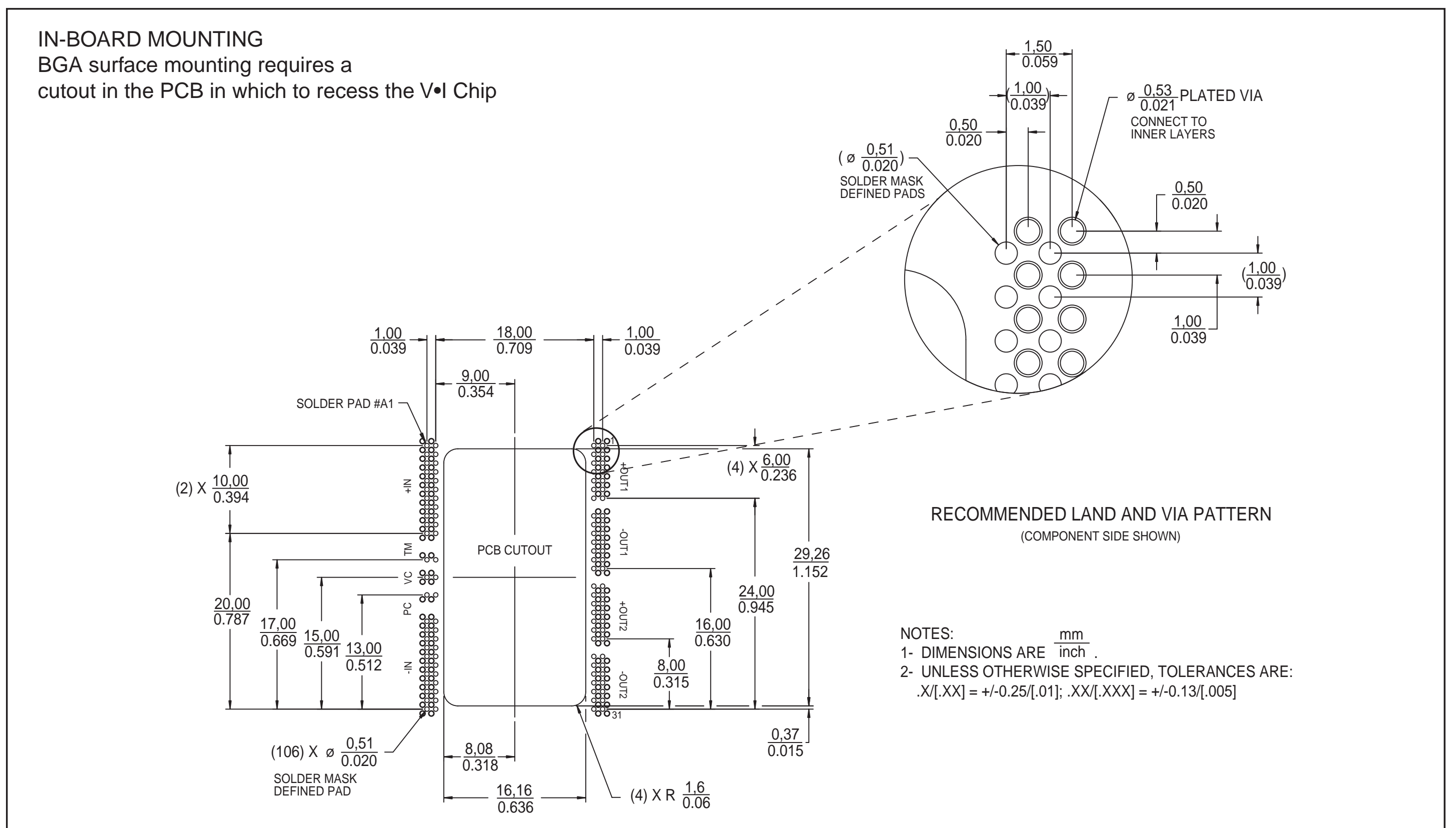


Figure 11— VTM BGA PCB land/VIA layout information; In-board mounting

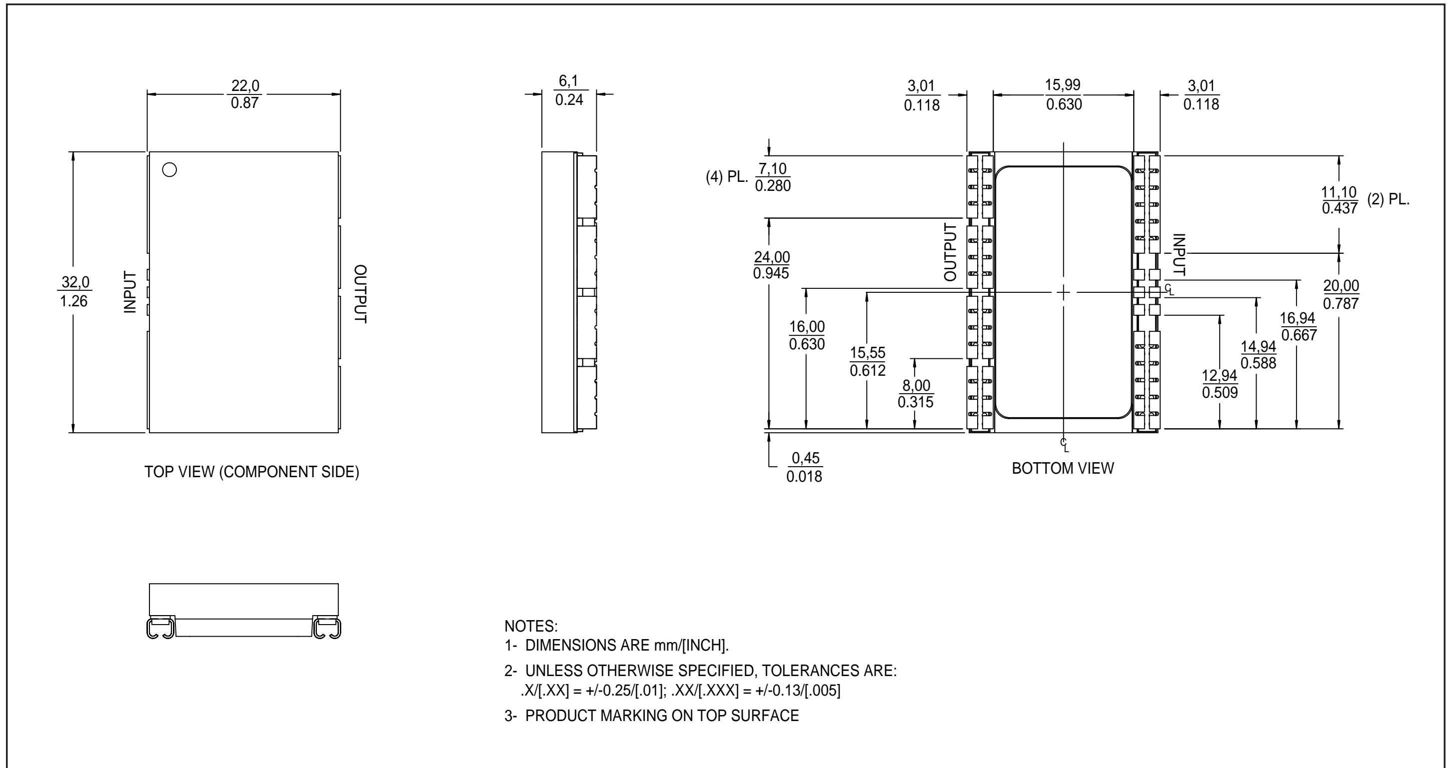


Figure 12*—VTM J-lead mechanical outline; On-board mounting*

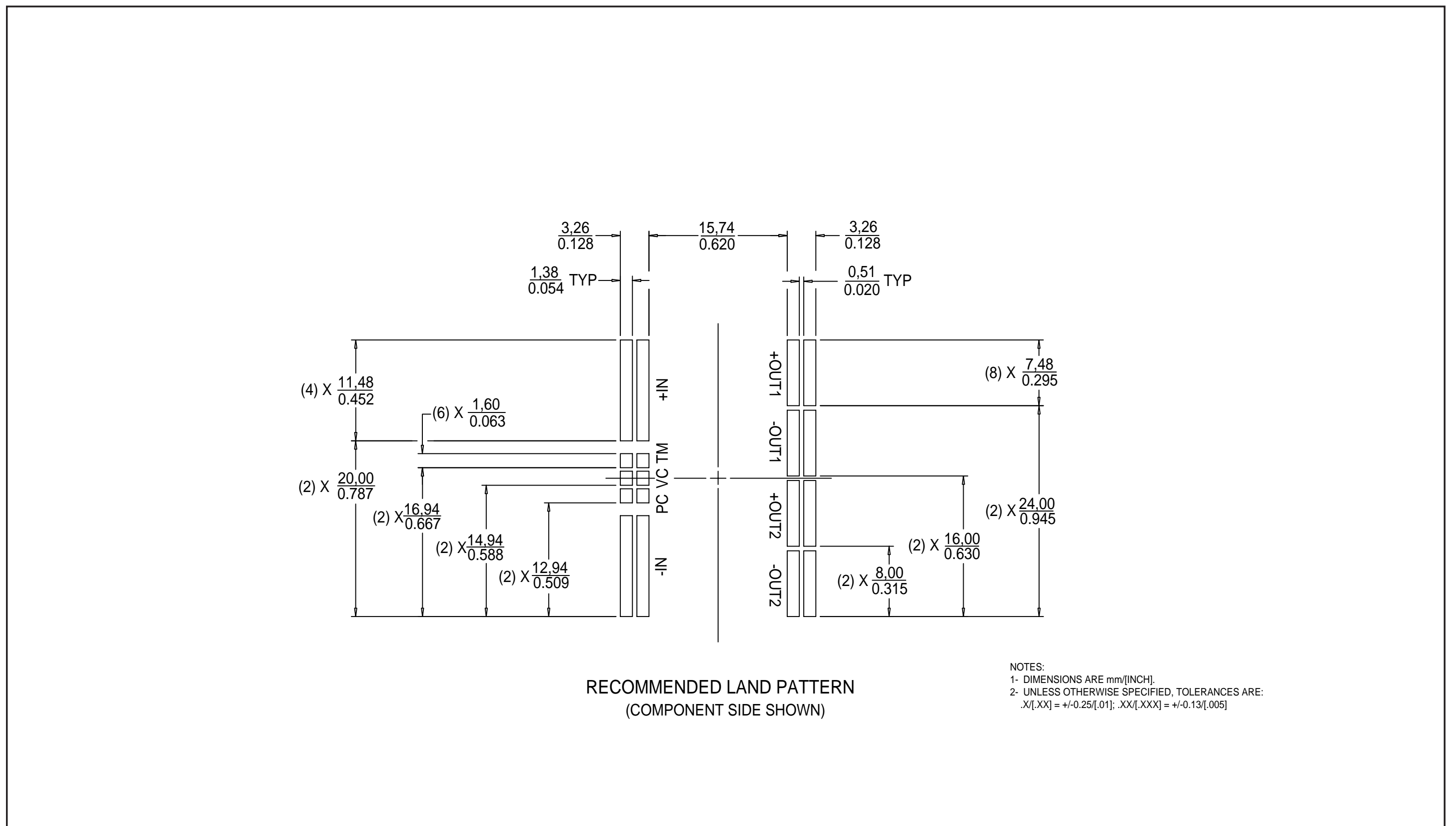


Figure 13*— VTM J-lead PCB land layout information; On-board mounting*

CONFIGURATION OPTIONS

CONFIGURATION	IN-BOARD* (Fig. 14)	ON-BOARD* (Fig. 15)	IN-BOARD WITH 0.25" HEATSINK	ON-BOARD WITH 0.25" HEATSINK
Effective Current Density	467 A/in^3	292 A/in^3	182 A/in^3	146 A/in^3
Junction-Board Thermal Resistance	2.1 °C/W	2.4 °C/W	2.1 °C/W	2.4 °C/W
Junction-Case Thermal Resistance	1.1 °C/W	1.1 °C/W	N/A	N/A
Junction-Ambient Thermal Resistance 300LFM	6.5 °C/W	6.8 °C/W	5.0 °C/W	5.0 °C/W

*Surface mounted to a 2" x 2" FR4 board, 4 layers 2 oz Cu

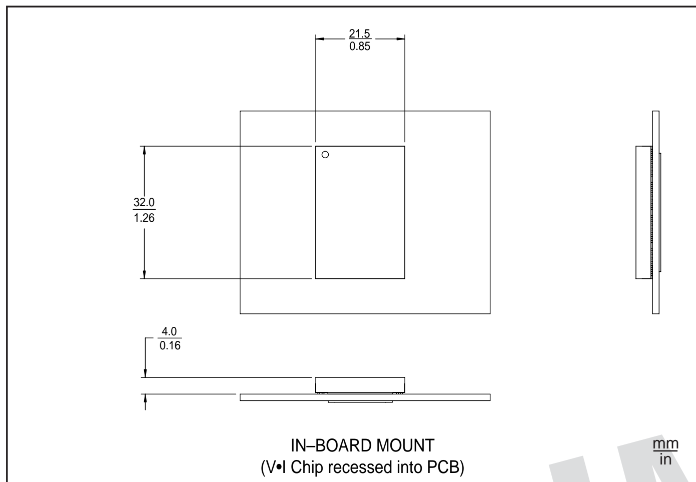


Figure 14*—In-board mounting – package K*

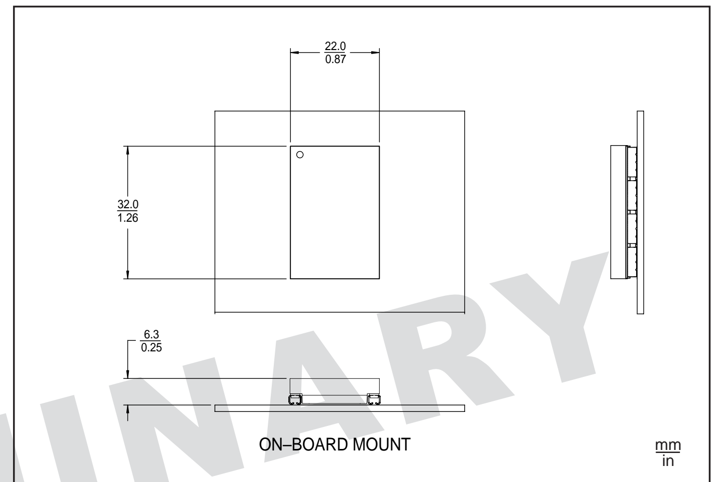


Figure 15*—On-board mounting – package F*

PRELIMINARY

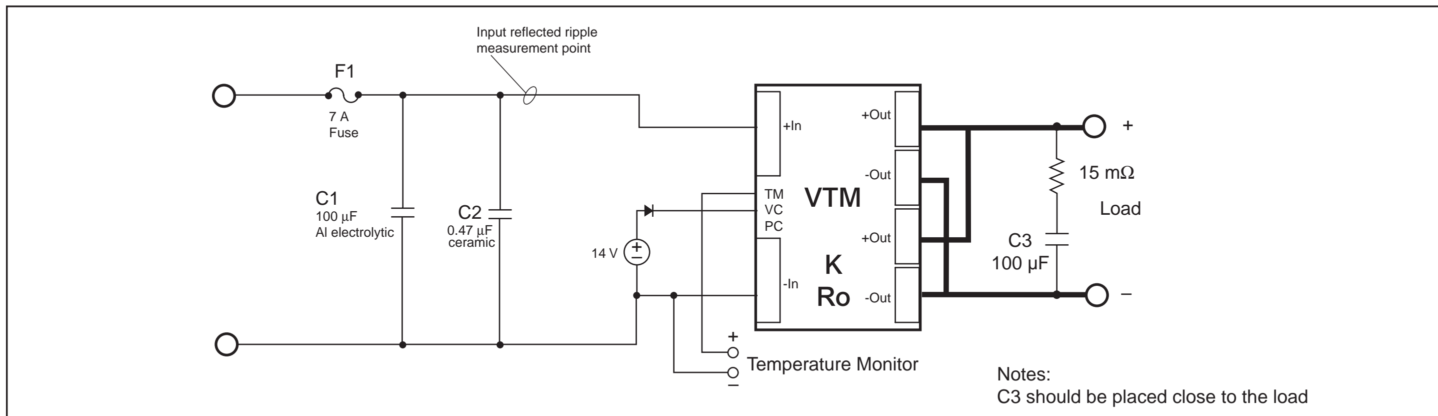


Figure 16*—VTM test circuit*

Application Note

Parallel Operation

In applications requiring higher current or redundancy, VTMs can be operated in parallel without adding control circuitry or signal lines. To maximize current sharing accuracy, it is imperative that the source and load impedance on each VTM in a parallel array be equal. If VTMs are being fed by an upstream PRM, the VC nodes of all VTMs must be connectd to the PRM VC.

To achieve matched impedances, dedicated power planes within the PC board should be used for the output and output return paths to the array of paralleled VTMs. This technique is preferable to using traces of varying size and length.

The VTM power train and control architecture allow bi-directional power transfer when the VTM is operating within its specified ranges. Bi-directional power processing improves transient response in the event of an output load dump. The VTM may operate in reverse, returning output power back to the input source. It does so efficiently.

Thermal Management

The high efficiency of the VTM results in low power dissipation minimizing temperature rise, even at full output current. The heat generated within the internal semiconductor junctions is coupled through very low thermal resistances, $R\theta_{JC}$ and $R\theta_{JB}$ (see Figure 17), to the PC board allowing flexible thermal management.

CASE 1 Convection via optional heatsink to air

In an environment with forced convection over the surface of a PCB with 0.4" of headroom, a VTM with a 0.25 heat sink offers a simple thermal management option. The total Junction toAmbient thermal resistance of a surface mounted V048K020T080 with a heat sink attached is 4.8 ºC/W in 300 LFMairflow, (see Figure 18).

At 2 Vout and full rated current (80A), the VTM dissipates approximately 12 W per Figure 4. This results in a temperature rise of approximately 56 ºC, allowing operation in an air temperature of 69 ºC without exceeding the 125 ºC max junction temperature.

CASE 2 Conduction via the PC board to air

The low Junction to BGA thermal resistance allows the use of the PC board as a means of removing heat from the VTM. Convection from the PC board to ambient, or conduction to a cold plate, enable flexible thermal management options.

With a VTM mounted on a 2.0 in^2 area of a multi-layer PC board with appropriate power planes resulting in 8 oz of effective copper weight, the Junction-to-BGA thermal resistance, $R\theta_{JA}$, is 6.5 ºC/W in 300 LFM of air. With a maximum junction temperature of 125 ºC and 12 W of dissipation at full current of 80 A, the resulting temperature rise of 76 ºC allows the VTM to operate at full rated current up to a 49 ºC ambient temperature. See thermal resistances on page 9 for additional details on this thermal management option.

Adding low-profile heat sinks to the PC board can lower the thermal resistance of the PC board surrounding the VTM. Additional cooling may be added by coupling a cold plate to the PC board with low thermal resistance stand offs.

CASE 3 Combined direct convection to the air and conduction to the PC board.

A combination of cooling techniques that utilize the power planes and dissipation to the air will also reduce the total thermal impedance. This is the most effective cooling method. To estimate the total effect of the combination, treat each cooling branch as one leg of a parallel resistor network.

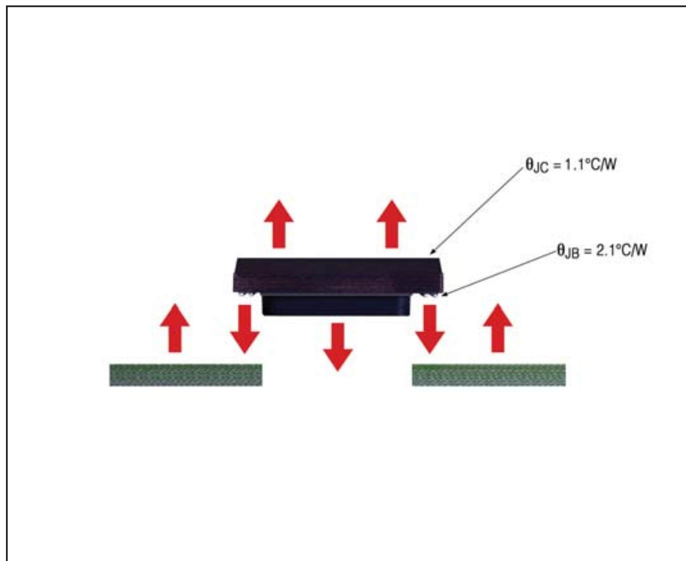


Figure 17—Thermal resistance

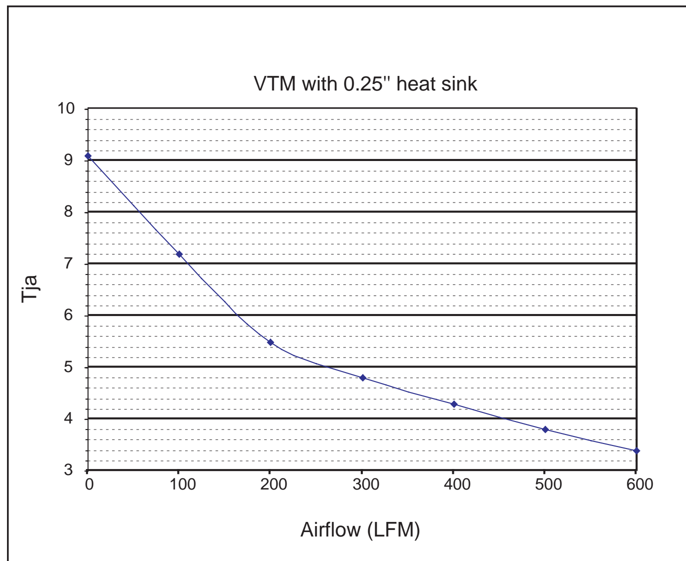


Figure 18—Junction-to-ambient thermal resistance of VTM with 0.25" Heat Sink.

■ V•I Chip VTM LEVEL 1 DC BEHAVIORAL MODEL for 48V to 2V, 80A

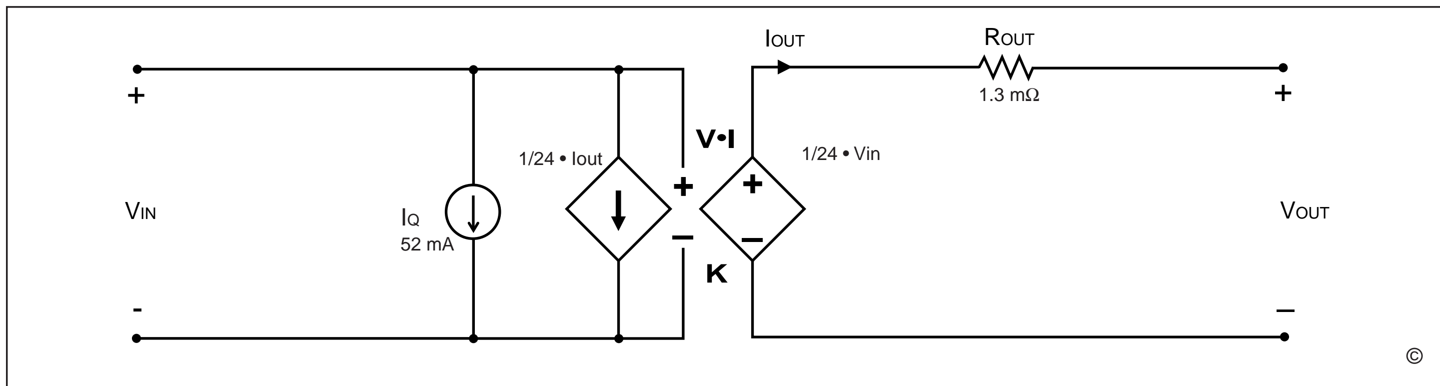


Figure 19—This model characterizes the DC operation of the V•I Chip VTM, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.

■ V•I Chip VTM LEVEL 2 TRANSIENT BEHAVIORAL MODEL for 48V to 2V, 80A

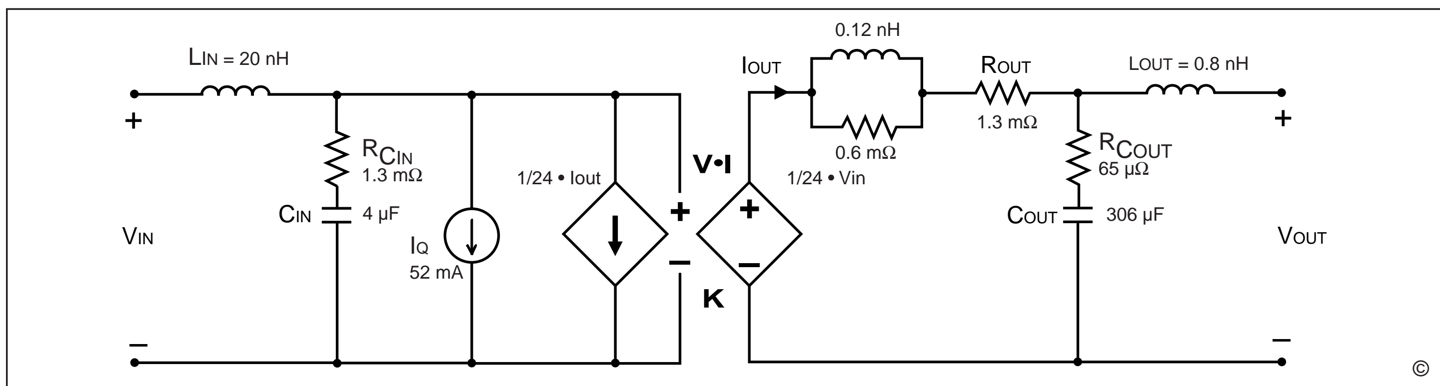


Figure 20—This model characterizes the AC operation of the V•I Chip VTM including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.

In figures 21 – 24;

K = VTM Transformation Ratio

Ro = VTM Output Resistance

Vf = PRM Output (Factorized Bus Voltage)

Vo = VTM Output

VL = Desired Load Voltage

FPA Adaptive Loop

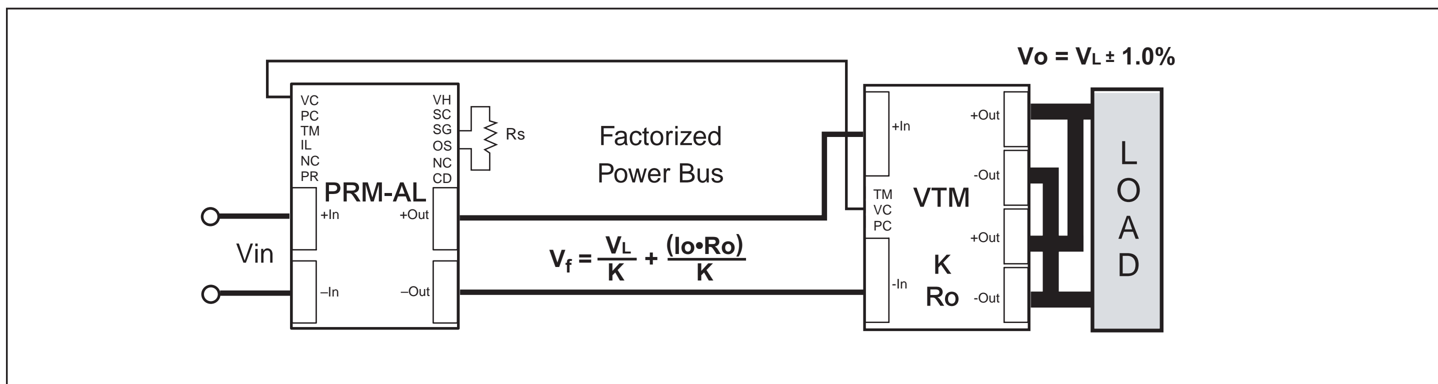


Figure 21 — The PRM controls the factorized bus voltage, Vf, in proportion to output current to compensate for the output resistance, Ro, of the VTM. The VTM output voltage is typically within 1% of the desired load voltage (VL) over all line and load conditions.

FPA Non-isolated Remote Loop

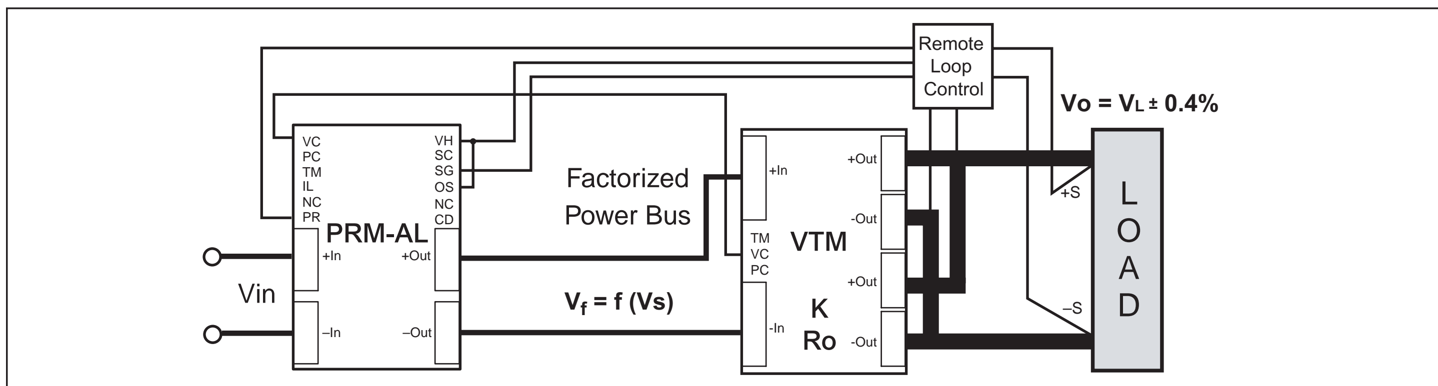


Figure 22 — An external error amplifier or Point-of-Load IC (POLIC) senses the load voltage and controls the PRM output – the factorized bus – as a function of output current, compensating for the output resistance of the VTM and for distribution resistance.

FPA Isolated Remote Loop

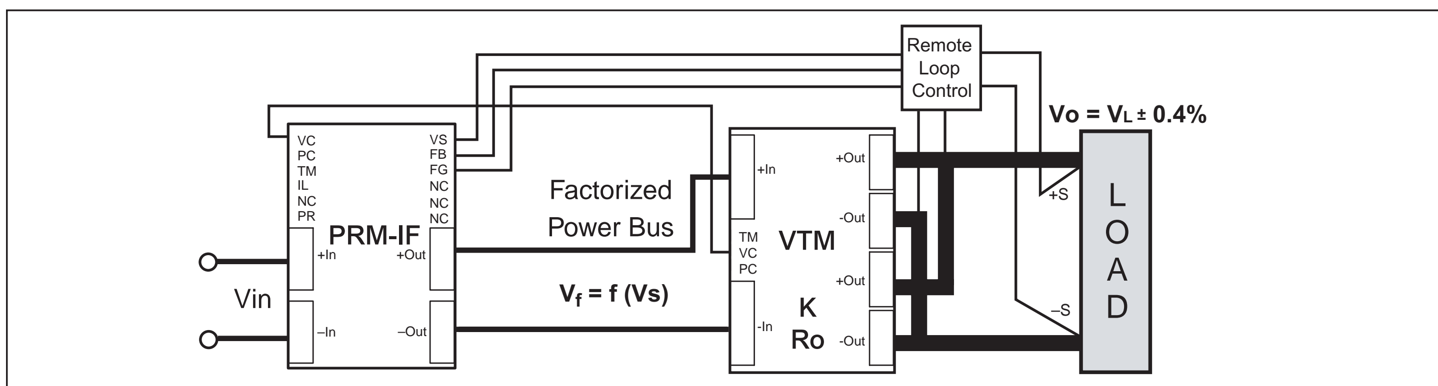


Figure 23—An external error amplifier or Point-of-Load IC (POLIC) senses the load voltage and controls the PRM output – the factorized bus – as a function of output current, compensating for the output resistance of the VTM and for distribution resistance. The factorized bus voltage (Vf) increases in proportion to load current. The remote feed back loop is isolated within the PRM to support galvanic isolation and hipot compliance at the system level.

V•I Chip Soldering Recommendations

V•I Chip modules are intended for reflow soldering processes. The following information defines the processing conditions required for successful attachment of a V•I Chip to a PCB. Failure to follow the recommendations provided can result in aesthetic or functional failure of the module.

Storage

V•I Chip modules are currently rated at MSL 5. Exposure to ambient conditions for more than 72 hours requires a 24 hour bake at 125ºC to remove moisture from the package.

Solder Paste Stencil Design

Solder paste is recommended for a number of reasons, including overcoming minor solder sphere co-planarity issues as well as simpler integration into overall SMD process.

63/37 SnPb, either no-clean or water-washable, solder paste should be used. Pb-free development is underway.

The recommended stencil thickness is 6 mils. The apertures should be 20 mils in diameter for the In-Board (BGA) application and 0.9-0.9:1 for the On-Board (J-Leaded).

Pick & Place

In-Board (BGA) modules should be placed as accurately as possible to minimize any skewing of the solder joint; a maximum offset of 10 mils is allowable. On-Board (J-Leaded) modules should be placed within ±5 mils.

To maintain placement position, the modules should not be subjected to acceleration greater than 500 in/sec^2 prior to reflow.

Reflow

There are two temperatures critical to the reflow process; the solder joint temperature and the module's case temperature. The solder joint's temperature should reach at least 220ºC, with a time above liquidus (183ºC) of ~30 seconds.

The module's case temperature must not exceed 208 ºC at anytime during reflow.

Because of the ΔT needed between the pin and the case, a forced-air convection oven is preferred for reflow soldering. This reflow method generally transfers heat from the PCB to the solder joint. The module's large mass also reduces its temperature rise. Care should be taken to prevent smaller devices from excessive temperatures. Reflow of modules onto a PCB using Air-Vac-type equipment is not recommended due to the high temperature the module will experience.

Inspection

For the BGA-version, a visual examination of the post-reflow solder joints should show relatively columnar solder joints with no bridges. An inspection using x-ray equipment can be done, but the module's materials may make imaging difficult.

The J-Lead version's solder joints should conform to IPC 12.2
- Properly Wetted Fillet must be evident
- Heel fillet height must exceed lead thickness plus solder thickness.

Removal and Rework

V•I Chip modules can be removed from PCBs using special tools such as those made by Air-Vac. These tools heat a very localized region of the board with a hot gas while applying a tensile force to the component (using vacuum). Prior to component heating and removal, the entire board should be heated to 80-100ºC to decrease the component heating time as well as local PCB warping. If there are adjacent moisture-sensitive components, a 125ºC bake should be used prior to component removal to prevent popcorning. V•I Chip modules should not be expected to survive a removal operation.

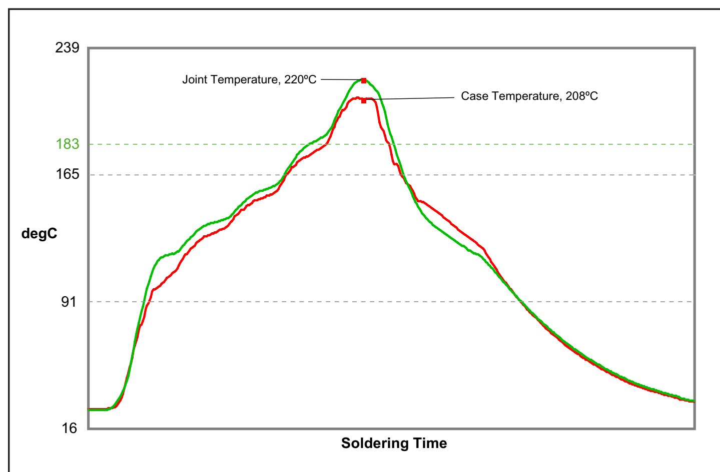


Figure 25—Thermal profile diagram

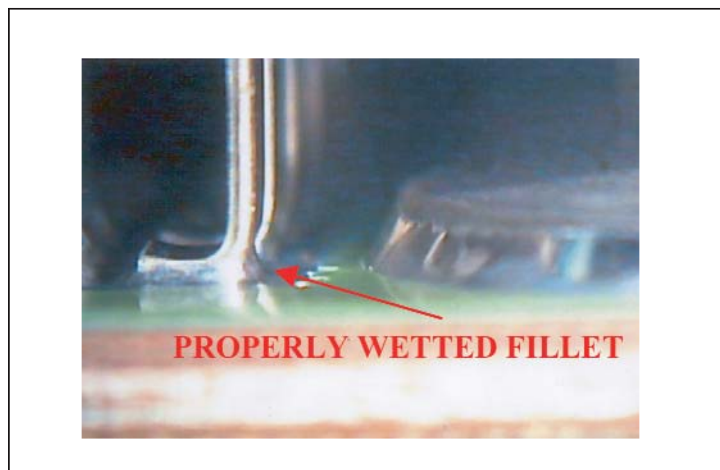


Figure 26— Properly reflowed V•I Chip J-Lead.

Input Impedance Recommendations

To take full advantage of the VTM's capabilities, the impedance of the source (input source plus the PC board impedance) must be low over a range from DC to 5 MHz. The input of the VTM (factorized bus) should be locally bypassed with a 8 µF low Q aluminum electrolytic capacitor. Additional input capacitance may be added to improve transient performance or compensate for high source impedance. The VTM has extremely wide bandwidth so the source response to transients is usually the limiting factor in overall output response of the VTM.

Anomalies in the response of the source will appear at the output of the VTM, multiplied by its K factor of 1/24. The DC resistance of the source should be kept as low as possible to minimize voltage deviations on the input to the VTM. If the VTM is going to be operating close to the high limit of its input range, make sure input voltage deviations will not trigger the over voltage shutdown.

Input Fuse Recommendations

V•I Chips are not internally fused in order to provide flexibility in power system configuration. However, input line fusing of V•I Chips must always be incorporated within the power system. A fast acting fuse, such as NANO2 FUSE 451 Series 7 A 125 V, is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +IN port.

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- The electrical and thermal utility of the V•I Chip package
- The design of the V•I Chip package
- The Power Conversion Topology utilized in the V•I Chip package
- The Control Architecture utilized in the V•I Chip package
- The Factorized Power Architecture.

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