□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V236H3
SUFFIX: LH3

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Aug. 17, 2010	All	All	The approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V236H3-LH3 is a 23.6" TFT Liquid Crystal Display module with WLED Backlight unit, a 15-pin power interface and a 51-pin 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display up to 16.7M colors. The converter module for Backlight unit is not built in.

1.2 FEATURES

- Extra-wide viewing angle.
- High contrast ratio.
- Fast response time.
- High color saturation.
- Full HD (1920 x 1080 pixels) resolution.
- DE (Data Enable) only mode.
- LVDS (Low Voltage Differential Signaling) interface.
- RoHS compliance.
- support 120Hz frame rate

1.3 APPLICATION

- Standard Living Room TVs
- MFM Application
- 3D Application

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	521.28(H) x 293.22(V) (23.547" diagonal)	mm	(1)
Bezel Opening Area	525.22 (H) x 297.22 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.0905(H) x 0.2715(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Power consumption	19.93W (LVDS input Power 6.1W + LED Backlight Power 13.83 W)	Watt	(2)
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally white	-	-
Surface Treatment	Anti-Glare coating (Haze 25%)	-	(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) Please refer sec 3.1 and 3.2 for more information of Power consumption

Note (3) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	544.3	544.8	545.3	mm	(1)
	Vertical (V)	320.0	320.5	321.0	mm	(1)
	Depth (D)	12.61	13.11	13.61	mm	(1)
Weight		-	2450	2500	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

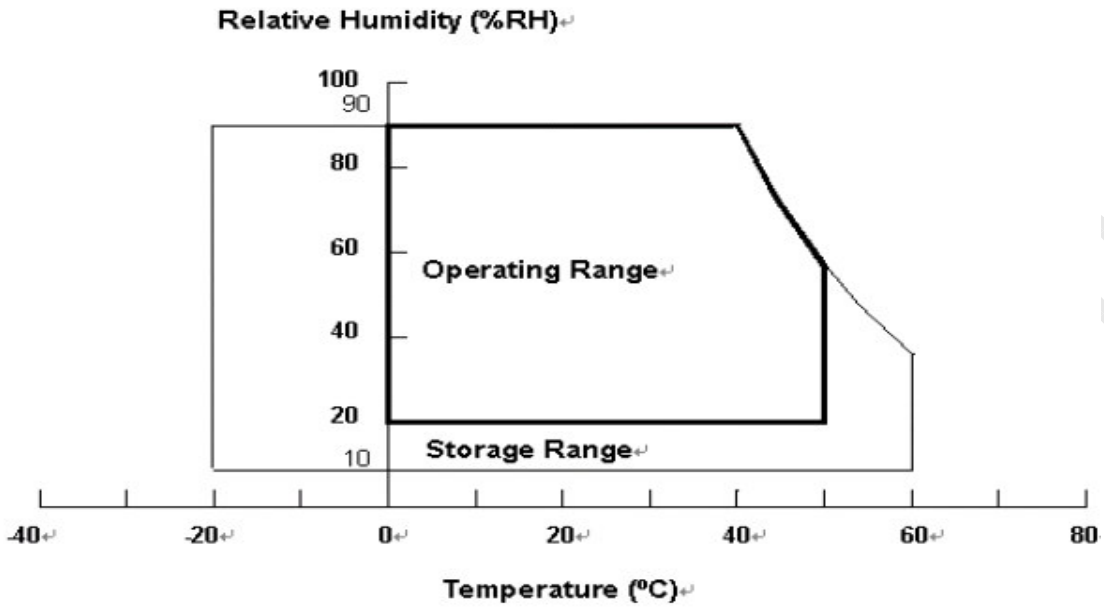
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 300 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	6	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

3. ELECTRICAL CHARACTERISTICS

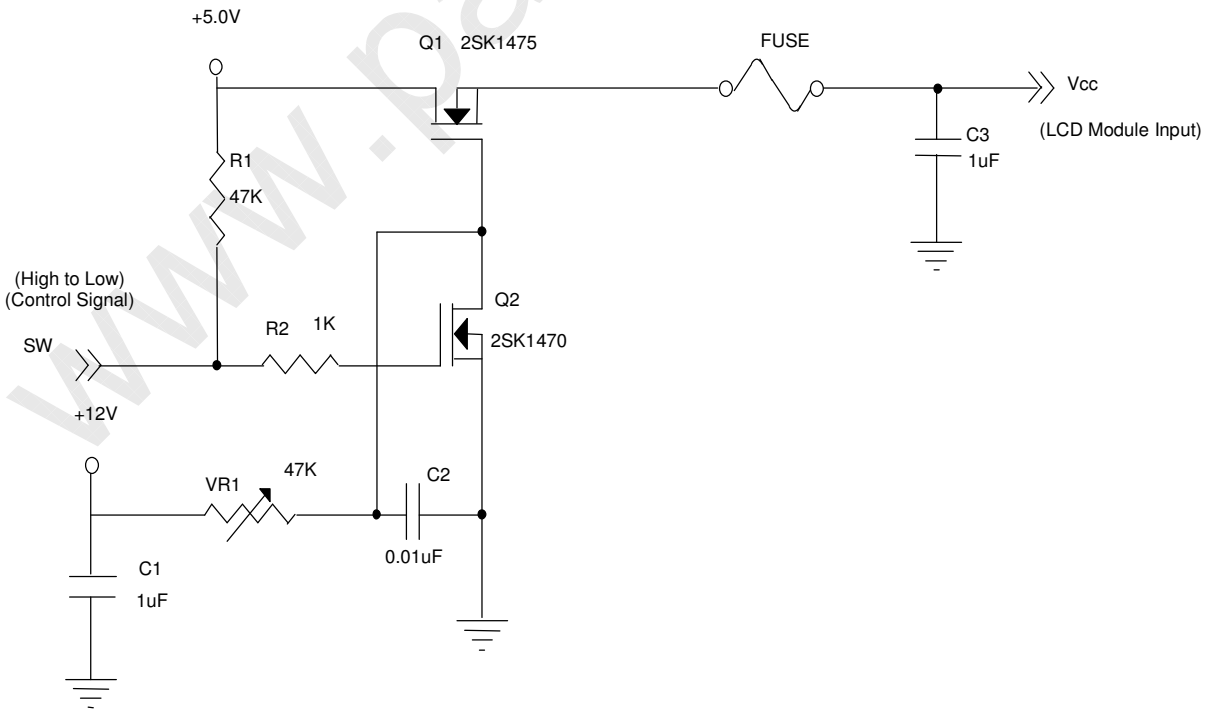
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

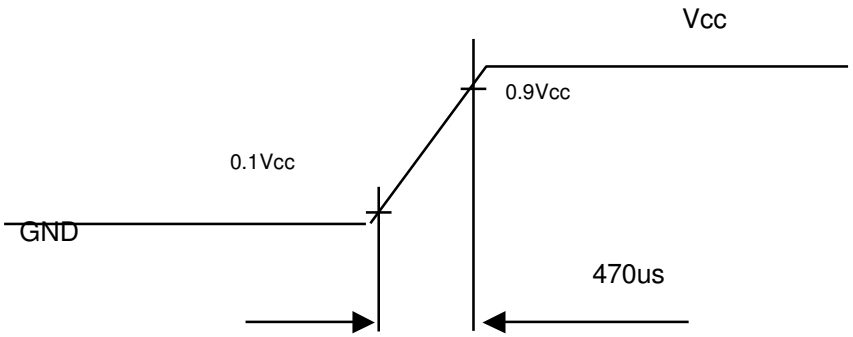
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5.0	5.5	V	(1)
Rush Current		I_{RUSH}	–	–	5	A	(2)
Power consumption		P_T	–	6.1	8.5		(3)
Power Supply Current	White Pattern	–	–	0.8	1.11	A	(4)
	Vertical Strip(MNT)	–	–	0.98	1.36	A	
	Black Pattern	–	–	1.22	1.70	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	–	–	mV	(5)
	Differential Input Low Threshold Voltage	V_{LVTL}	–	–	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	–	600	mV	

Note (1) The module should be always operated within the above ranges.

Note (2) Even though Inrush current is over the specified value, there is no problem if I2T of fuse Spec is satisfied. The measurement condition is shown as bellowing.



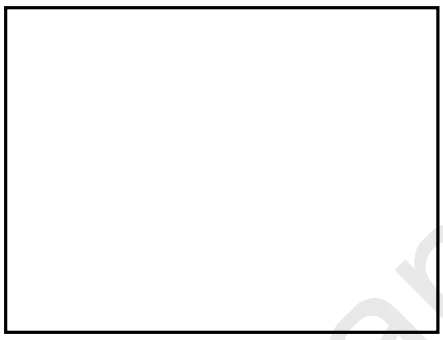
Vcc rising time is 470us



Note (3) The Specified Power consumption is under Vertical Stripe pattern.

Note (4) The specified power supply current is under the conditions at Vcc=5.0V, Ta = 25 ± 2 ºC, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

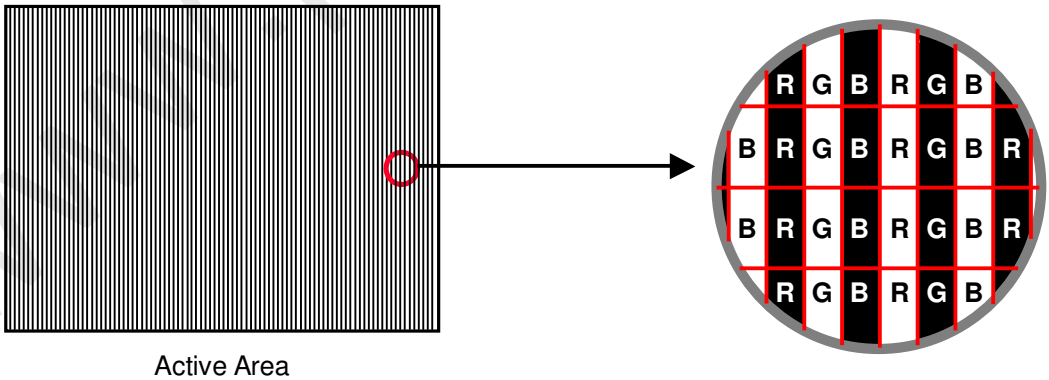


Active Area

b. Black Pattern

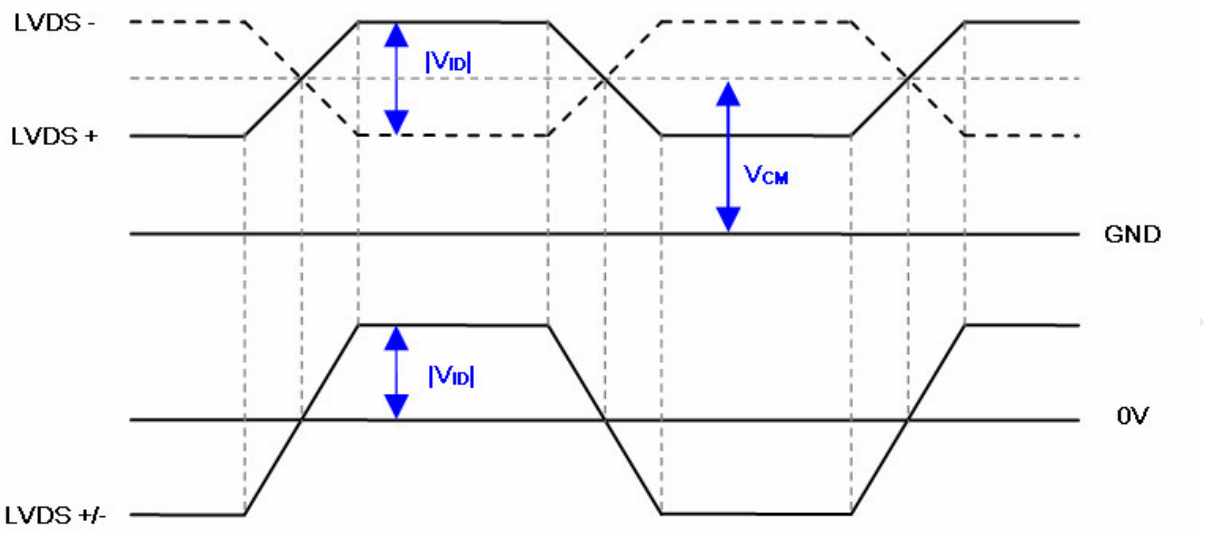
Active Area

c. Vertical Stripe Pattern



Active Area

Note (5) The LVDS input characteristics are as follows :



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LED LIGHT BAR CHARACTERISTICS

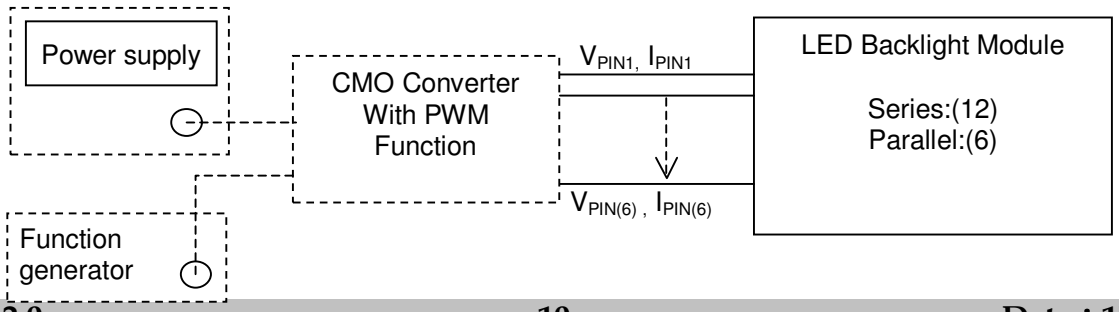
(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Light Bar Voltage	V_W	34	38.4	42	V	(1), Duty=100%, I_L =60mA
Forward Voltage	V_f	-	3.2	3.5	V	I_L =60mA
LED Current	I_L	---	60	75	mA	(1), (2) Duty=100%
Power consumption	P_{BL}	---	13.83	18.9	W	(1) Duty=100%, I_L =60mA
Life time	-	30,000	-	-	Hrs	(3)

Note (1)LED light bar input voltage and current are measured by utilizing a true RMS multimeter as shown below:

Note (2) $P_{BL} = I_{PIN} \times V_{PIN} \times$ (6) input pins , LED light bar circuit is (12)Series, (6)Parallel.

Note (3)The lifetime of LED is defined as the time when LED packages continue to operate under the conditions at Ta = 25 ±2 ℃ and I= (20)mA (per chip) until the brightness becomes ≦ 50% of its original value.



3.2.2 LIGHTBAR Connector Pin Assignment

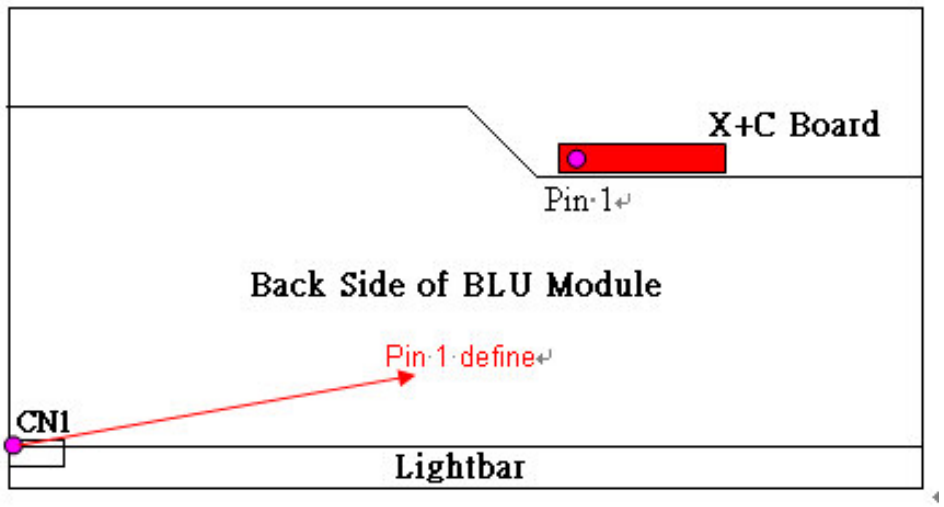
Connector: B-F,7083K-F12N-00L ,ENTERY(恩得利),

161035-12041-3 P-TWO (禾昌), GB5DH120-112M-7H,Foxconn(鴻海), or Compatible

(1) Input connector pin assignment: CN1

Pin No.	Symbol	Feature
1	NC	Not connection, this pin should be open
2	LED1	Cathode of LED string
3	LED2	Cathode of LED string
4	LED3	Cathode of LED string
5	NC	Not connection, this pin should be open
6	VLED (38.4V)	VLED
7	VLED (38.4V)	VLED
8	NC	Not connection, this pin should be open
9	LED4	Cathode of LED string
10	LED5	Cathode of LED string
11	LED6	Cathode of LED string
12	NC	Not connection, this pin should be open

3.3 LVDS INPUT SIGNAL SPECIFICATIONS

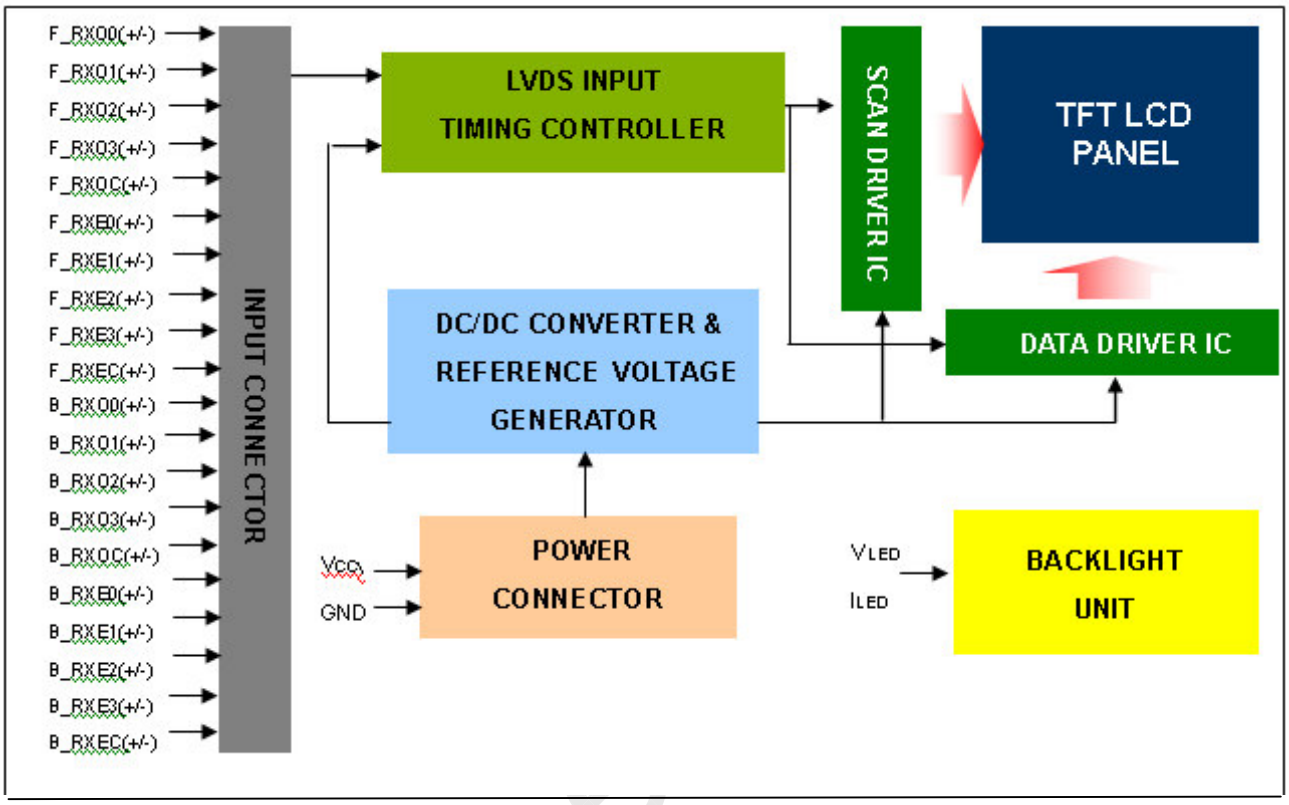


3.3.1 LVDS DATA MAPPING TABLE

LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

Pin	Name	Description
1	B_RXO0-	B_ Negative LVDS differential data input. Channel O0 (odd)
2	B_RXO0+	B_ Positive LVDS differential data input. Channel O0 (odd)
3	B_RXO1-	B_ Negative LVDS differential data input. Channel O1 (odd)
4	B_RXO1+	B_ Positive LVDS differential data input. Channel O1 (odd)
5	B_RXO2-	B_ Negative LVDS differential data input. Channel O2 (odd)
6	B_RXO2+	B_ Positive LVDS differential data input. Channel O2 (odd)
7	GND	Ground
8	B_RXOC-	B_ Negative LVDS differential clock input. (odd)
9	B_RXOC+	B_ Positive LVDS differential clock input. (odd)
10	GND	Ground
11	B_RXO3-	B_ Negative LVDS differential data input. Channel O3(odd)
12	B_RXO3+	B_ Positive LVDS differential data input. Channel O3 (odd)
13	GND	Ground
14	B_RXE0-	B_ Negative LVDS differential data input. Channel E0 (even)
15	B_RXE0+	B_ Positive LVDS differential data input. Channel E0 (even)
16	B_RXE1-	B_ Negative LVDS differential data input. Channel E1 (even)
17	B_RXE1+	B_ Positive LVDS differential data input. Channel E1 (even)
18	B_RXE2-	B_ Negative LVDS differential data input. Channel E2 (even)
19	B_RXE2+	B_ Positive LVDS differential data input. Channel E2 (even)
20	GND	Ground
21	B_RXEC-	B_ Negative LVDS differential clock input. (even)
22	B_RXEC+	B_ Positive LVDS differential clock input. (even)
23	GND	Ground
24	B_RXE3-	B_ Negative LVDS differential data input. Channel E3 (even)
25	B_RXE3+	B_ Positive LVDS differential data input. Channel E3 (even)
26	GND	Ground
27	F_RXO0-	F_ Negative LVDS differential data input. Channel O0 (odd)
28	F_RXO0+	F_ Positive LVDS differential data input. Channel O0 (odd)
29	F_RXO1-	F_ Negative LVDS differential data input. Channel O1 (odd)
30	F_RXO1+	F_ Positive LVDS differential data input. Channel O1 (odd)
31	F_RXO2-	F_ Negative LVDS differential data input. Channel O2 (odd)
32	F_RXO2+	F_ Positive LVDS differential data input. Channel O2 (odd)
33	GND	Ground
34	F_RXOC-	F_ Negative LVDS differential clock input. (odd)
35	F_RXOC+	F_ Positive LVDS differential clock input. (odd)
36	GND	Ground
37	F_RXO3-	F_ Negative LVDS differential data input. Channel O3(odd)
38	F_RXO3+	F_ Positive LVDS differential data input. Channel O3 (odd)
39	GND	Ground
40	F_RXE0-	F_ Negative LVDS differential data input. Channel E0 (even)
41	F_RXE0+	F_ Positive LVDS differential data input. Channel E0 (even)
42	F_RXE1-	F_ Negative LVDS differential data input. Channel E1 (even)
43	F_RXE1+	F_ Positive LVDS differential data input. Channel E1 (even)
44	F_RXE2-	F_ Negative LVDS differential data input. Channel E2 (even)
45	F_RXE2+	F_ Positive LVDS differential data input. Channel E2 (even)
46	GND	Ground
47	F_RXEC-	F_ Negative LVDS differential clock input. (even)
48	F_RXEC+	F_ Positive LVDS differential clock input. (even)
49	GND	Ground
50	F_RXE3-	F_ Negative LVDS differential data input. Channel E3 (even)
51	F_RXE3+	F_ Positive LVDS differential data input. Channel E3 (even)

Note (1) MSAKS24020P51A (STM) or FI-R51S-HF (JAE) or equivalent

Note (2) The first pixel is odd.

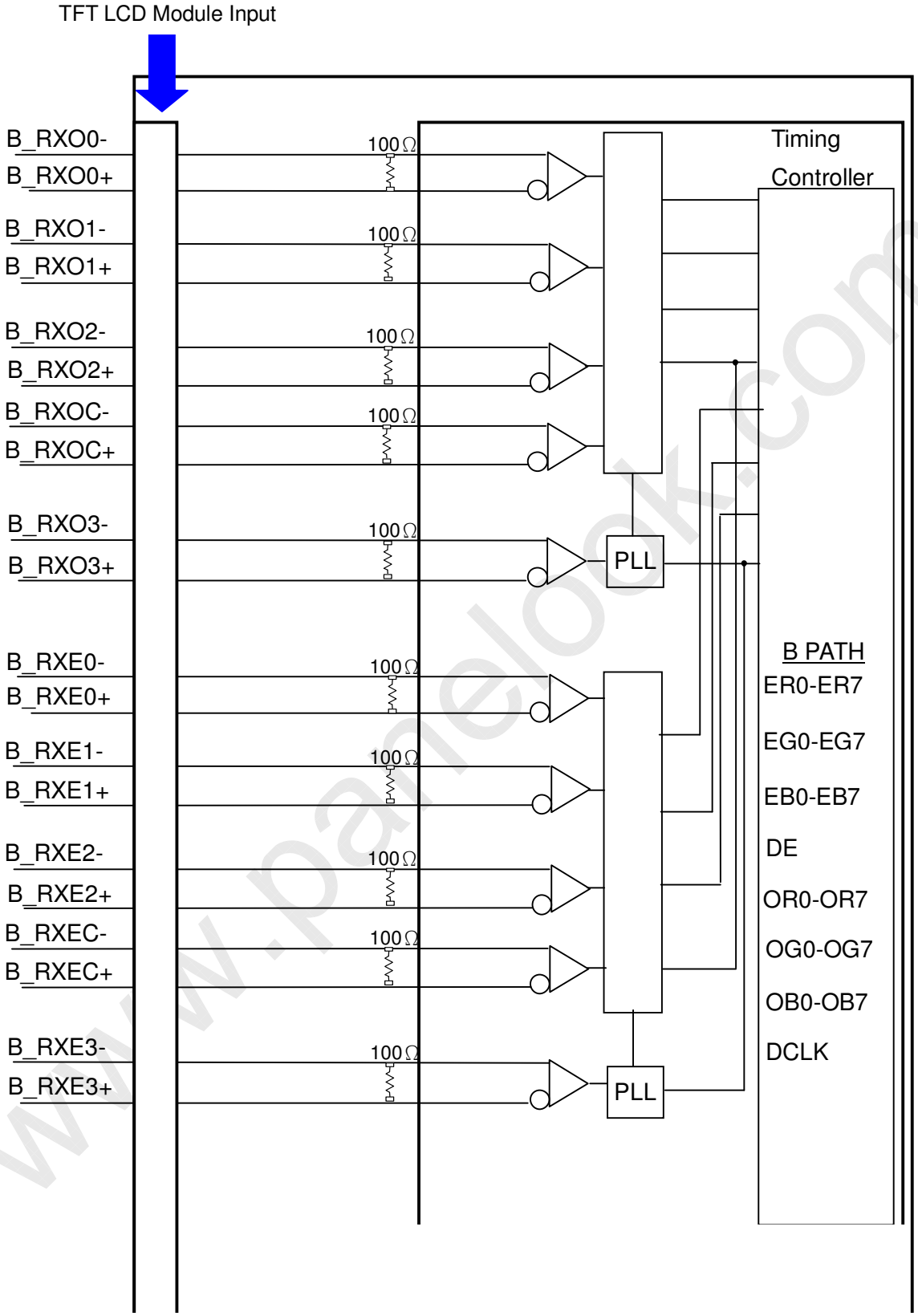
Note (3) Input signal of even and odd clock should be the same timing.

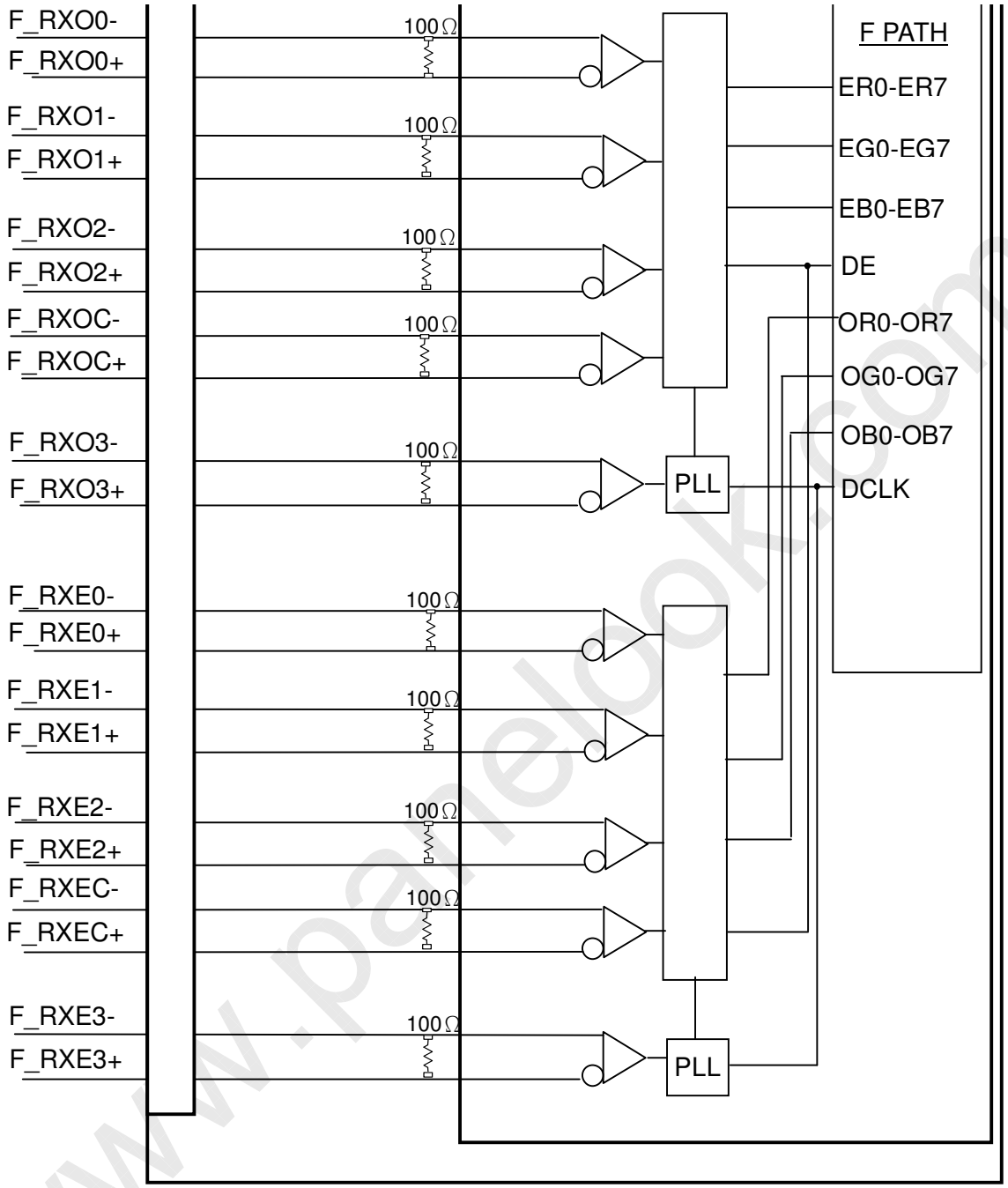
5.2 TFT LCD Module Power Input

Pin	Name	Description
1	NC	Not connection, this pin should be open.
2	NC	Not connection, this pin should be open.
3	NC	Not connection, this pin should be open.
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	NC	Not connection, this pin should be open.
9	NC	Not connection, this pin should be open.
10	GND	Ground
11	Vcc	+5.0V power supply
12	Vcc	+5.0V power supply
13	Vcc	+5.0V power supply
14	Vcc	+5.0V power supply
15	Vcc	+5.0V power supply

Note (1) Connector Part No.: Yeonho 12507WR-H15L or Compatible

5.3 BLOCK DIAGRAM OF INTERFACE





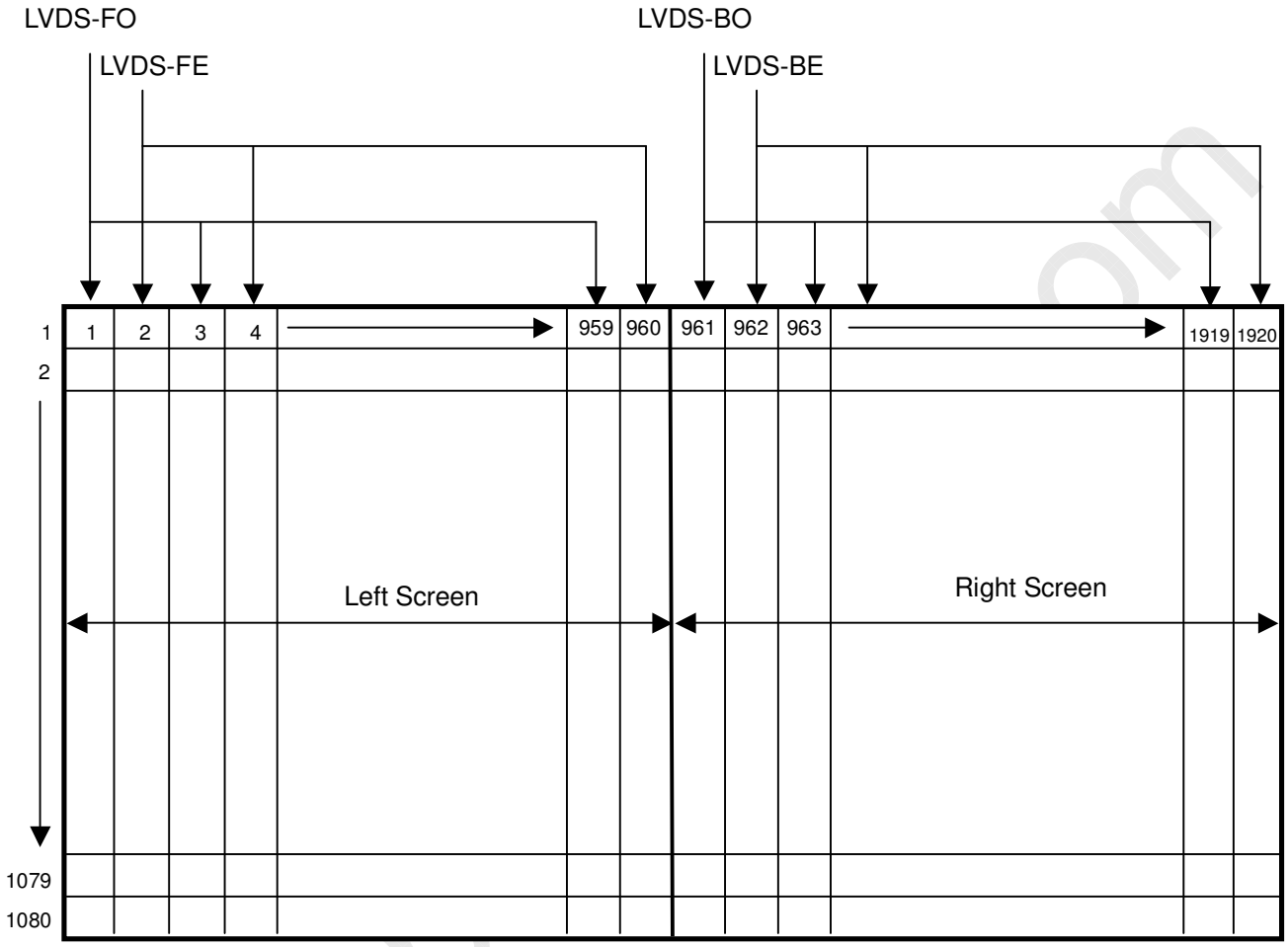
ER0~ER7	Even pixel R data	OR0~OR7	Odd pixel R data
EG0~EG7	Even pixel G data	OG0~OG7	Odd pixel G data
EB0~EB7	Even pixel B data	OB0~OB7	Odd pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

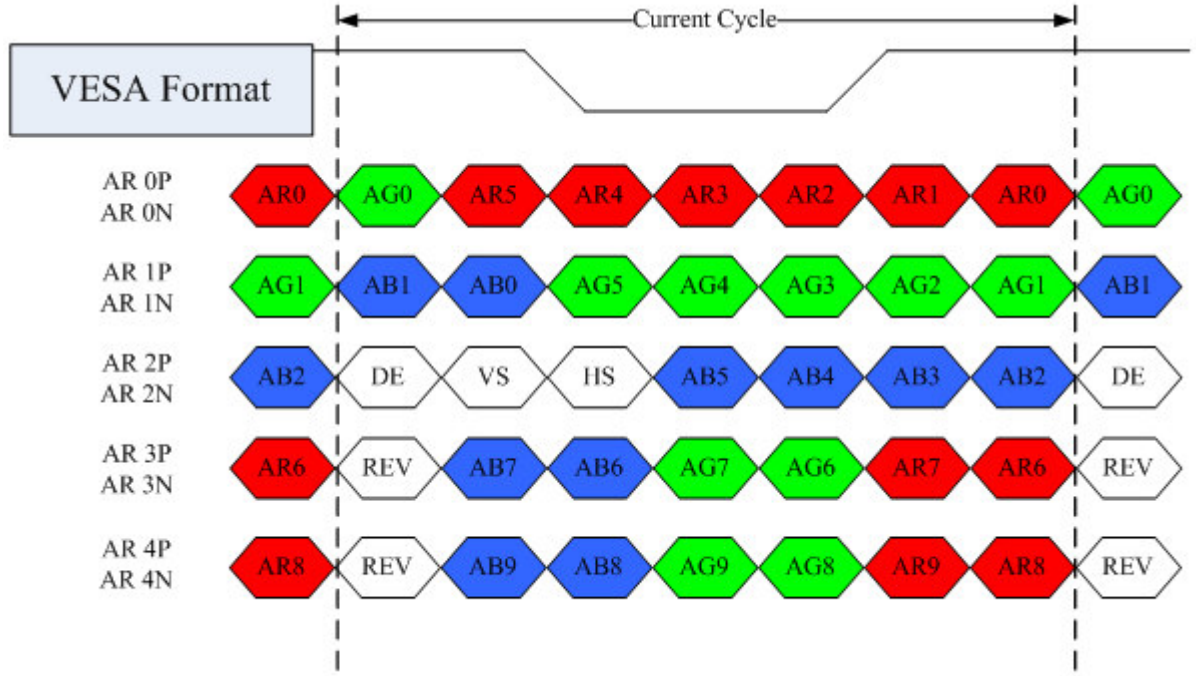
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

Screen Format



5.4 LVDS INTERFACE

VESA Format



AR0~AR9 : First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9 : First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9 : First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

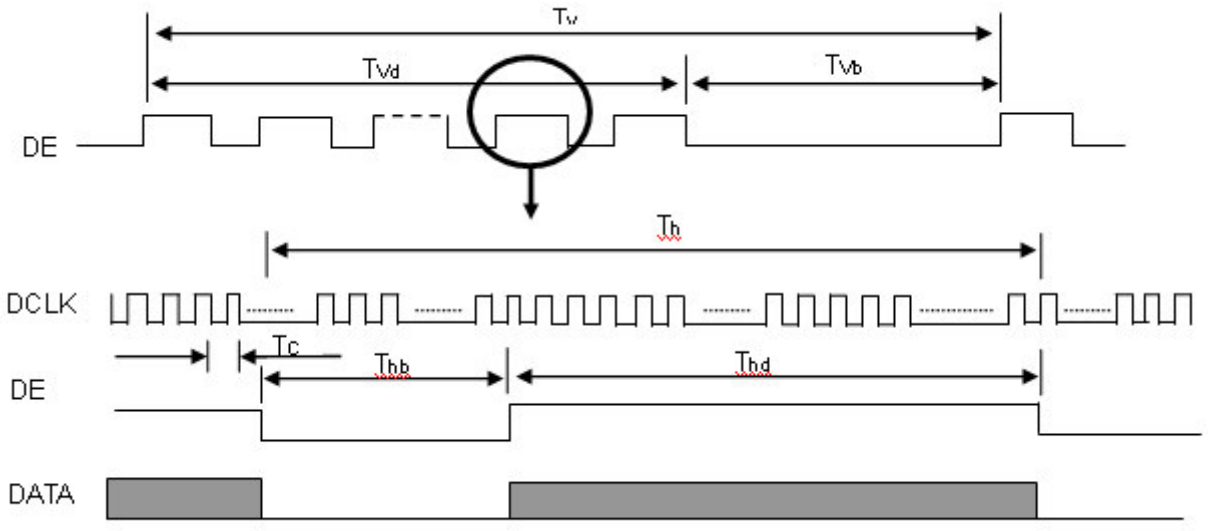
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. (Ta = 25 ± 2 ºC)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	31.9	74.25	80.9	MHz	
	Period	Tc	12.4	16.7	31.3-	ns	
	Input cycle to cycle jitter	T_{rcl}	-0.02*Tc	—	0.02*Tc	ns	(2)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(3)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	—	—	ps	
	Hold Time	Tlvhd	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_r	58	120	122	Hz	
	Total	Tv	1100	1125	1180	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	
	Blank	Tvb	Tv-Tvd	45	Tv+Tvd	Th	
Horizontal Active Display Term	Total	Th	500	550	562	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	
	Blank	Thb	Th-Thd	70	Th+Thd	Tc	

Note: Because this module is operated by DE only mode, Hsync and Vsync input signals are ignored.

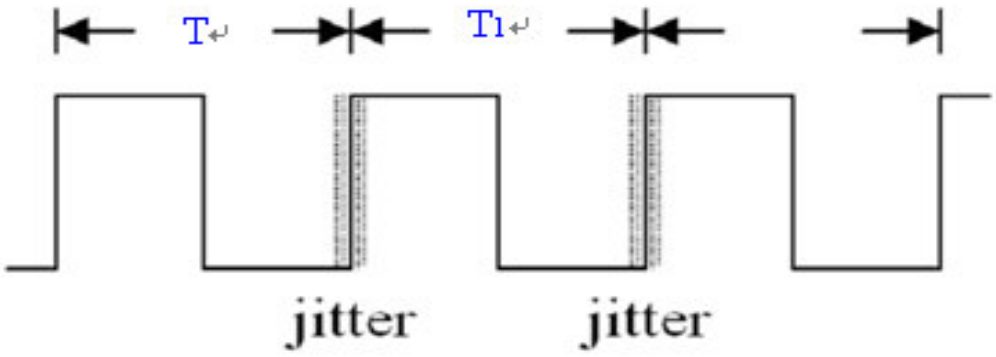
INPUT SIGNAL TIMING DIAGRAM



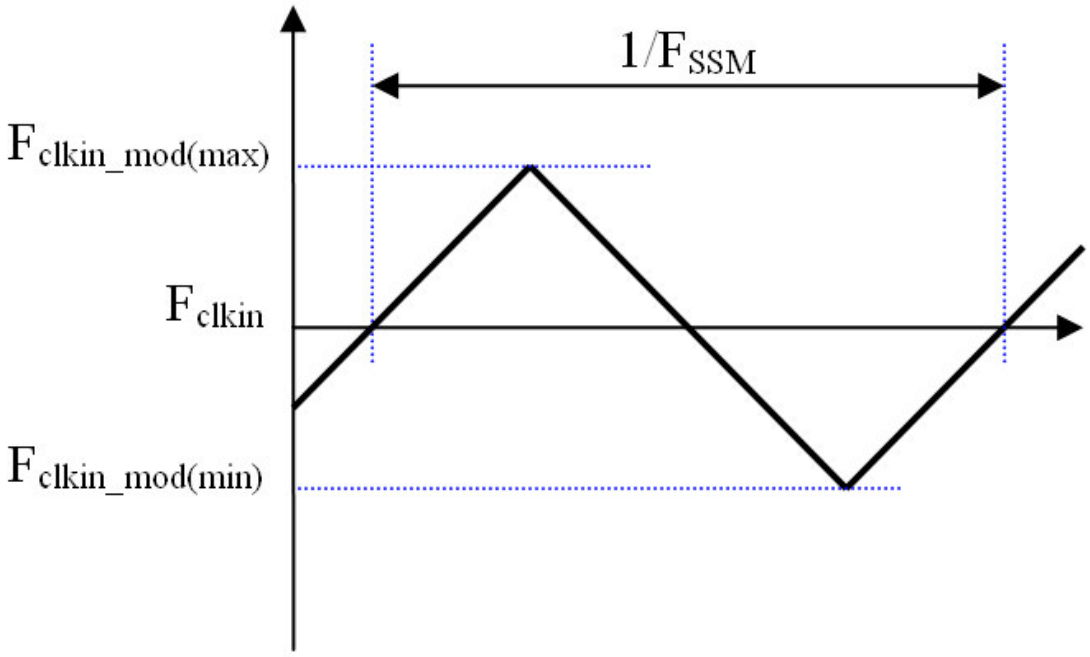
Note (1) Please make sure the range of frame rate has follow the below equation：

Fr(max) ≧ Fclkin ／ Tv×Th ≦ Fr(min)

Note (2) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

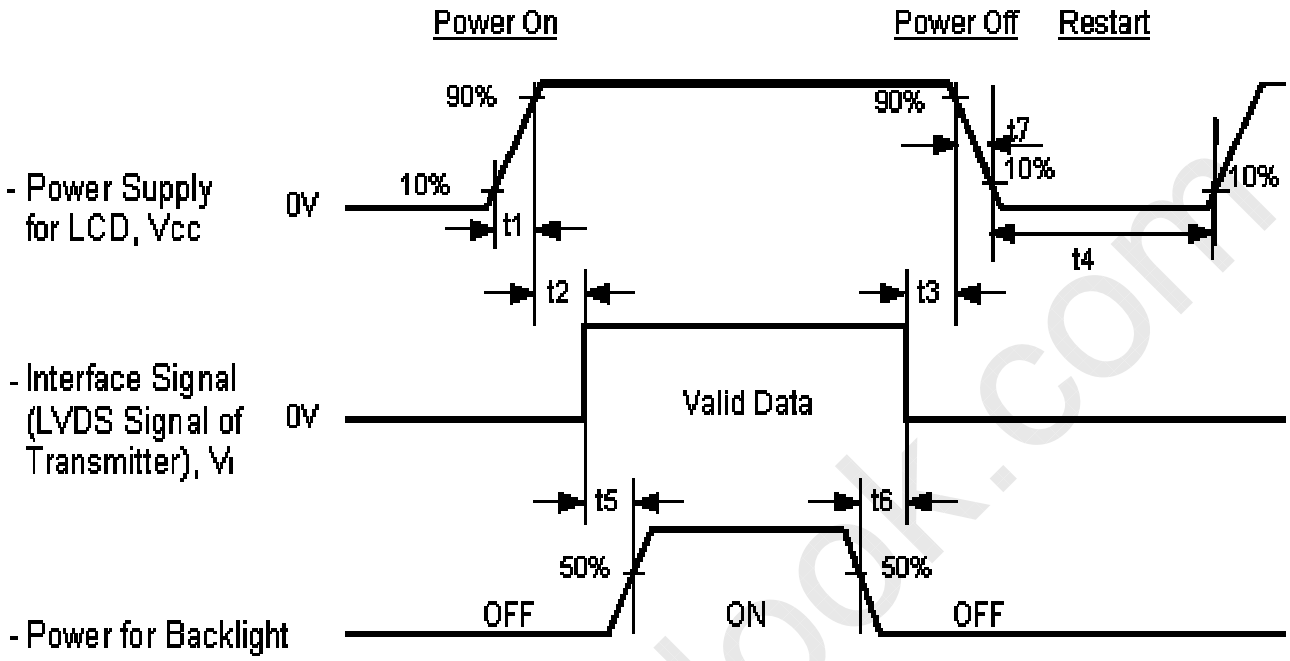


Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Timing Specifications:

0.5	<	t1	≦	10	msec
0	<	t2	≦	50	msec
0	<	t3	≦	50	msec
		t4	≧	500	msec
		t5	≧	450	msec
		t6	≧	90	msec
5	≦	t7	≦	100	msec

Note.

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.

(3) In case of Vcc = off level, please keep the level of input signals on the low or keep a high impedance.

(4) t4 should be measured after the module has been fully discharged between power of and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

(6) CMO won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.

(7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "t7 spec".

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	5	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	60 ± 1.2	mA

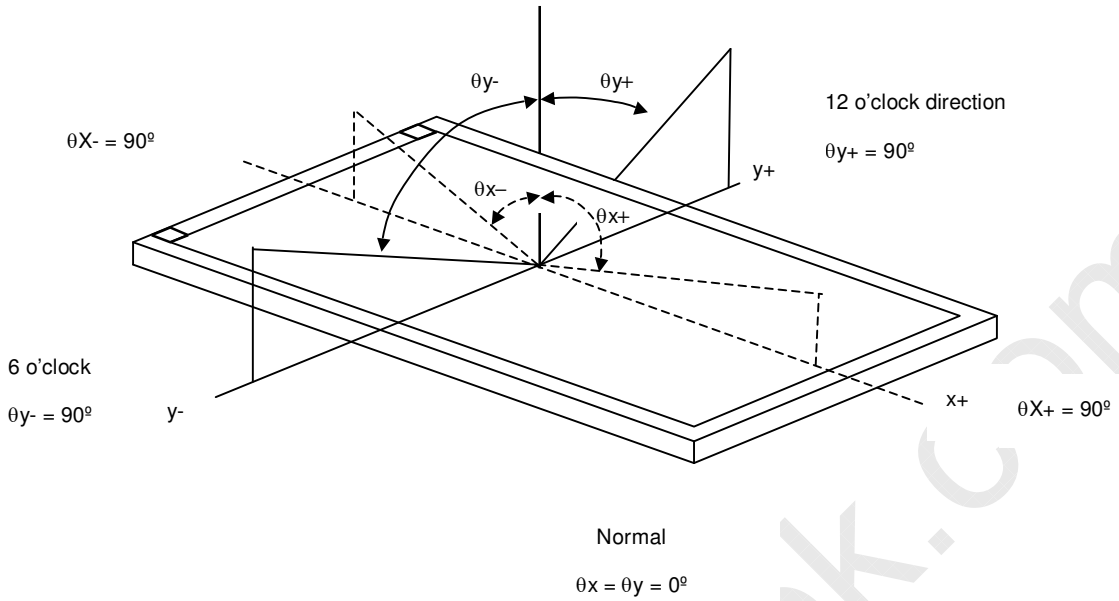
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	700	1000	-	-	Note (2)
Response Time		T_R		-	1.5	2.5	ms	Note (3)
		T_F		-	3.5	5.5		
Center Luminance of White		LC		250	300	-	cd/m^2	Note (5)
White Variation		δW		-	-	1.42	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (6)
Color Chromaticity	Red	Rx		Typ. -0.03	0.641	Typ. +0.03	-	(1)(4)
		Ry			0.338		-	
	Green	Gx			0.315		-	
		Gy			0.629		-	
	Blue	Bx			0.159		-	
		By			0.059		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
	Color Gamut	C.G		-	70	-	%	NTSC
Viewing Angle	Horizontal	$\theta_{x+} + \theta_{x-}$	CR ≧ 10 USB2000	150	170	-	Deg.	(1)(4)
	Vertical	$\theta_{Y+} + \theta_{Y-}$		140	160	-		
	Horizontal	$\theta_{x+} + \theta_{x-}$	CR ≧ 5 USB2000	160	178	-		
	Vertical	$\theta_{Y+} + \theta_{Y-}$		150	170	-		

Note (1) Definition of Viewing Angle (θx, θy) :



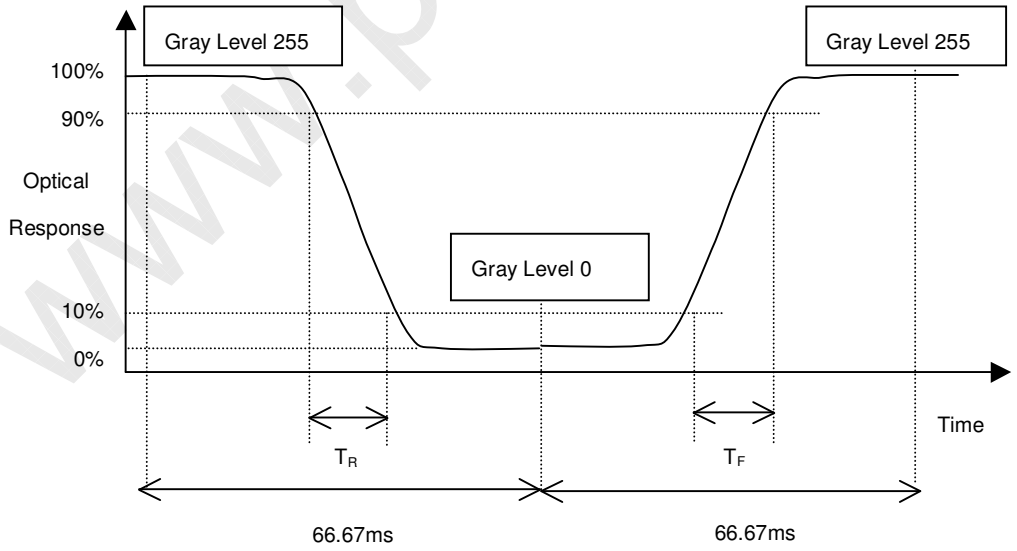
Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

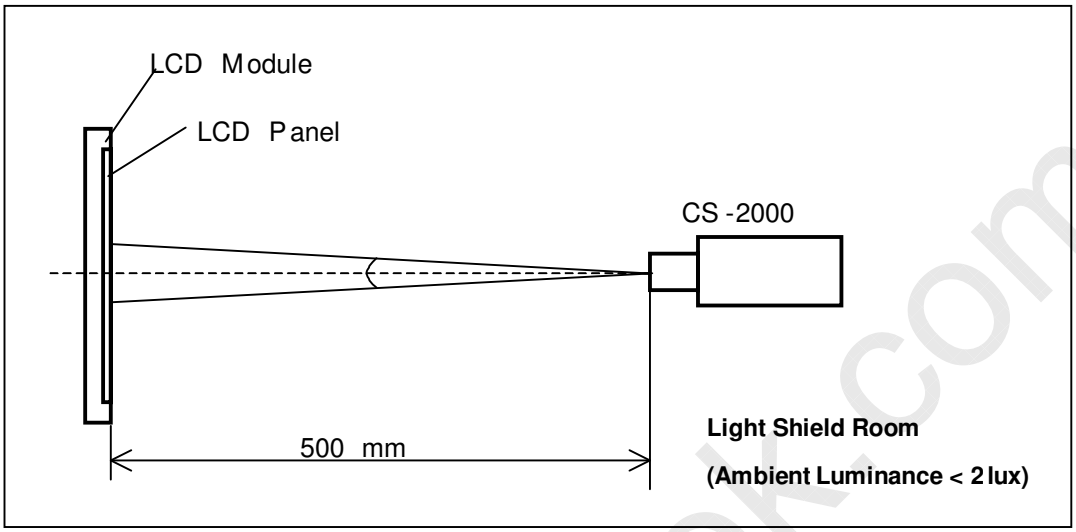
CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note(6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Measurement Setup:

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (5) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

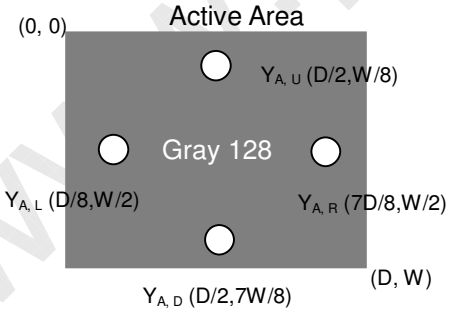
Note (6) Definition of Cross Talk (CT):

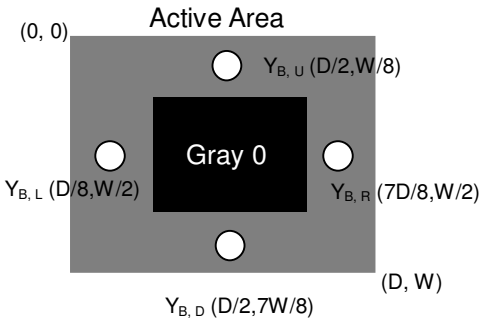
CT = | YB – YA | / YA × 100 (%)

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)





Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMIS LSI chips.

[5] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.

[6] Do not plug in or pull out the I/F connector while the module is in operation.

[7] Do not disassemble the module.

[8] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[9] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[10] When storing modules as spares for a long time, the following precaution is necessary.

[10.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

[10.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[11] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

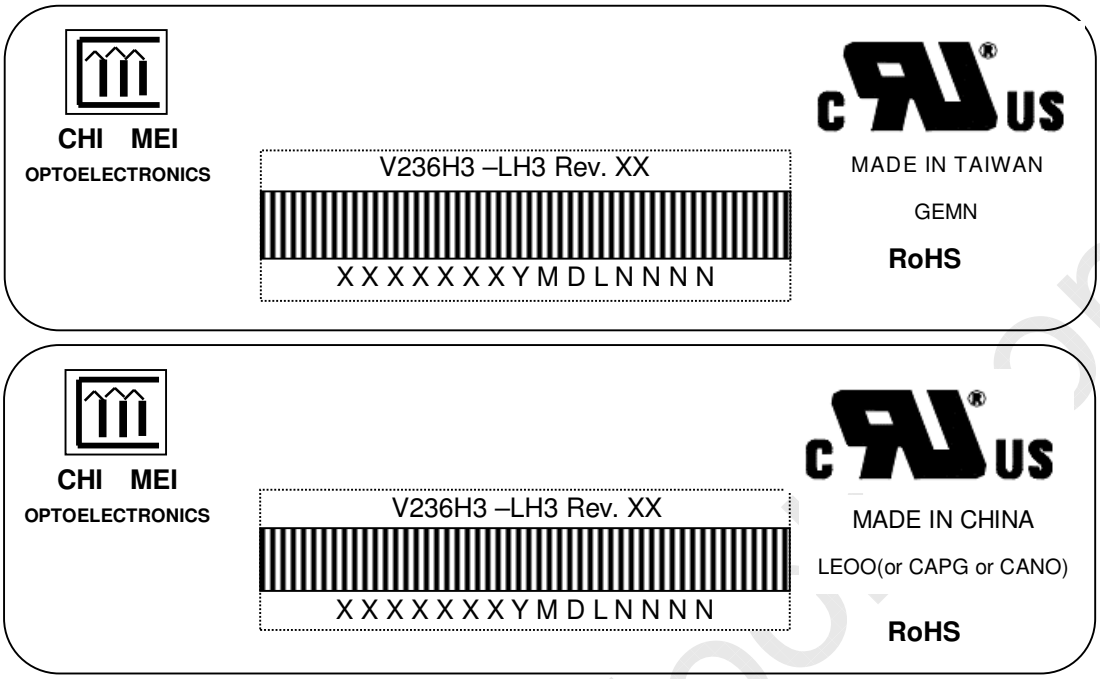
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

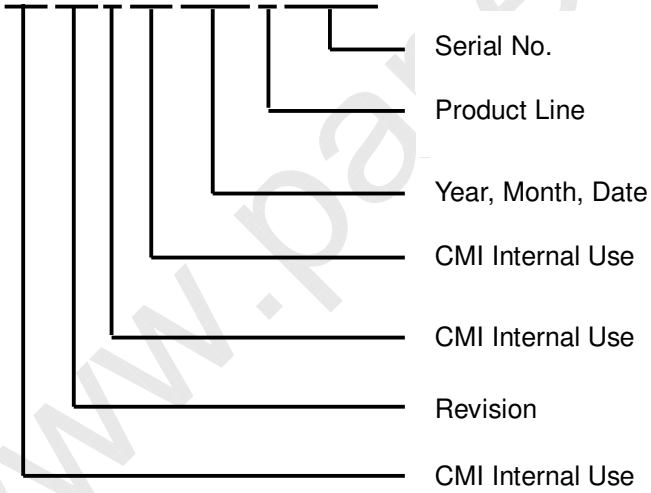
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V236H3 –LH3

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, …etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 11 LCD modules / 1 Box

(2) Box dimensions: 620(L) X 348 (W) X 430 (H) mm

(3) Weight: 30.1Kg (11 modules per box)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

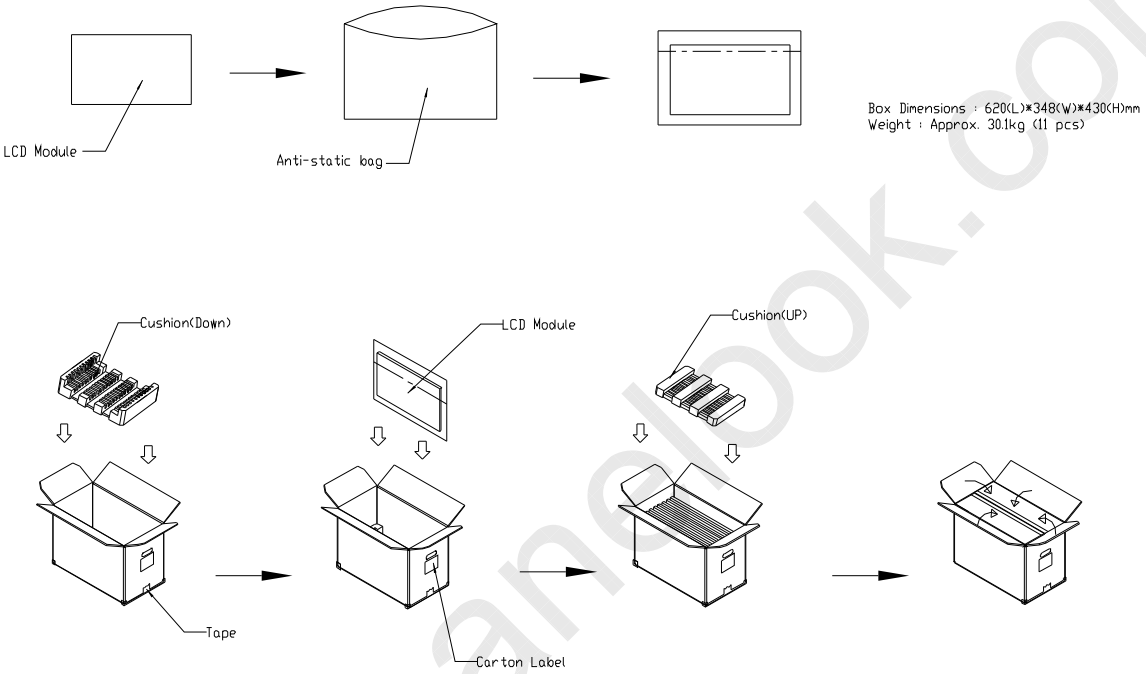
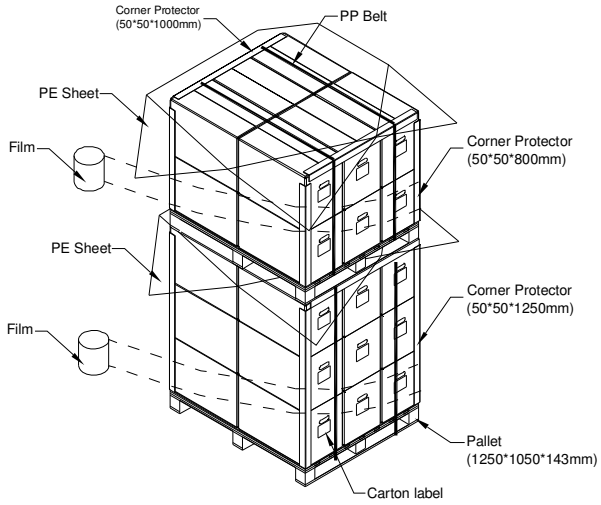


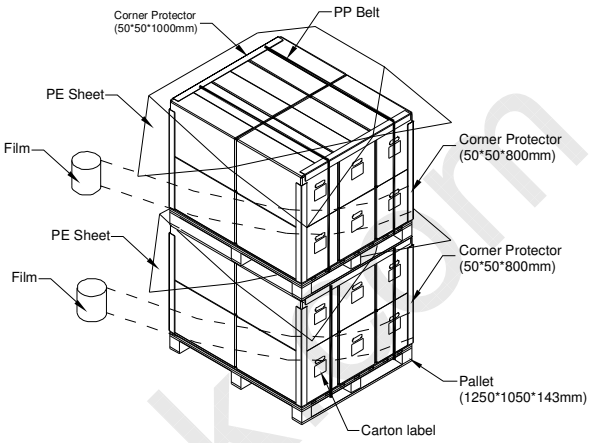
Figure 10-1 packing method

For ocean shipping

Sea / Land Transportation (40ft HQ Container)



Sea / Land Transportation (40ft Container)



For air transport

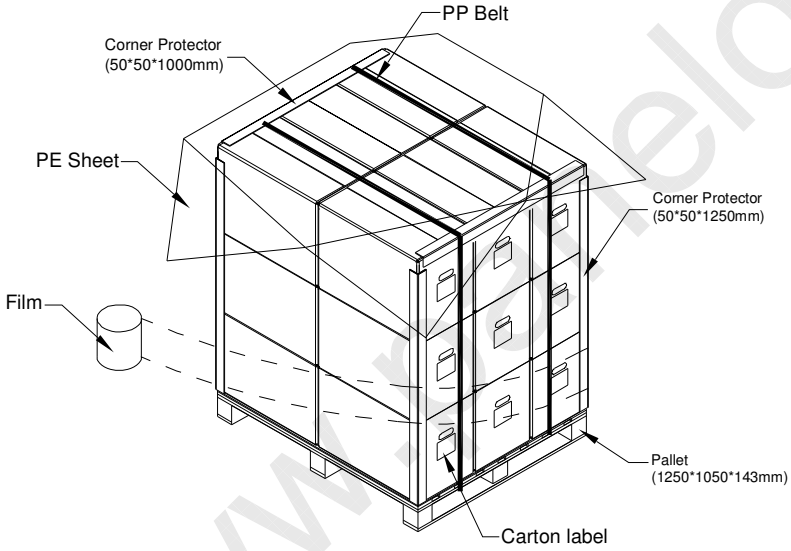
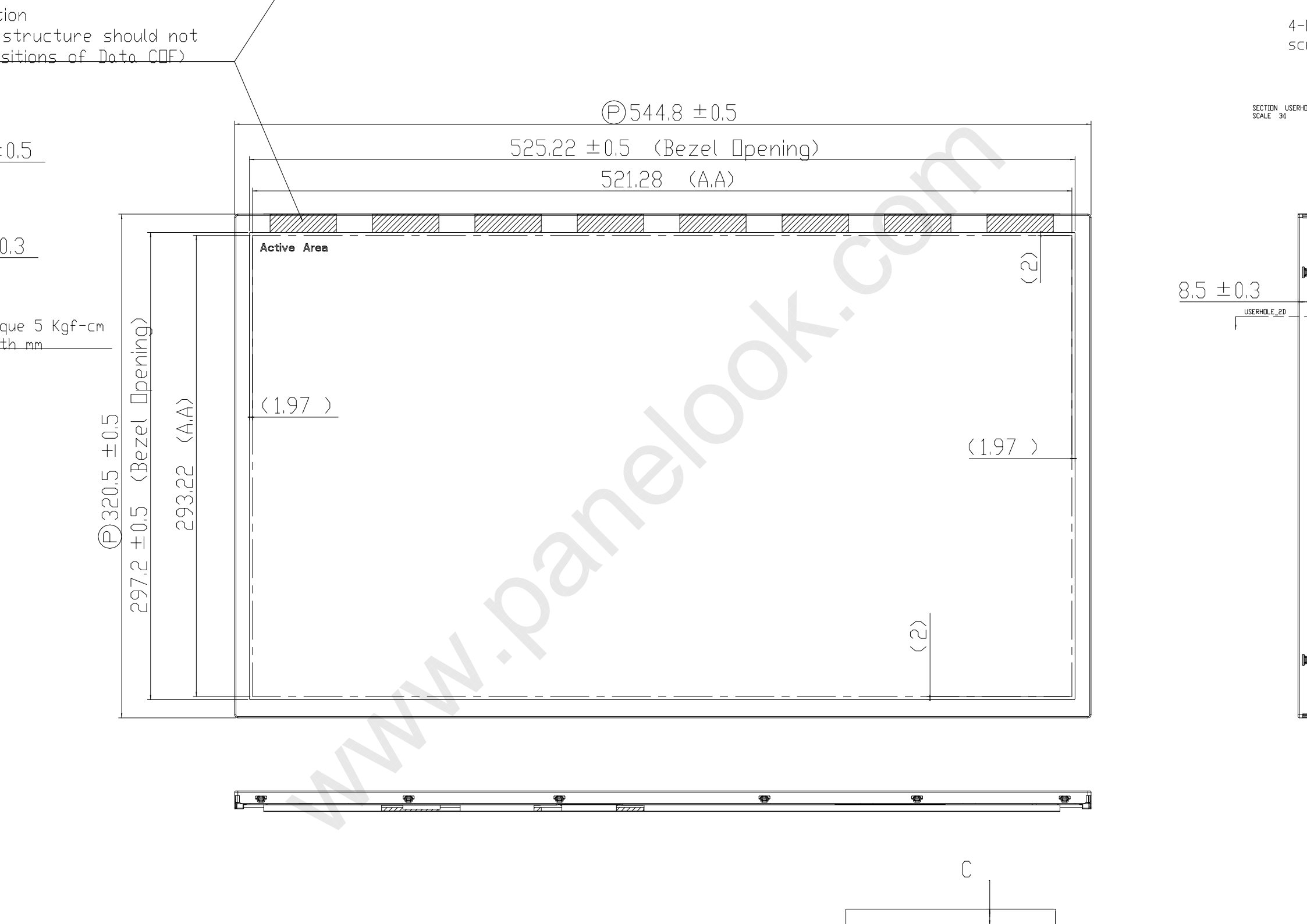
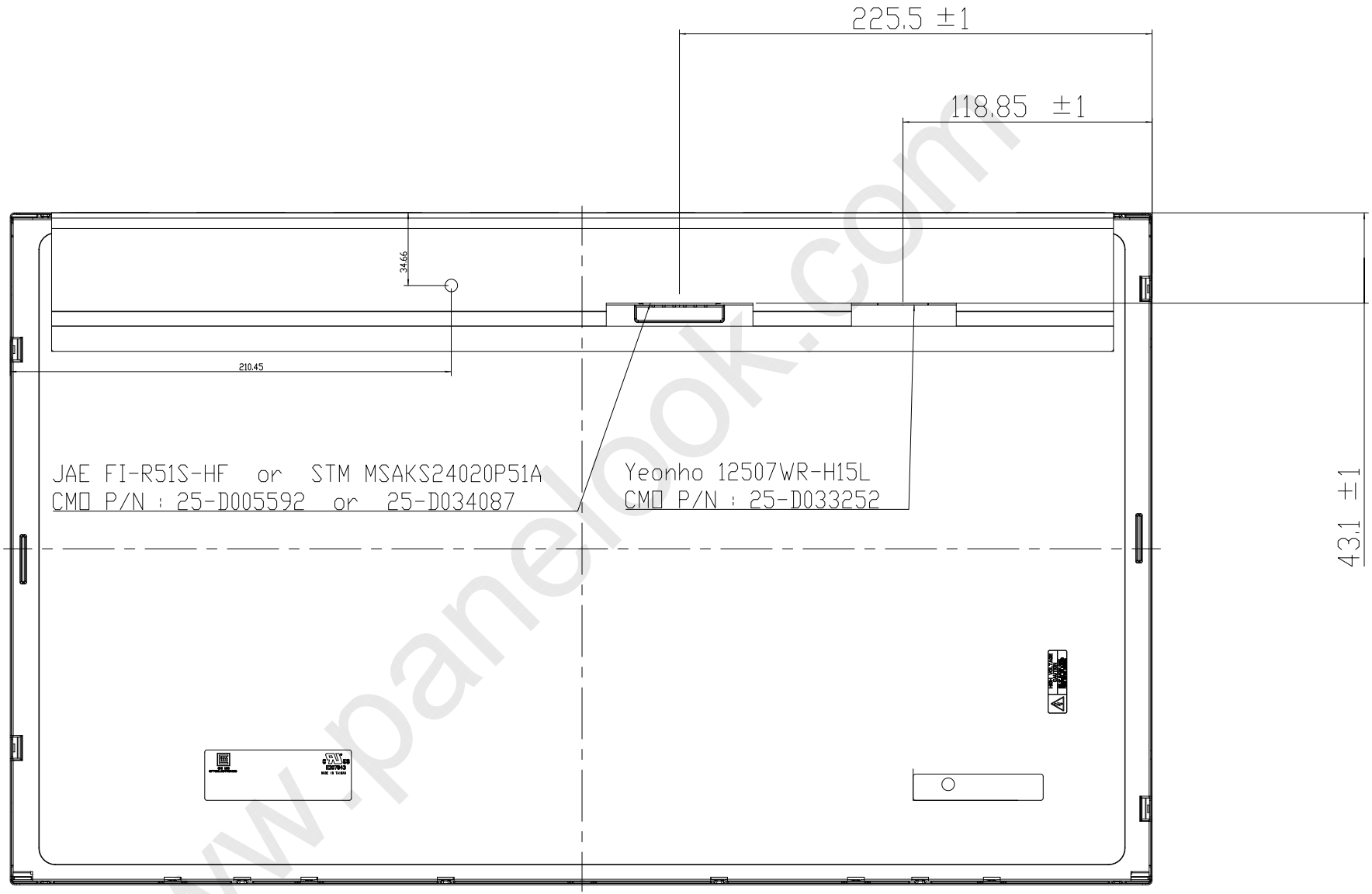


Figure 10-2 packing method

11. MECHANICAL CHARACTERISTIC





NOTES:
1.UNSPECIFIED TOLERANCE : ±0.5mm.