□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V236H3
SUFFIX: PS1

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Roger Huang	CS Tsai

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Jan. 14, 2011	All	All	The approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V236H3-PS1 is a 23.6" TFT Liquid Crystal Display product with driver ICs and 4ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 16.7M colors (6 bit+FRC).

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	23.547
Pixels [lines]	1920 × 1080
Active Area [mm]	521.28(H) x 293.22(V) (23.547" diagonal)
Sub-Pixel Pitch [mm]	0.0905(H) x 0.2715(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 685 g
Physical Size [mm]	534.56 (W) × 339.69 (H) ×2.9 (D) Typ.
Display Mode	Transmissive mode / Normallly white
Contrast Ratio	1000:1 Typ. (Typical value measure at CMO's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle	+85/-85(H), +80/-80(V) Typ. (CR≧10) (Typical value measure at CMO's module)
Color Chromaticity	R = (0.656, 0.328) G = (0.272, 0.601) B = (0.147, 0.101) W= (0.323, 0.367) * Please refer to "color chromaticity" on p.31
Cell Transparency [%]	5.5%
Polarizer Surface Treatment	Anti-Glare coating (Haze 25%), Hard coating (3H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	660	685	710	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)

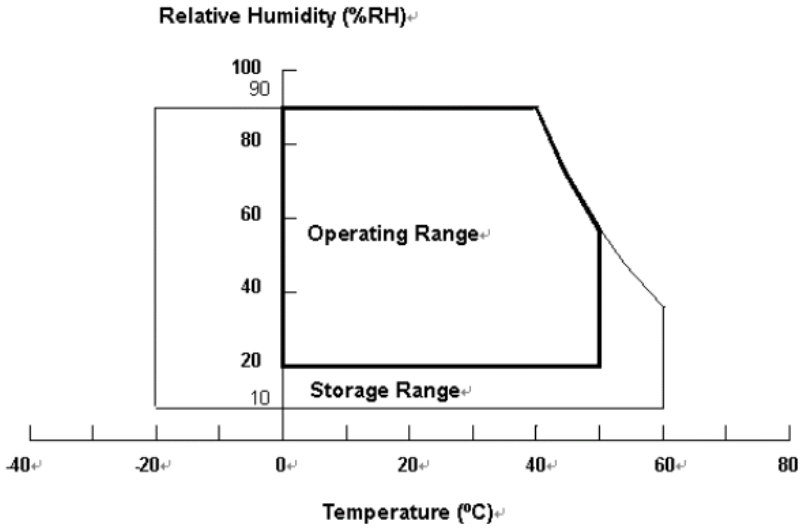
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stroed in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	12.6	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

3. ELECTRICAL CHARACTERISTICS

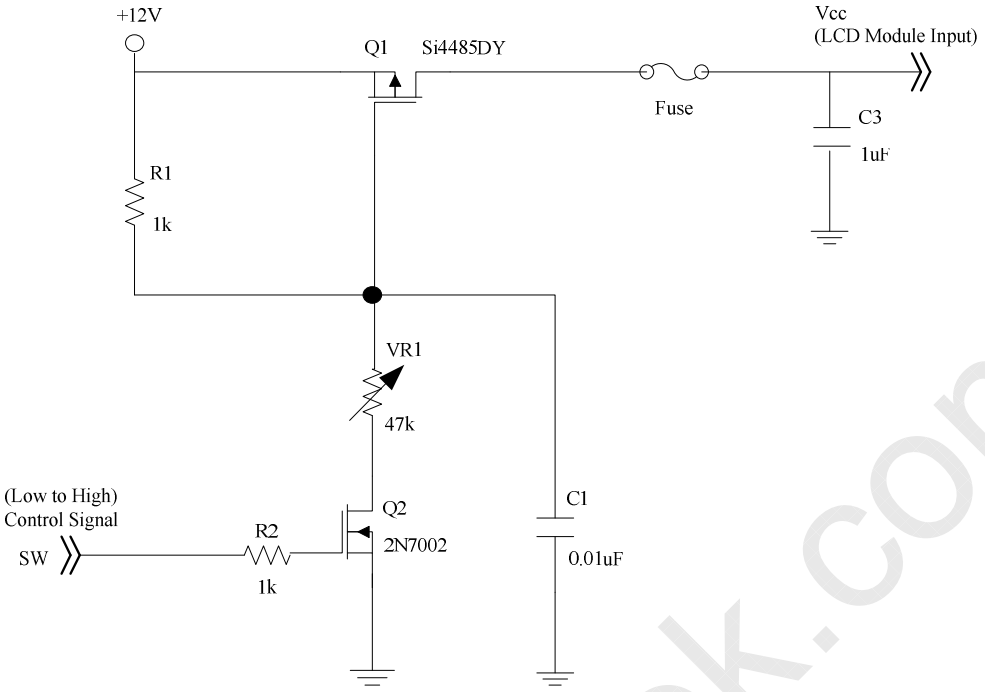
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

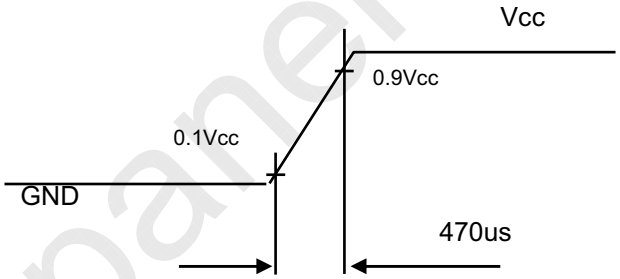
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	12.6	V	(1)
Rush Current		I_{RUSH}	–	–	3.8	A	(2)
Power Consumption	White Pattern	–	–	4.2	5.9	W	(3)
	Horizontal Stripe	–	–	7.68	10.8	W	
	Black Pattern	–	–	7.8	11	W	
Power Supply Current	White Pattern	–	–	0.35	0.5	A	
	Horizontal Stripe	–	–	0.64	0.9	A	
	Black Pattern	–	–	0.65	0.91	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	–	–	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	–	–	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	–	600	mV	
	Terminating Resistor	R_T	–	100	–	ohm	
CMIS interface	Input High Threshold Voltage	V_{IH}	2.7	–	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	–	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

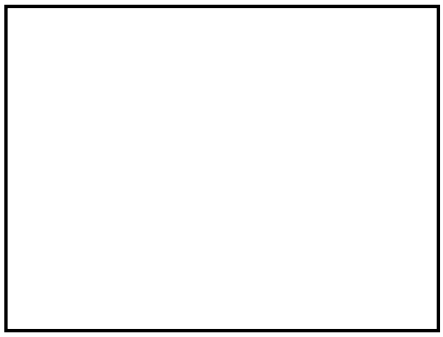


Vcc rising time is 470us



Note (3) The specified power consumption and power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

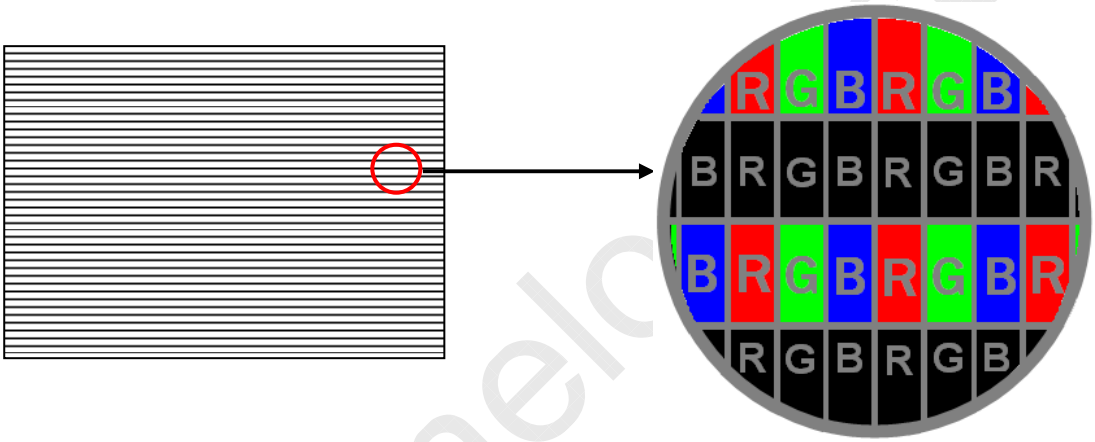
a. White Pattern



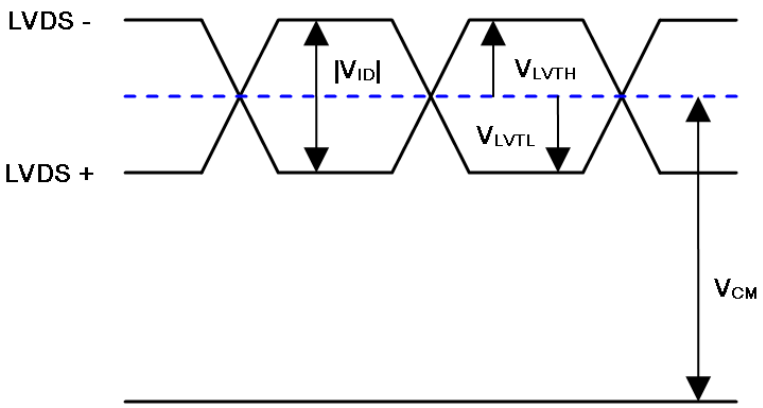
Active Area

b. Black Pattern

Active Area

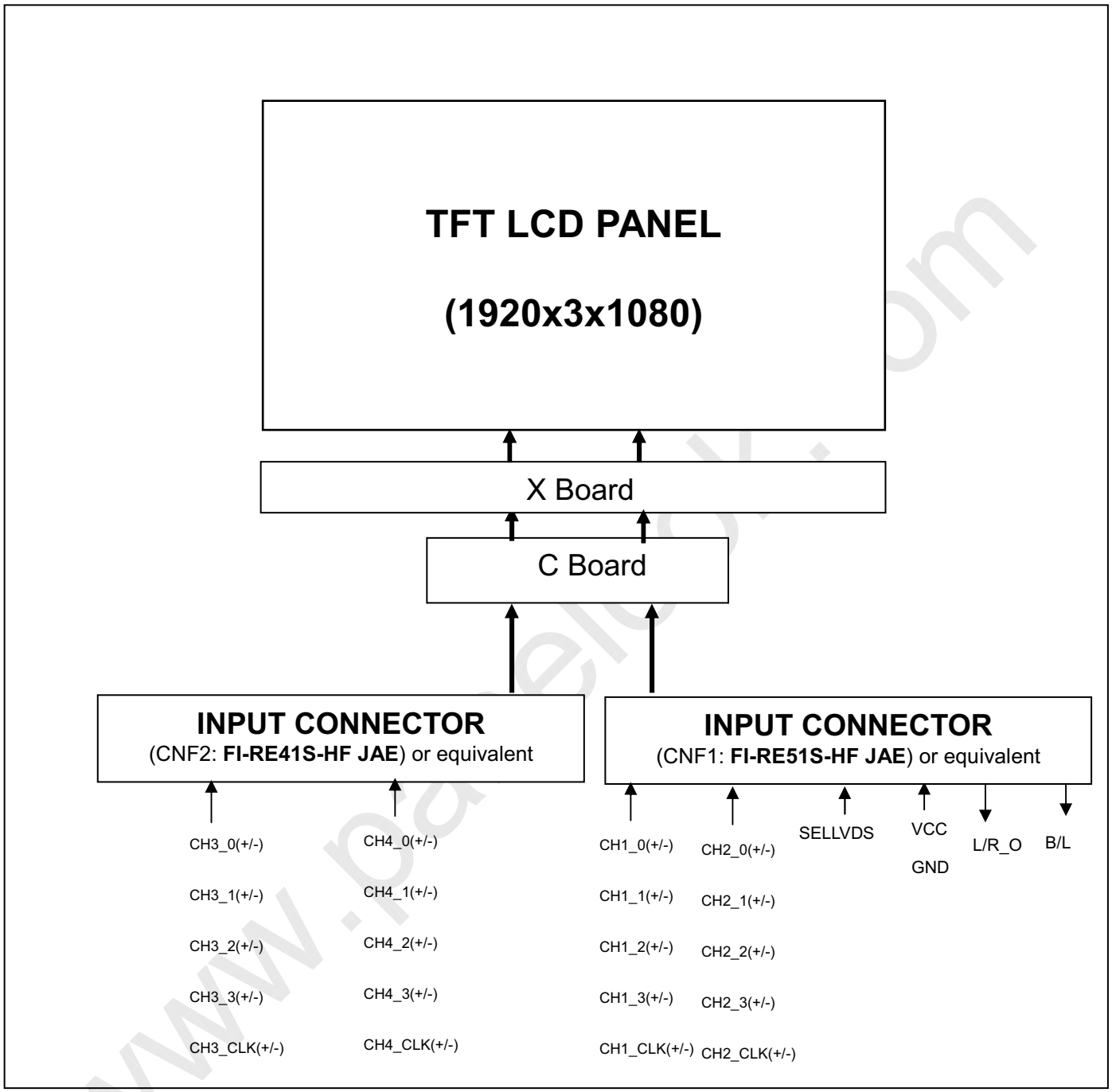


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INTPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Pin Assignment: (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	L/R_O	Output signal for Left Right Glasses control	(7)
6	B/L	Output signal for backlight on/off control signal , H: B/L off, L: B/L on (3D only)	H: +3.3V L: 0V
7	SELLVDS	LVDS Data Format Selection	(2)(6)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	N.C.	No Connection	
25	N.C.	No Connection	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(5)
27	LR	Input signal for Left Right eye frame synchronous	(4)(5)
28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	

29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	NC	No Connection	
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF2 Connector Pin Assignment (FI-RE41S-HF (JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	N.C.	No Connection	
23	N.C.	No Connection	
24	GND	Ground	
25	GND	Ground	
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	

31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32	GND	Ground	
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
38	N.C.	No Connection	
39	N.C.	No Connection	
40	GND	Ground	
41	GND	Ground	

CN6 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	B/L	Output signal for backlight on/off control signal , H: B/L off, L: B/L on (3D only)	H: +3.3V L: 0V
6	L/R_O	Output signal for Left Right Glasses control	(7)
7	N.C.	No Connection	
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND , H=Connect to +3.3V or Open

SELLVDS	Note
L	JEDIA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

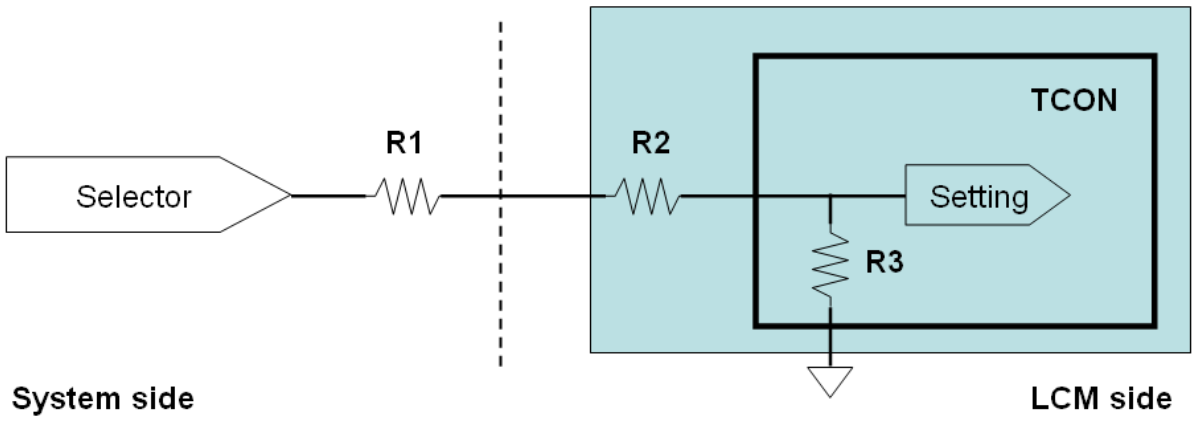
Note (4) Left Right synchronous signal for glasses.

V_{IL}=0~0.8 V, V_{IH}=2.0~3.3 V

LR	Note
L	Right synchronous signal
H	Left synchronous signal

Note (5) 2D/3D, and LR signal pin connected to the LCM side has the following diagram.

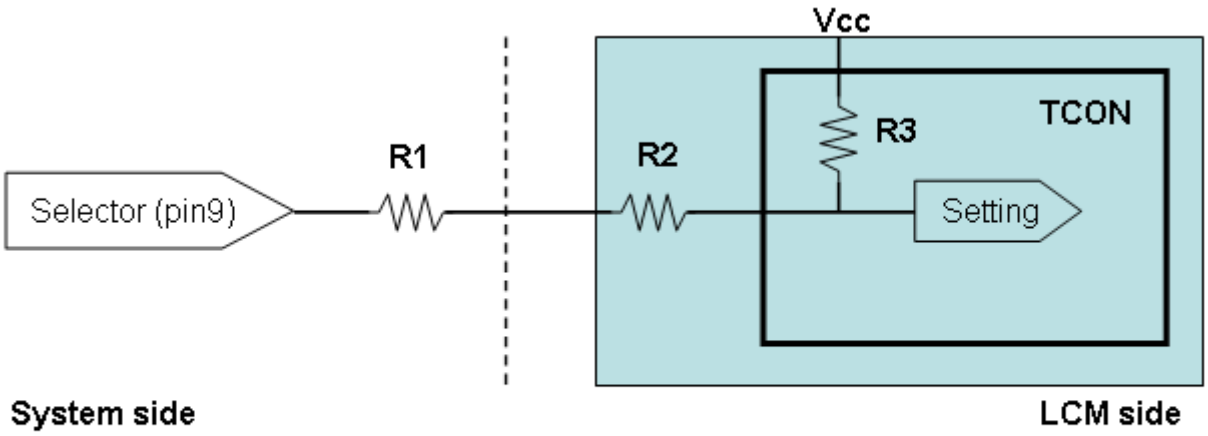
R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



System side: R1 < 1K

Note (6) SELLVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



System side
R1 < 1K

Note (7) The definition of L/R_O signal as follows

L= 0V , H= +3.3V

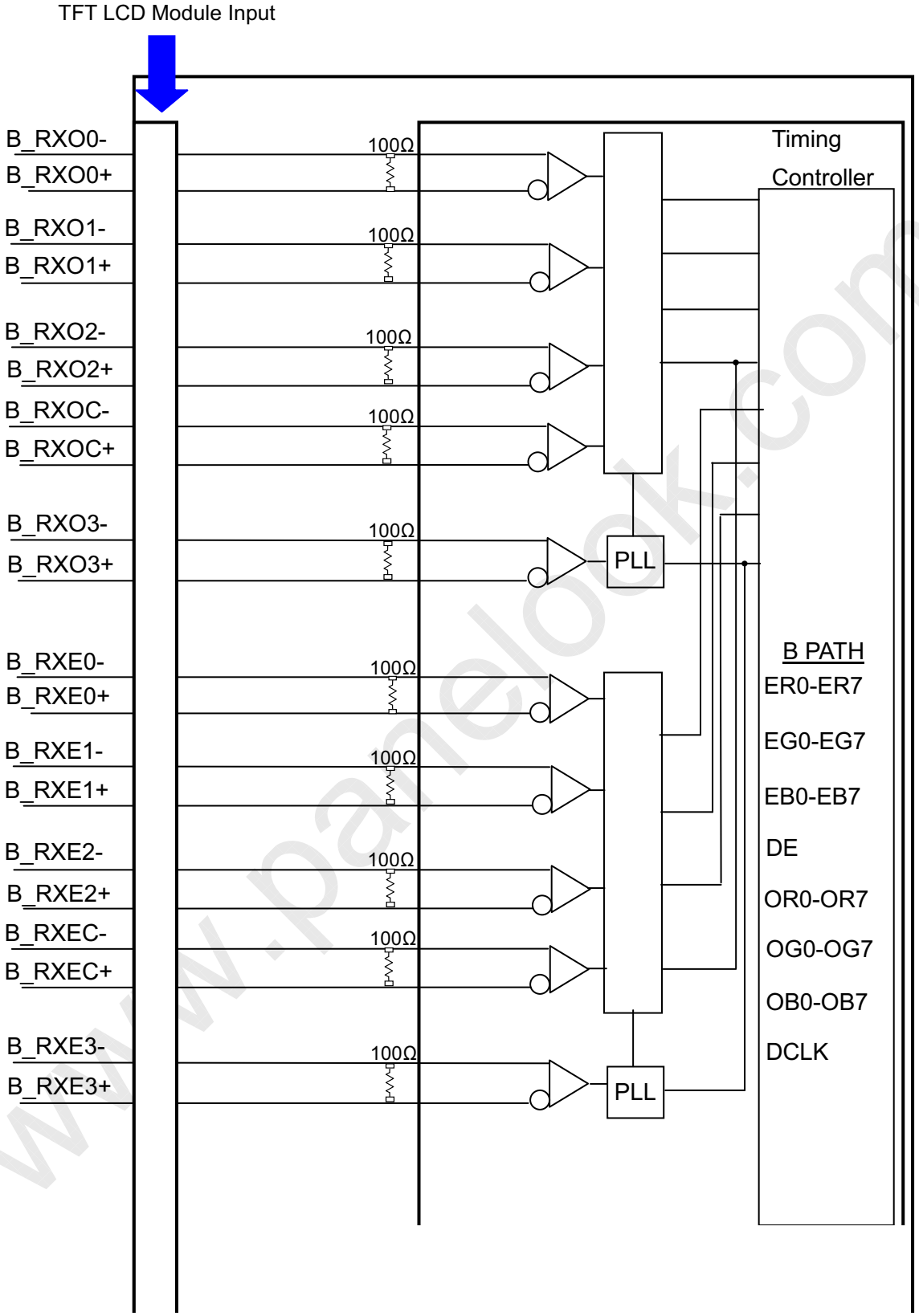
L/R_O	Note
L	Right glass turn on
H	Left glass turn on

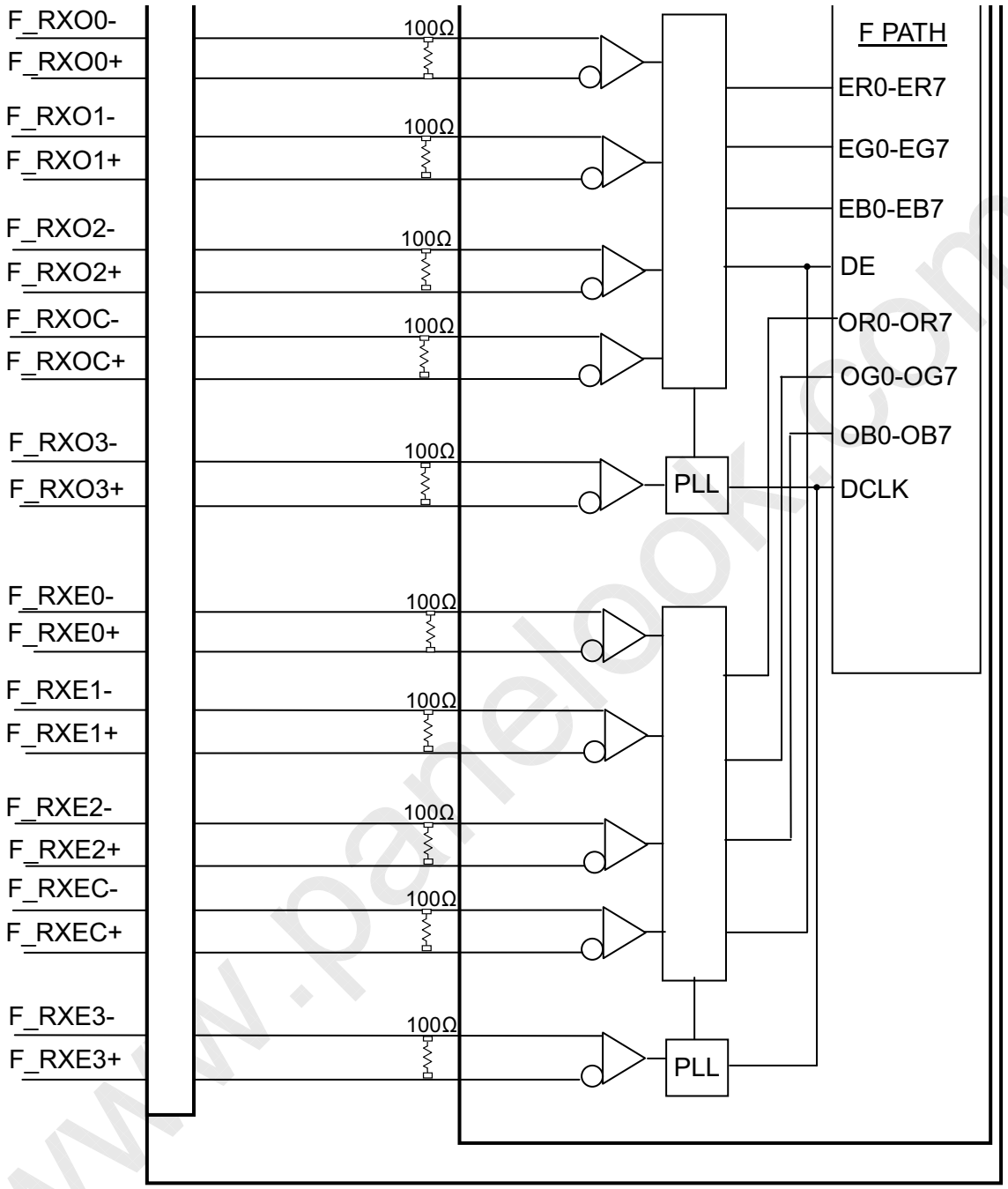
Note (8) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

Note (9) The screw hole which is distant from the connector is merged with Ground

5.2 BLOCK DIAGRAM OF INTERFACE





ER0~ER7	Even pixel R data	OR0~OR7	Odd pixel R data
EG0~EG7	Even pixel G data	OG0~OG7	Odd pixel G data
EB0~EB7	Even pixel B data	OB0~OB7	Odd pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

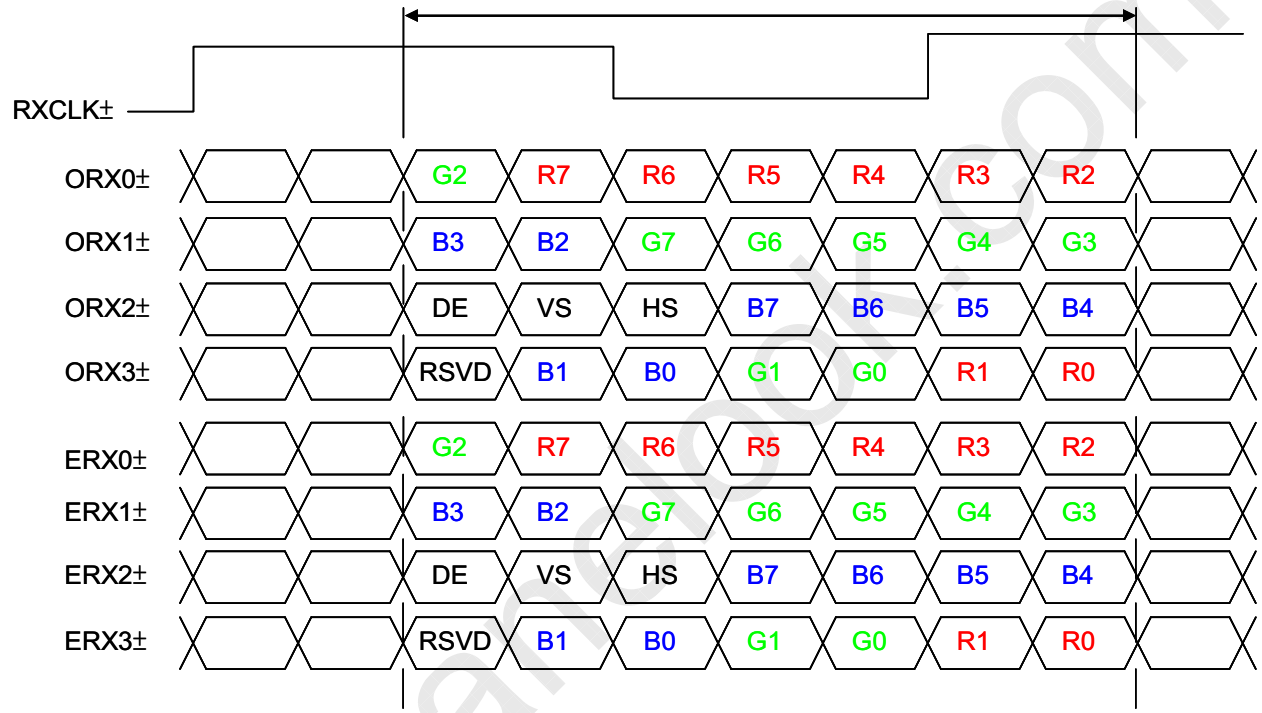
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.3 LVDS INTERFACE

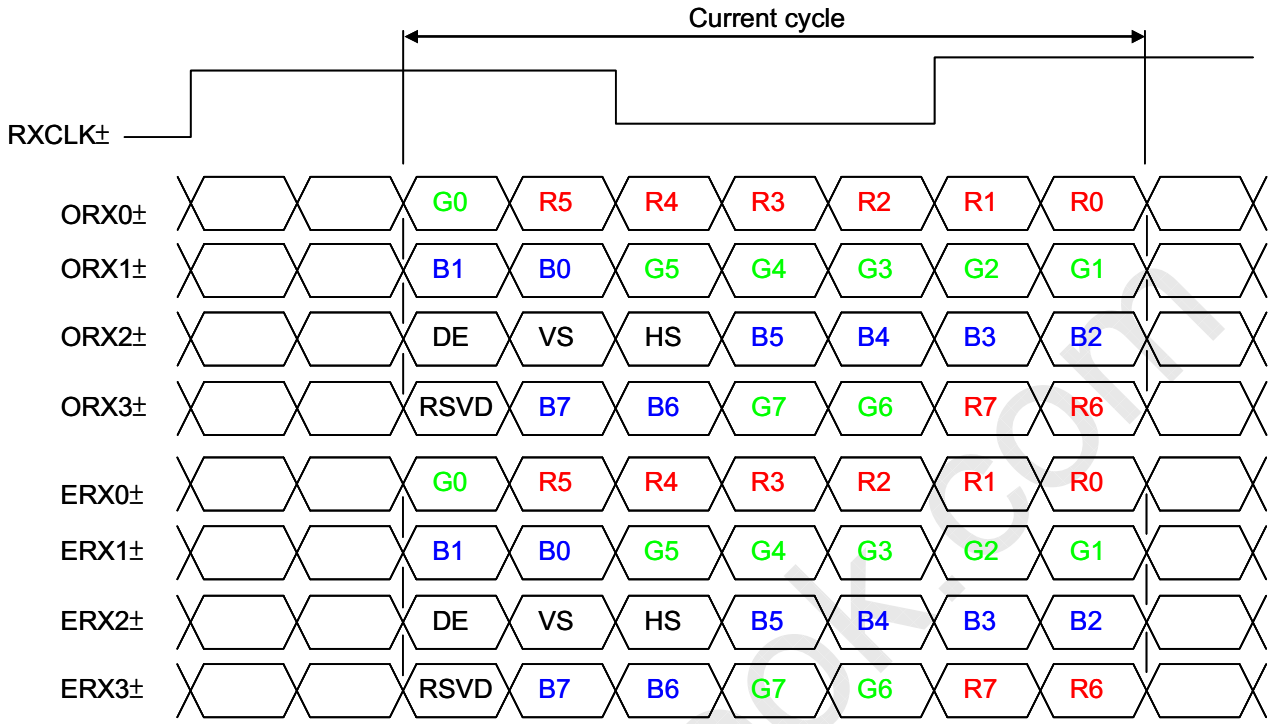
JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

JEDIA Format



VESA Format



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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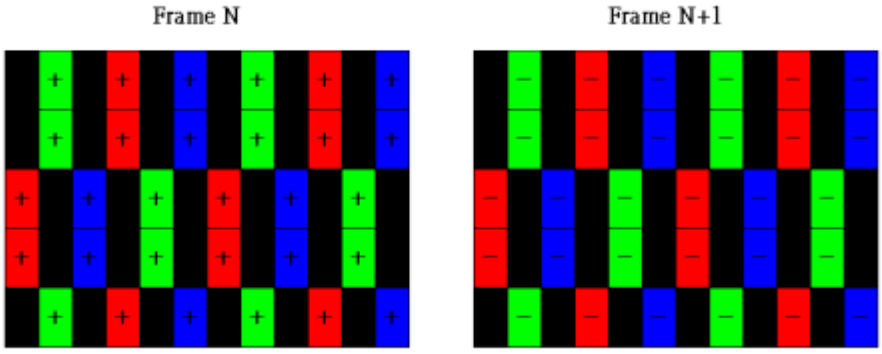
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern:

2 line-inversion pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com.The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

a. USB Sensor Board.
b. Programmable software.

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	96.23	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	

6.1.1 Timing spec for Frame Rate(F_{r5} = 100Hz)

Vertical Active Display Term	2D Mode	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	35	45	55	Th	—
	3D Mdoe	Total	Tv	1524			Th	(6)
		Display	Tvd	1080			Th	
		Blank	Tvb	444			Th	
Horizontal Active Display Term	2D Mode	Total	Th	540	550	575	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	60	70	95	Tc	—
	3D Mdoe	Total	Th	525			Tc	(7)
		Display	Thd	480			Tc	
		Blank	Thb	45			Tc	

6.1.2 Timing spec for Frame Rate(F_{r6} = 120Hz)

Vertical Active Display Term	2D Mode	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	35	45	55	Th	—
	3D Mdoe	Total	Tv	1524			Th	(6)

		Display	Tvd	1080			Th	
		Blank	Tvb	444			Th	
Horizontal Active Display Term	2D Mode	Total	Th	540	550	575	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	–
		Blank	Thb	60	70	95	Tc	–
	3D Mdoe	Total	Th	525			Tc	(7)
		Display	Thd	480			Tc	
		Blank	Thb	45			Tc	

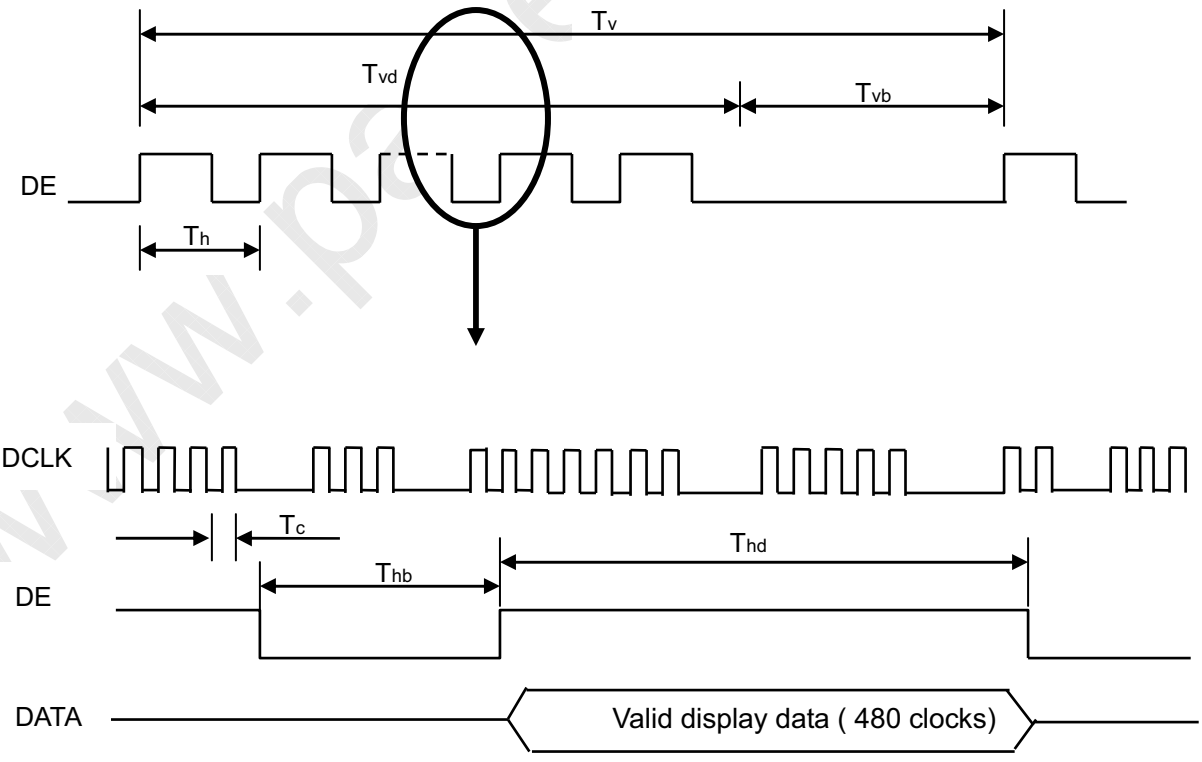
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

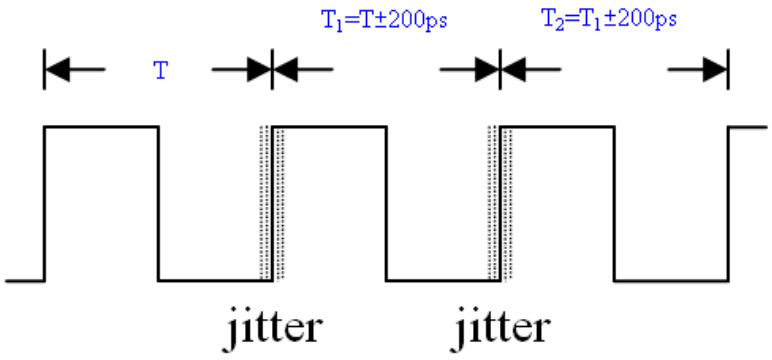
$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

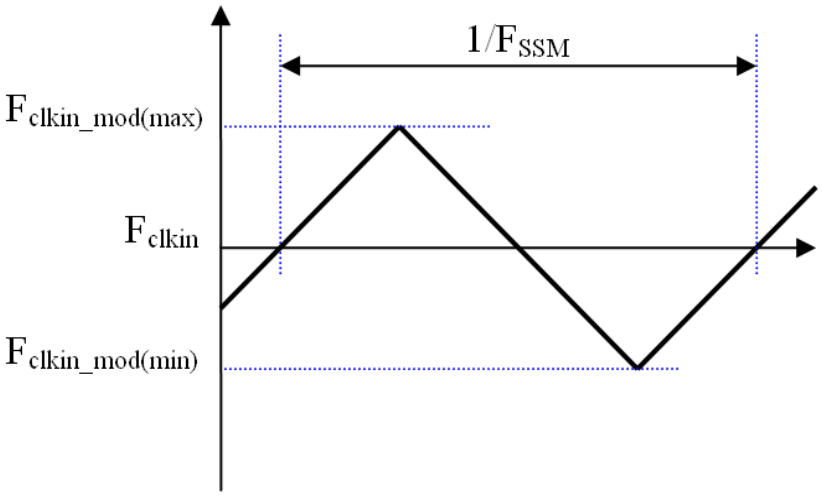
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

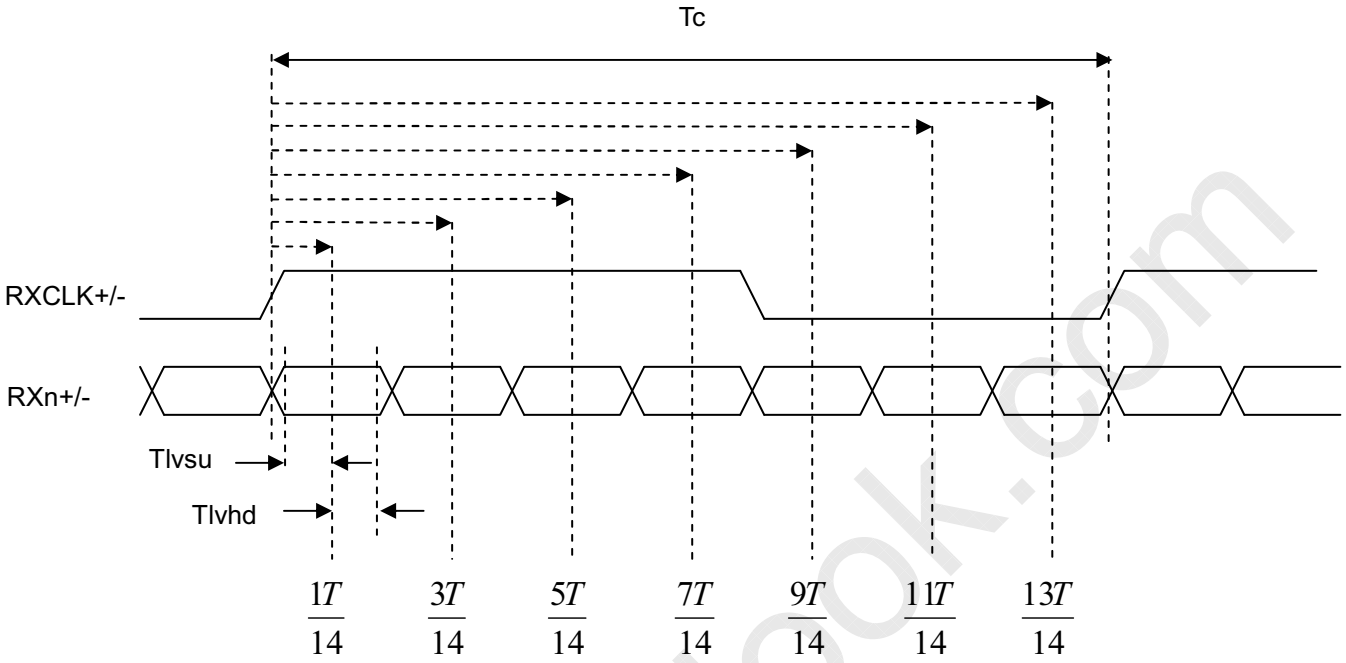


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



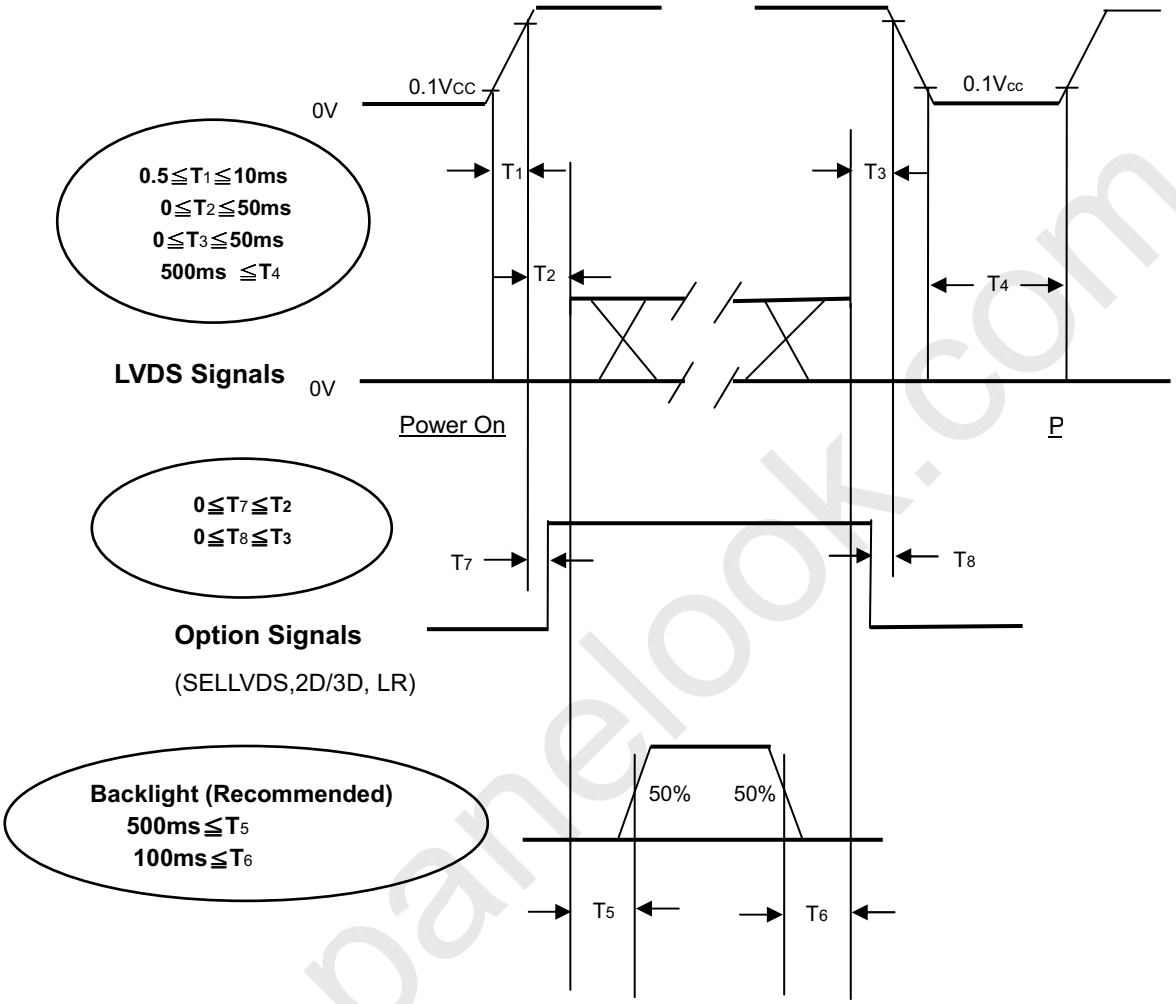
Note (6) Please fix the Vertical timing (Vertical Total =1524 / Display =1080 / Blank = 444) in 3D mode.

Note (7) Please fix the Horizontal timing (Horizontal Total =2100 / Display =1920 / Blank = 180) in 3D mode

6.2 POWER ON/OFF SEQUENCE

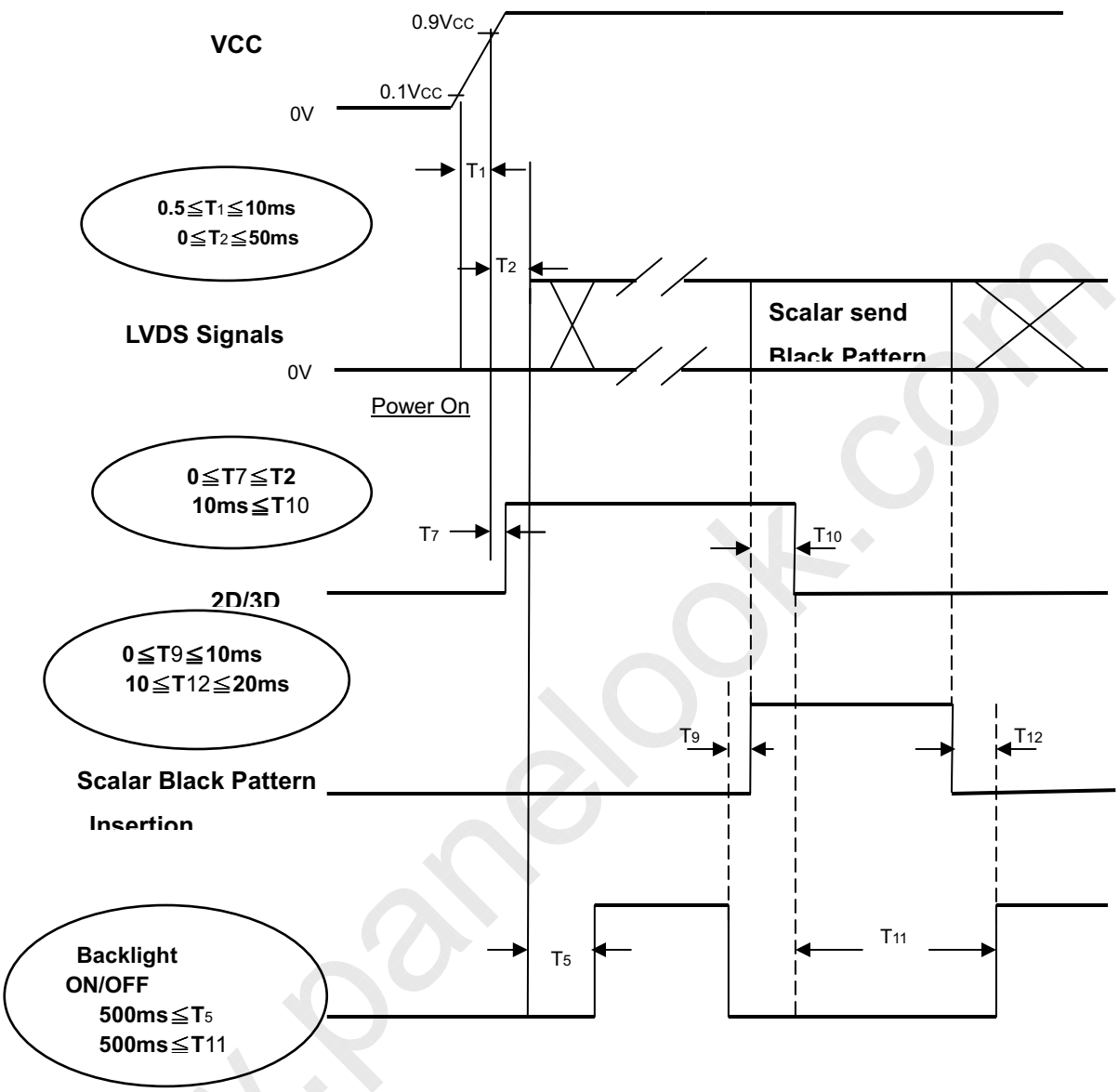
6.2.1 POWER ON/OFF SEQUENCE(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

6.2.2 2D to 3D SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

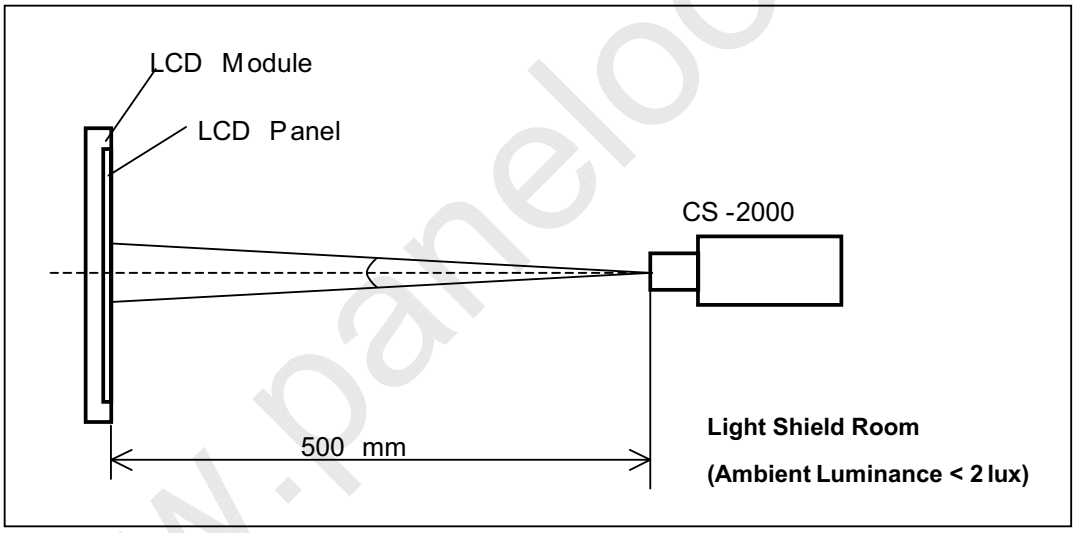
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	60 ± 1.2	mA
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction Standard light source "C"	Typ-0.03	0.656	Typ+0.03	-	(0)
		Rcy			0.328		-	
	Green	Gcx			0.272		-	
		Gcy			0.601		-	
	Blue	Bcx			0.147		-	
		Bcy			0.107		-	
	White	Wcx			0.323		-	
		Wcy			0.367		-	
Center Transmittance		T%	θ_x=0°, θ_Y =0° with CMI module	4.9	5.5	-	%	(1),(6)
Contrast Ratio		CR			1000	-	-	(1),(3)
Response Time		T_R	θ_x=0°, θ_Y =0° with CMO Module	-	0.8	-	ms	(1),(4)
		T_F		-	2.8	-	ms	
White Variation		δW	θ_x=0°, θ_Y =0° with CMI module	-	-	1.33	-	(1),(5)
Cross Talk	CT	2D	-	-	-	4	%	(7)
		3D-W	-	-	0.4	-	%	(8)
		3D-D	-	-	12	-	%	(8)
Viewing Angle	Horizontal	θ_x+	CR≥10 With CMO module	-	85	-	Deg.	(1),(2)
		θ_x-		-	85	-		
	Vertical	θ_Y+		-	80	-		
		θ_Y-		-	80	-		
Absorption direction of the up polarizer		Φ_{up}	-	-	45	-	Deg.	(9)

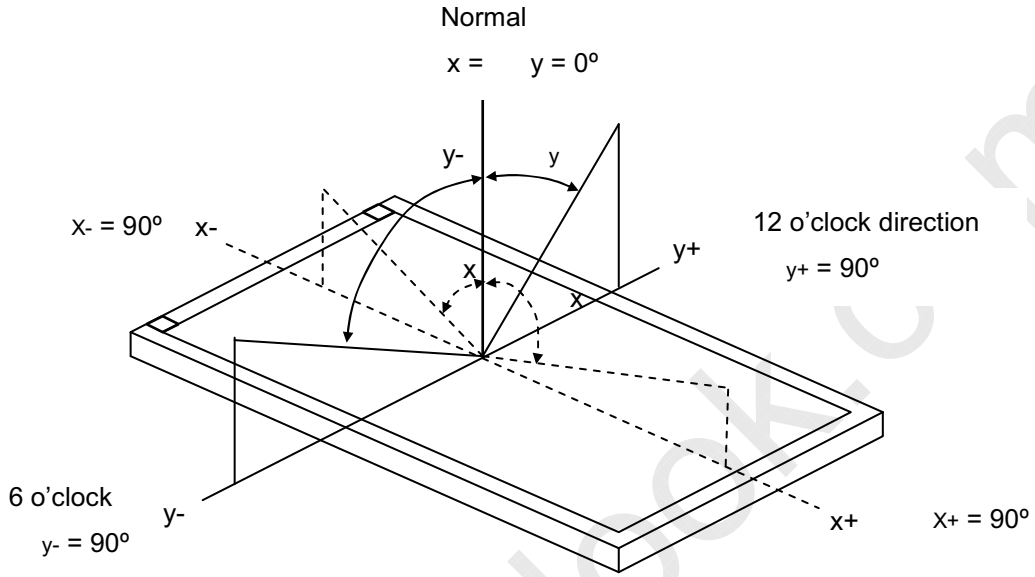
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's and BLU's spectrum at center point. White is without signal input and R,G,B are with signal input. BLU is supplied by CMO.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R, 2 選 1)



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

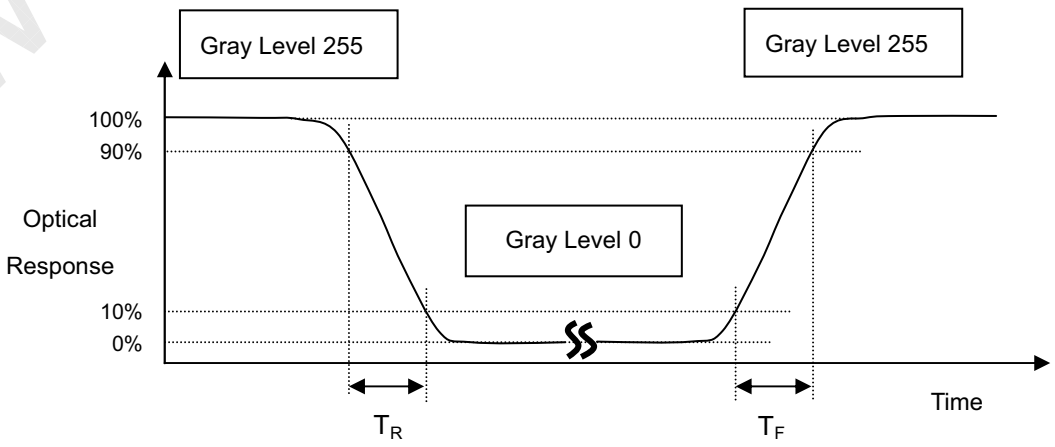
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (5).

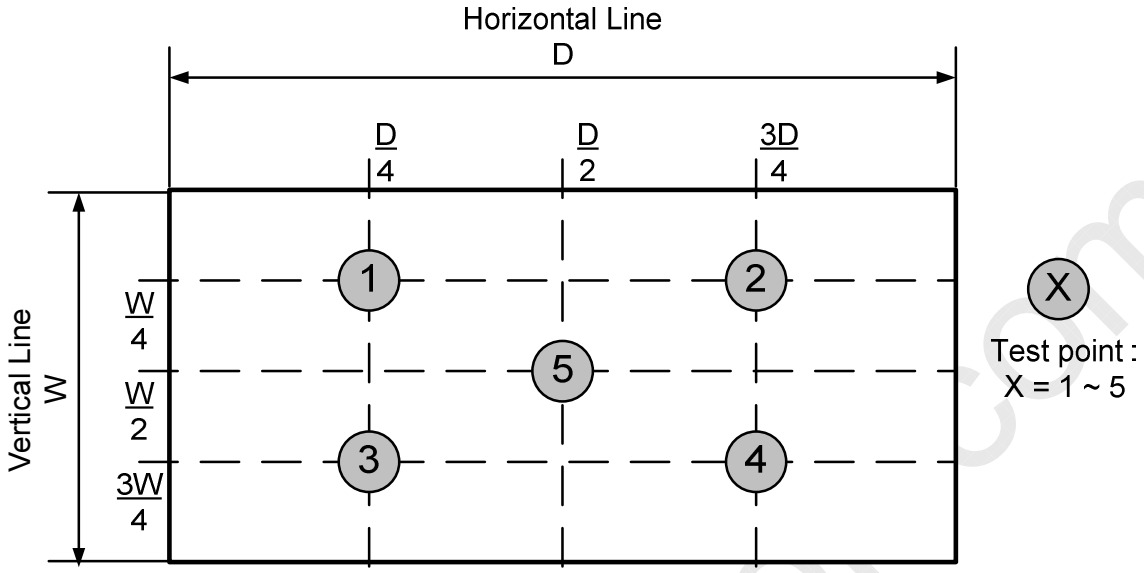
Note (4) Definition of Response Time (T_R, T_F):



Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



Note (6) Definition of Transmittance (T%) :

Measure the luminance of gray level 255 at center point of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\%$$

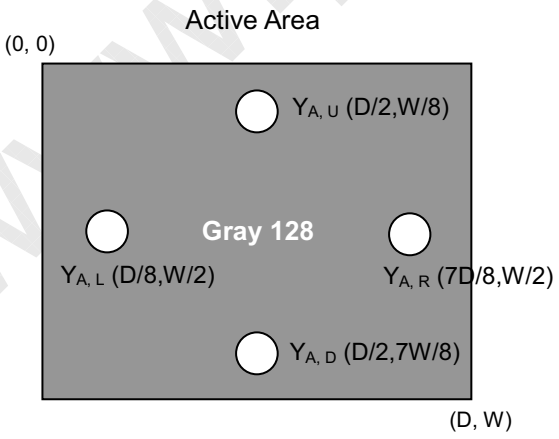
Note (7) Definition of Cross Talk (CT):

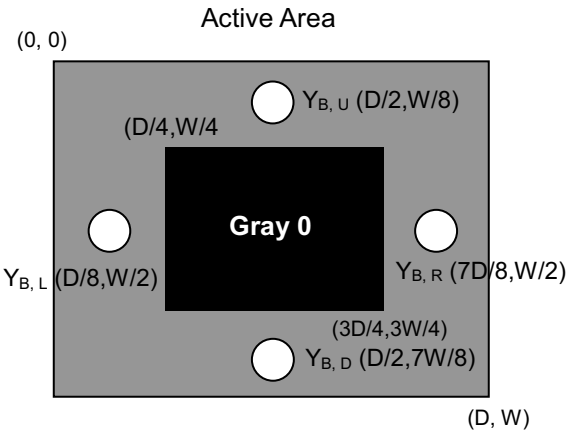
$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)

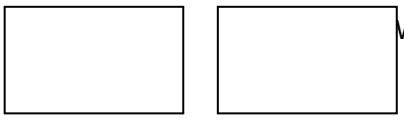




Note(8) Definition of the 3D mode performance (measured under 3D mode):

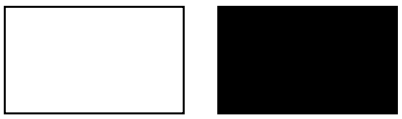
a. Test pattern

Left eye image and right eye image are displayed alternated



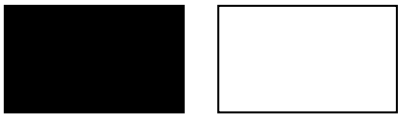
W

Left eye image: W255; Right eye image: W255



WB

Left eye image: W255; Right eye image: W0



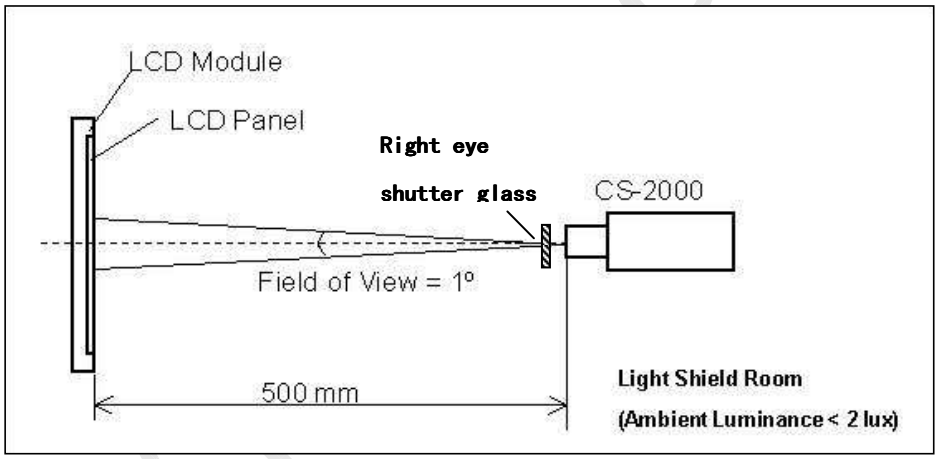
BW

Left eye image: W0; Right eye image: W255

BB

Left eye image: W0; Right eye image: W0

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation.

The luminance of the test pattern “WW”, denoted L(WW); the luminance of the test pattern ”WB”, denoted L(WB); the luminance of the test pattern “BW”, denoted L(BW); the luminance of the test pattern “BB”, denoted “L(BB)

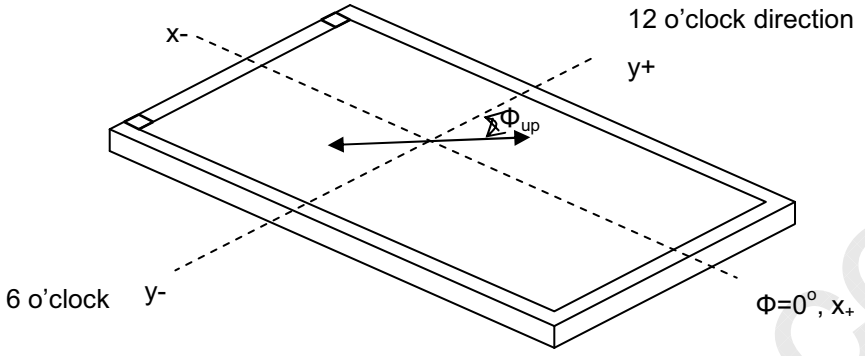
c. Definition of the Center Luminance of White, Lc (3D) : L(WW)

d. Definition of the 3D mode white crosstalk, CT (3D-W) : $CT(3D-W) \equiv \left| \frac{L(WB)-L(BB)}{L(WW)-L(BB)} \right|$

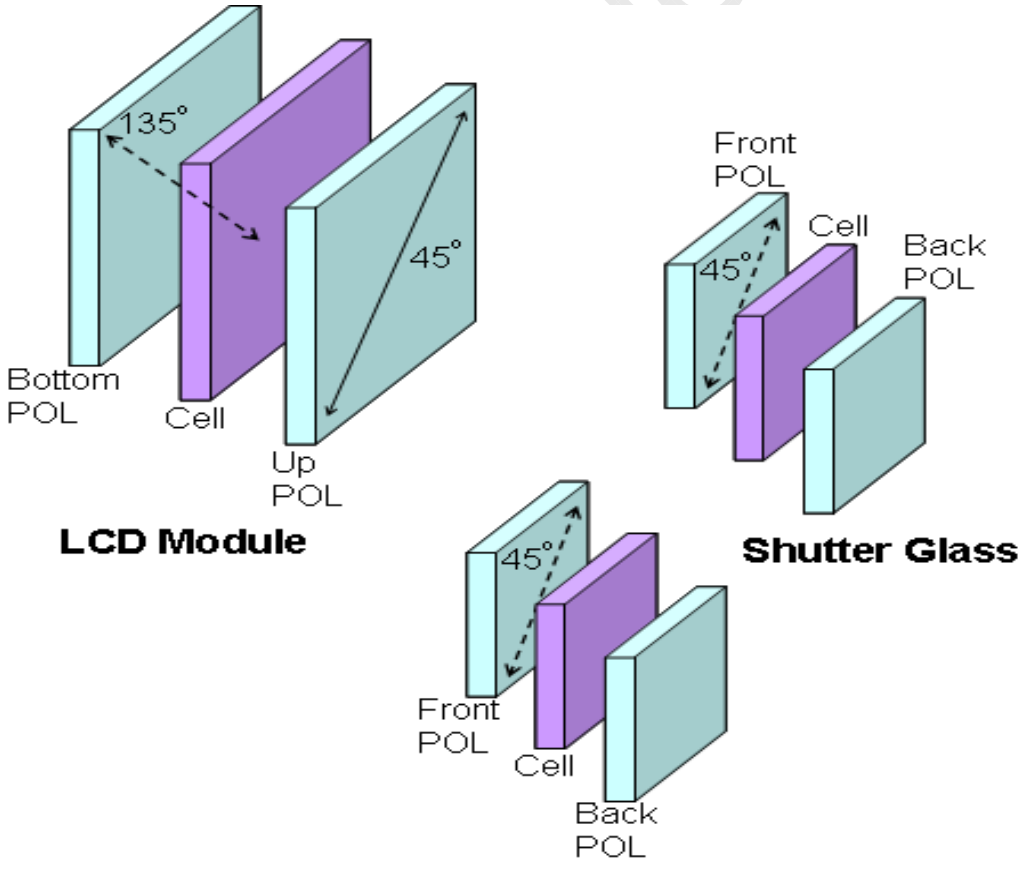
e. Definition of the 3D mode dark crosstalk, CT (3D-D) : $CT(3D-D) \equiv \left| \frac{L(WW)-L(BW)}{L(WW)-L(BB)} \right|$

Note (9) This is a reference for designing the shutter glasses of 3D application. (TN case)

Definition of the absorption direction of the up polarizer:



The absorption axis of the front polarizer of the shutter glasses should be parallel to this panel absorption direction to get a maximum 3D mode luminance.



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] The distance between COF edge and rib of BLU must bigger than 5mm. This can prevent the damage of COF when assemble the module.

[6] Do not design sharp-pointed structure / parting line / tooling gate on the COF position of plastic parts, because the burr will scrape the COF.

[7] If COF would bended to assemble in the module. Do not put the IC location on the bending corner of COF.

[8] The gap between COF IC and any structure of BLU must bigger than 2mm. This can prevent the damage of COF IC

[9] Bezel opening must have no burr. Burr will scrape the panel surface.

[10] Bezel of module and bezel of set can not press or touch the panel surface. It will make light leakage or scrape. When module used FFC / FPC, but no FFC / FPC to be attached in the open cell. Customer can refer the FFC / FPC drawing and buy it by self.

[11] The gap between Panel and any structure of Bezel must bigger than 2mm. This can prevent the damage of Panel.

[12] Do not plug in or pull out the I/F connector while the module is in operation.

[13] Do not disassemble the module.

[14] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[15] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[16] When storing modules as spares for a long time, the following precaution is necessary.

[16.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[16.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[17] When ambient temperature is lower than 10ºC, the display quality might be reduced.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

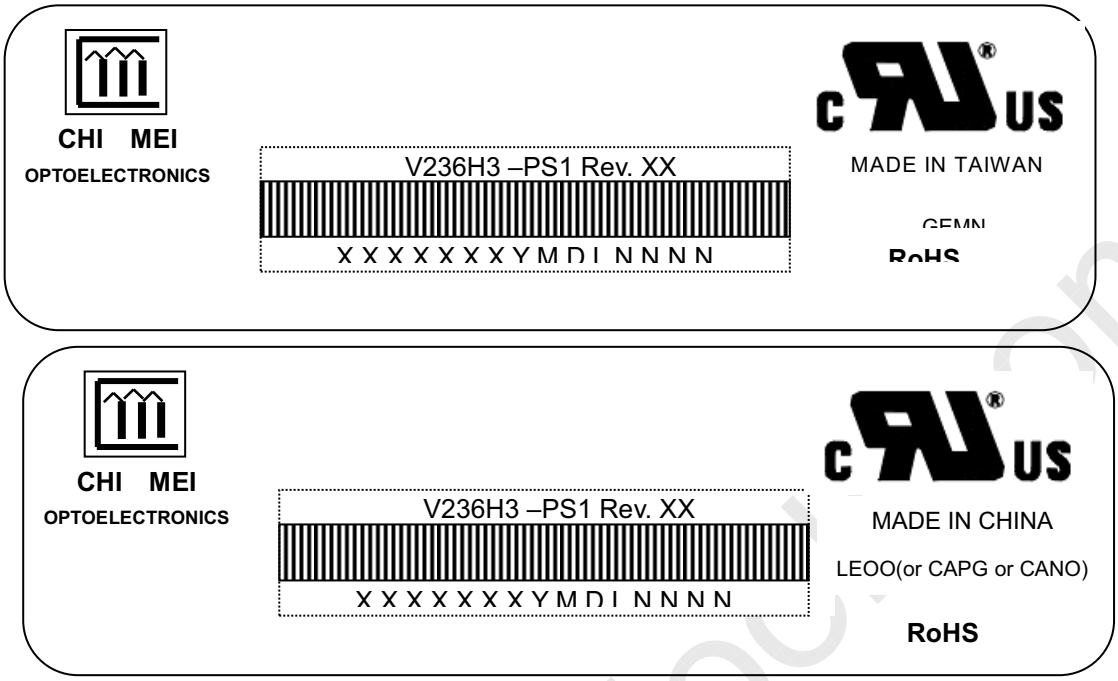
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

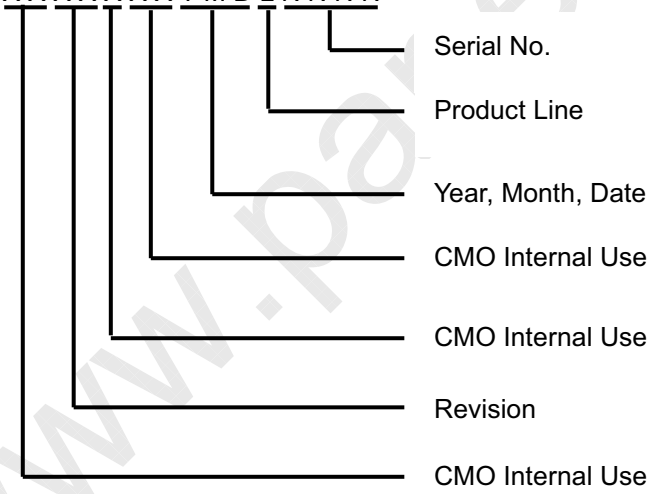
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V236H3-PS1

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 24 open cells / 1 Box

(2) Box dimensions : 670(L)x575(W)x325(H)mm

(3) Weight : approximately 24Kg (24 open cells per box)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

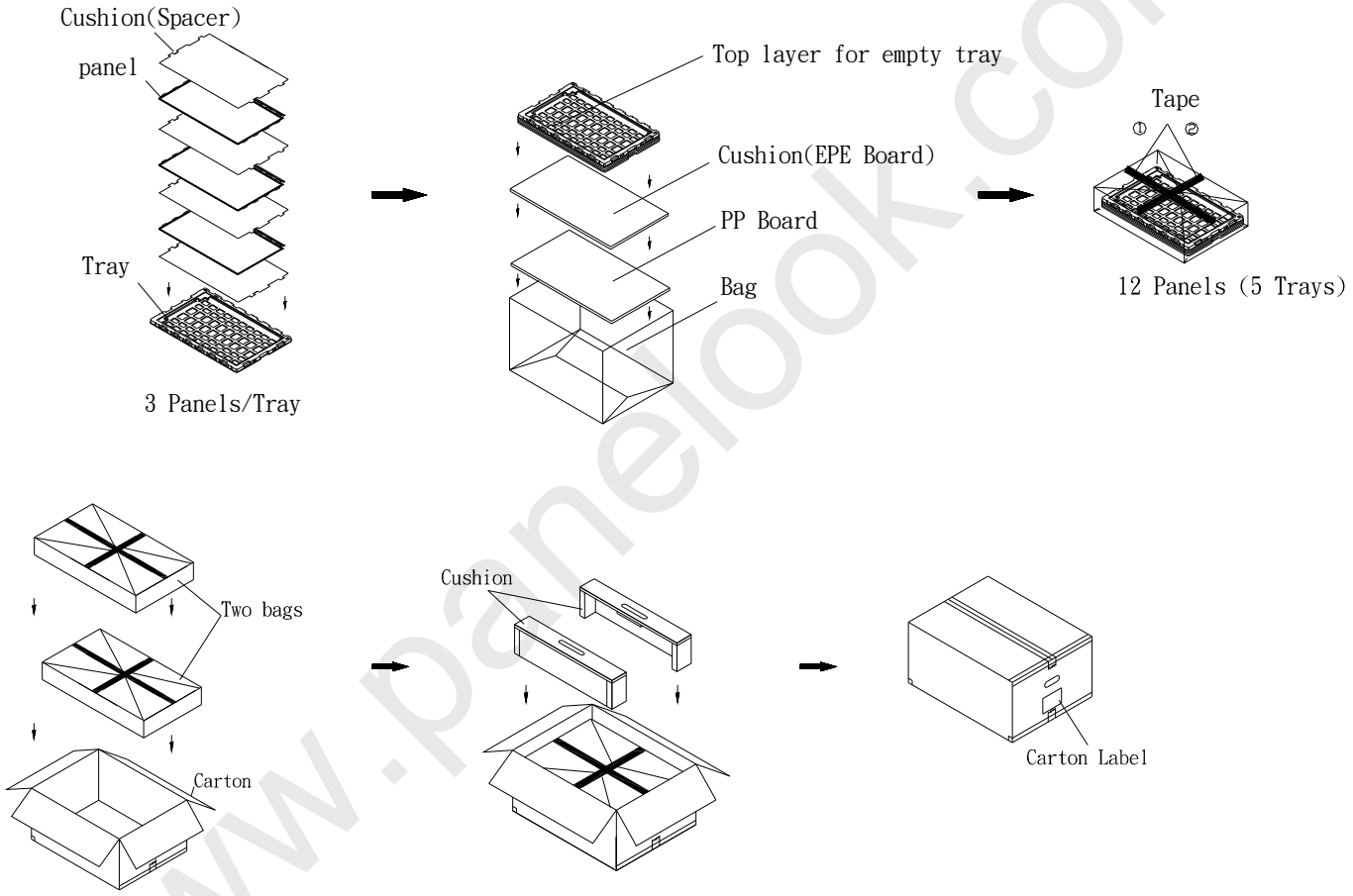


Figure.10-1 packing method

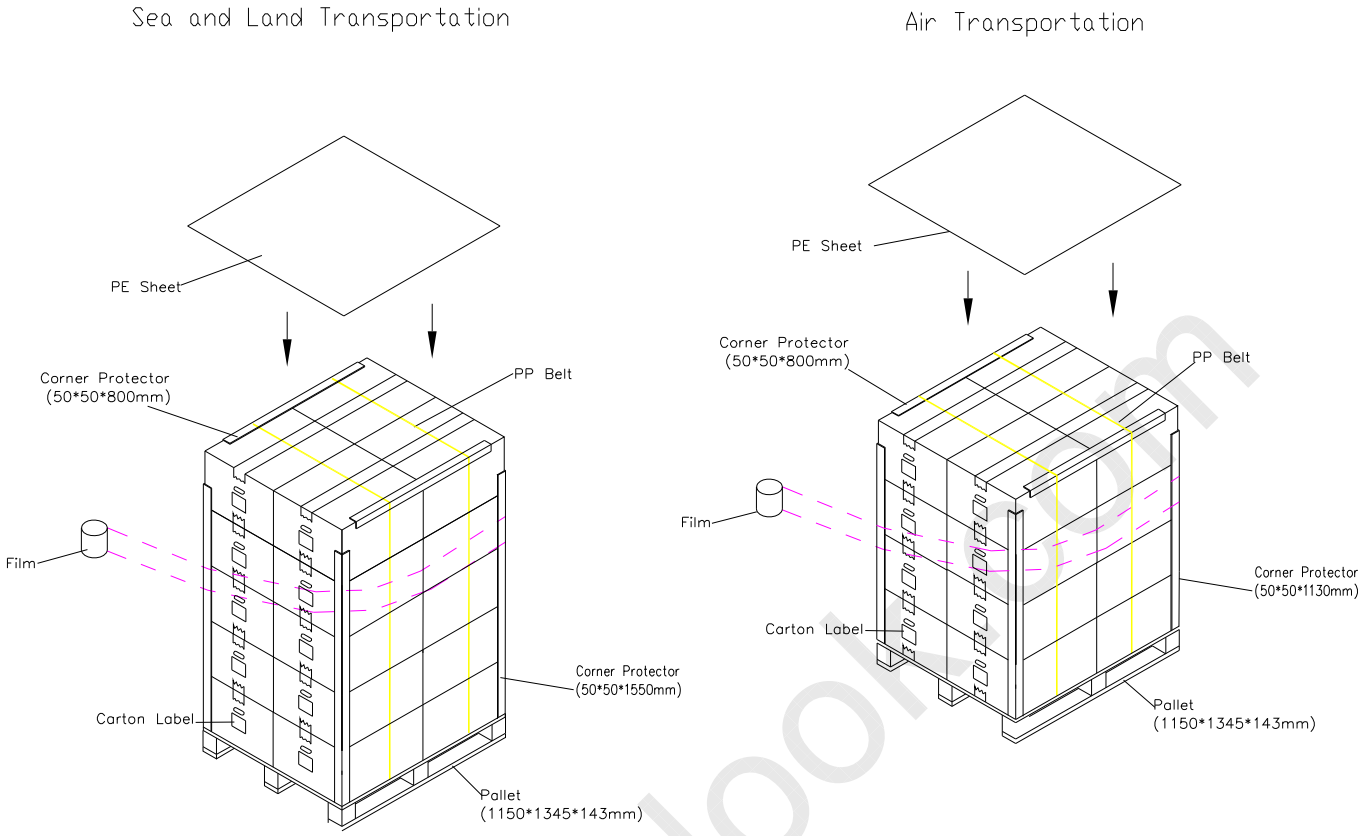
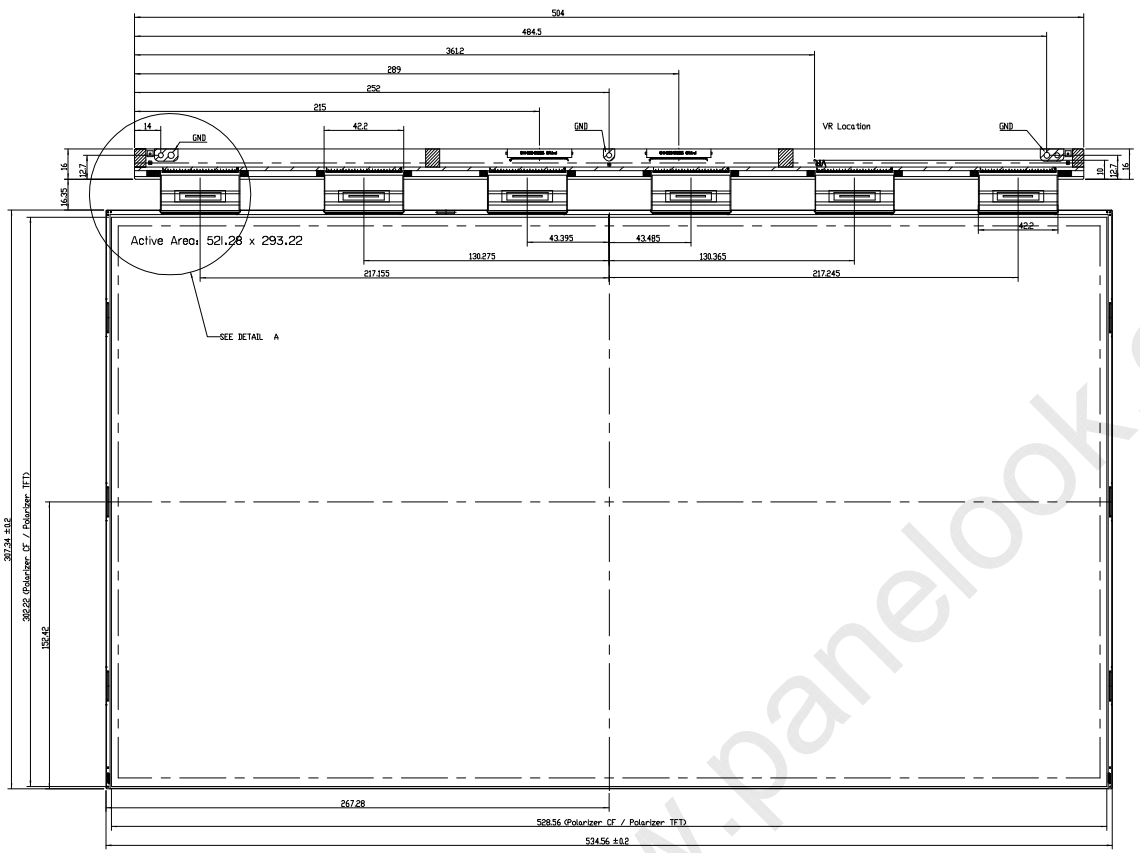
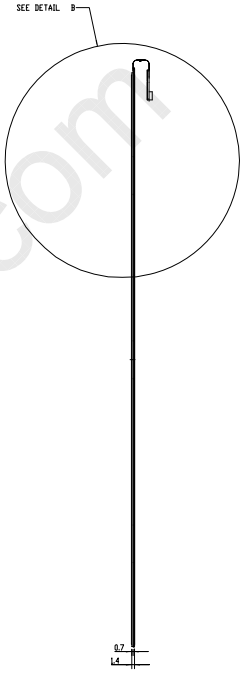
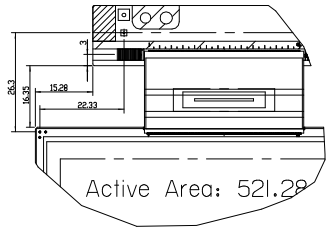


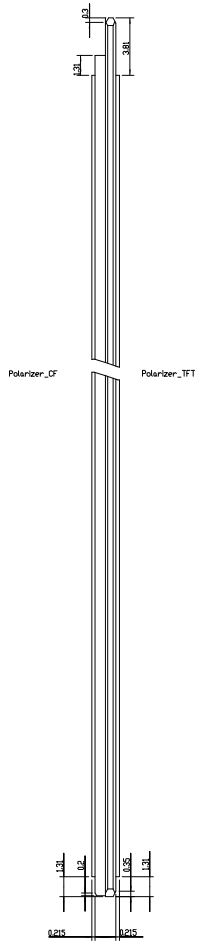
Figure.10-2 packing method

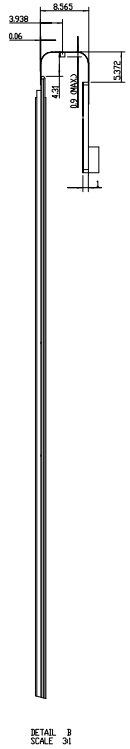
11. MECHANICAL CHARACTERISTIC

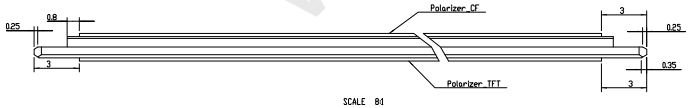








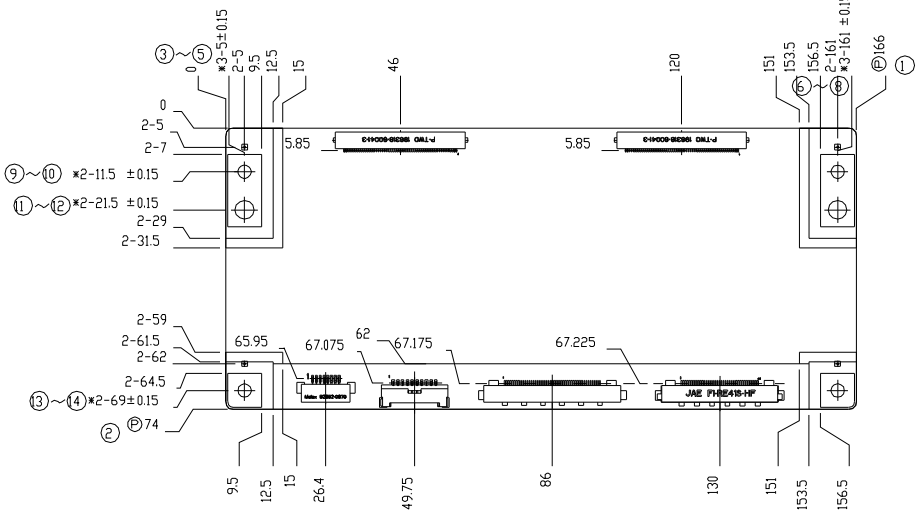


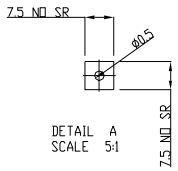


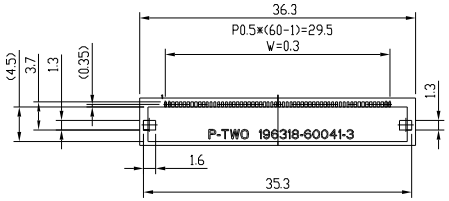
Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	ASSY_PANEL_CCF_PCB_V236H3-L11		REV. A
Approved	KL_LIN	Drawing No.	V236341B1A
Checked	TIGER	Part No.	TBD
Drawer	BELLE_CHENG	Material	TBD
Designer	BENEI_HUANG	Date	10-Dec-2010
		Scale	3:1
		Sheet	1 / 1
		Unit	mm

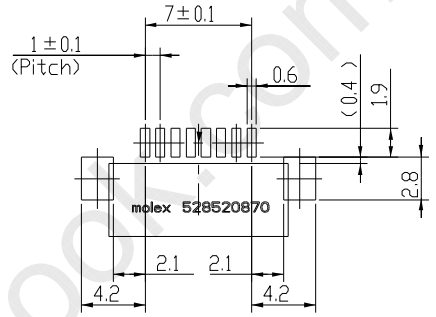
CHIMEI INNOLUX CORP.



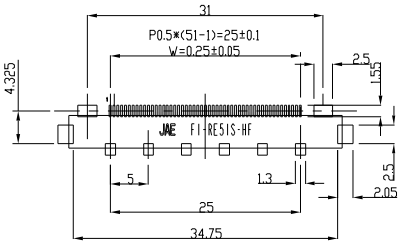




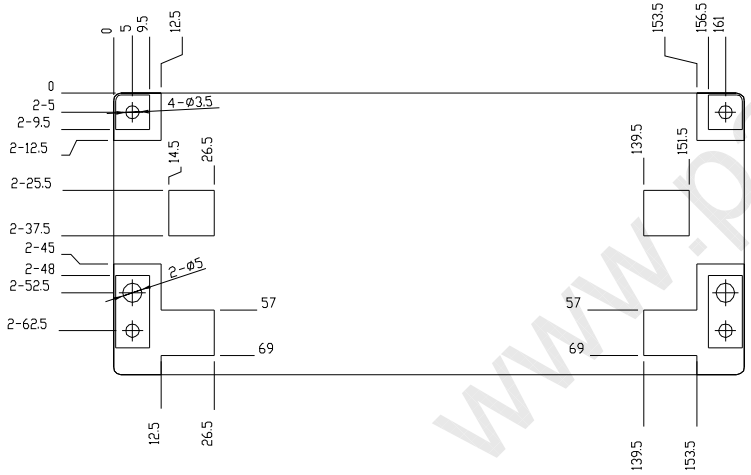
P-TWO 196318-60041-3
OR
STARCONN
106C60-102001-01-R
SCALE : 2.000

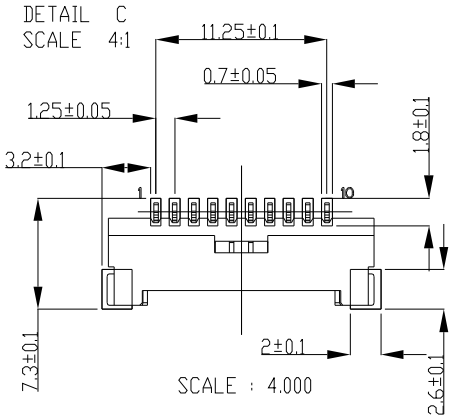


MOLEX 528520870 / (25-D014918)
SCALE : 4.000



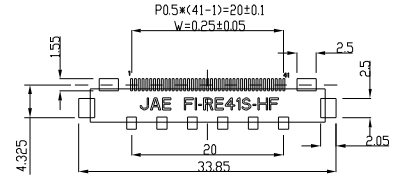
JAE FI-RE51S-HF
SCALE 2:1





SCALE : 4.000

LM123S010HTX3(UNICORN)



JAE FI-RE41S-HF
SCALE 2:1

NOTES:
1. THICKNESS : 1.0mm±0.1mm.
2. COMPONENT HEIGHT LIMITATION :
   FRONT SIDE is 4mm MAX ,
   BACK SIDE is 0mm MAX ,
   UNLESS OTHERWISE INDECATED.
3. GENERAL TOLERANCE IS 0.2mm.
4. ALL FILLET RADIUS IS 2.0mm.
5. " * " MARKS THE CRITICAL DIMENSION.
6. " Ⓟ " MARKS THE CPK DIMENSION.
7. " ▨ " : GND.
8. " ▩ " : NO COMPONENT AREA
9. " ▩ " : COMPONENT HEIGHT 2.5mm MAX

MARK	DESCRIPTION	DATE	CHANGED BY	APPROVAL BY	ECR NO.
A	FIRST RELEASE	2010/09/28	ChungYu Han	Davis Wang	

CHI MEI OPTOELECTRONICS CORP. 奇美電子股份有限公司

APPROVED: Davis Wang		DWG NO: V546B2604A	
CHECKED: Hans Liu		DATE: 2010/09/28	
DESINGER: ChungYu Han		PART NO: 35-D055997	
DRAWER: ChungYu Han	REV.: A	UNIT:	SCALE: / SHEET:
TITLE: assy_pcb_ctrl_V546H1-LS1		MM	1:1 / 1/1