



V2462/V2464

Preliminary

LINEAR INTEGRATED CIRCUIT

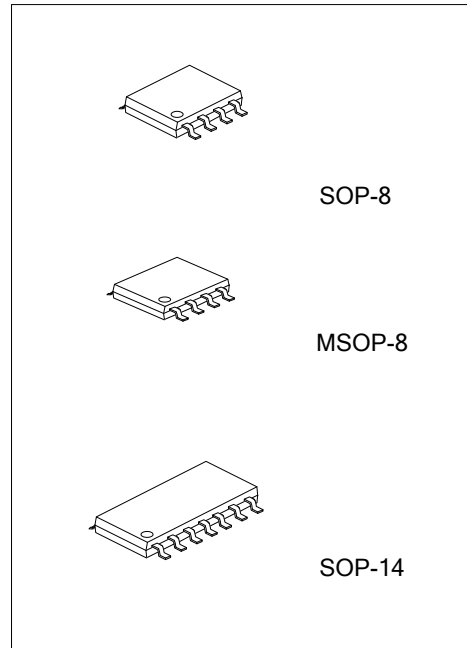
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

DESCRIPTION

The UTC **V2462/2464** are dual/quad low-power rail-to-rail input/output op amplifiers with low supply current (500uA/op) and low voltage (2.7-6V), that can be designed into a wide range of applications.

The UTC **V2462/2464** have a guaranteed 1.6 V/μs slew rate and low supply current. rail-to-rail output and high output current make the I_{CS} ideal for buffering analog-to-digital converters. And the input common-mode voltage range including ground and V_{DD}. Besides, they are also able to driving large capacitive loads.

Good ac performance can be provided because of 6.4MHz of bandwidth and 1.6 V/μs of slew rate. Furthermore, low input noise voltage (11nV/√Hz) and low input offset voltage (100μV) make good DC performance.

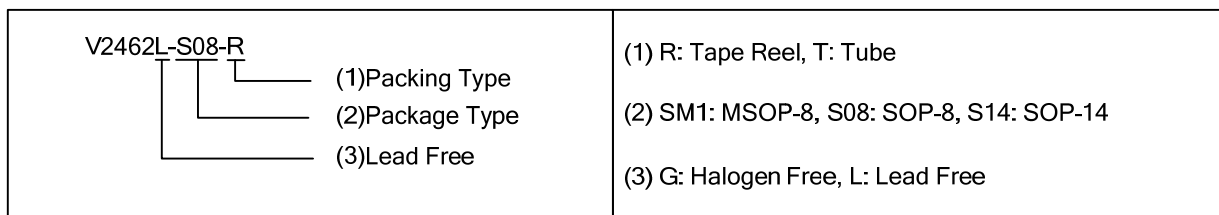


FEATURES

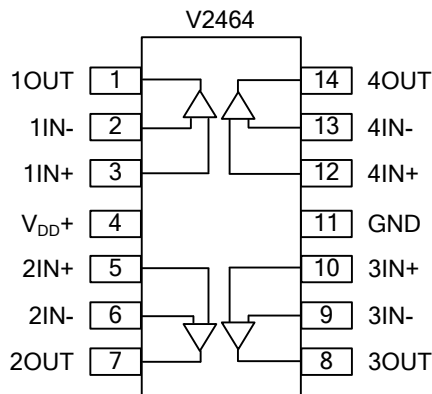
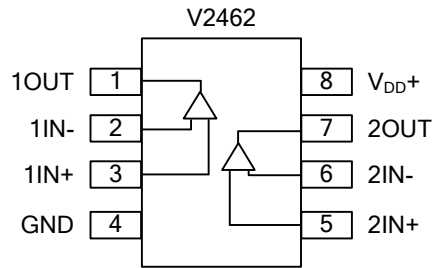
- * Rail-to-Rail Output Swing
- * Gain Bandwidth Product 6.4 MHz
- * ±80mA Output Drive Capability
- * Supply Current 500μA/channel
- * Input Offset Voltage 100μV
- * Input Noise Voltage 11nV/√Hz
- * Slew Rate 1.6V/μs
- * Universal Operational Amplifier EVM
- * Available in Q-Temp Automotive
- * HighRel Automotive Applications
- Configuration Control/Print Support
- Qualification to Automotive Standards

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
V2462L-S08-R	V2462G-S08-R	SOP-8	Tape Reel
V2462L-S08-T	V2462G-S08-T	SOP-8	Tube
V2462L-SM1-R	V2462G-SM1-R	MSOP-8	Tape Reel
V2462L-SM1-T	V2462G-SM1-T	MSOP-8	Tube
V2464L-S14-R	V2464G-S14-R	SOP-14	Tape Reel
V2464L-S14-T	V2464G-S14-T	SOP-14	Tube



■ PIN CONFIGURATION



■ PIN DESCRIPTION

UTC V2462:

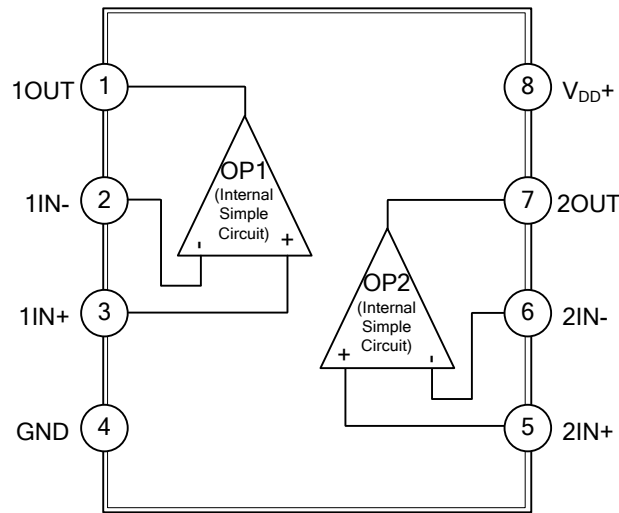
PIN NO.	PIN NAME	DESCRIPTION
1	1OUT	Output terminal of CH1
2	1IN-	Negative input terminal of CH1
3	1IN+	Positive input terminal of CH1
4	GND	Ground
5	2IN+	Positive input terminal of CH2
6	2IN-	Negative input terminal of CH2
7	2OUT	Output terminal of CH2
8	V _{DD} +	Supply voltage terminal

UTC V2464:

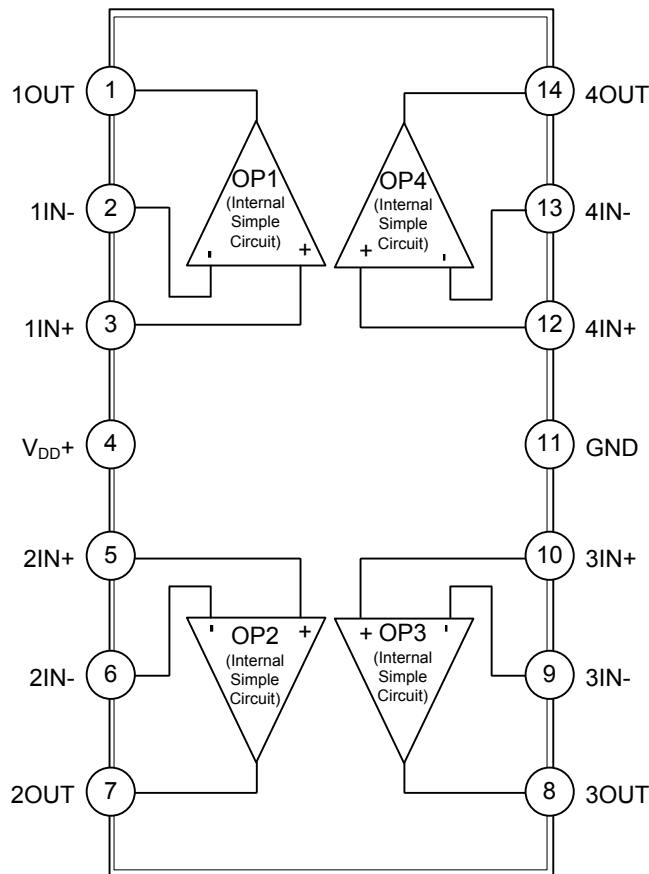
PIN NO.	PIN NAME	DESCRIPTION
1	1OUT	Output terminal of CH1
2	1IN-	Negative input terminal of CH1
3	1IN+	Positive input terminal of CH1
4	V _{DD} +	Supply voltage terminal
5	2IN+	Positive input terminal of CH2
6	2IN-	Negative input terminal of CH2
7	2OUT	Output terminal of CH2
8	3OUT	Output terminal of CH3
9	3IN-	Negative input terminal of CH3
10	3IN+	Positive input terminal of CH3
11	GND	Ground
12	4IN+	Positive input terminal of CH4
13	4IN-	Negative input terminal of CH4
14	4OUT	Output terminal of CH4

■ BLOCK DIAGRAM

V2462

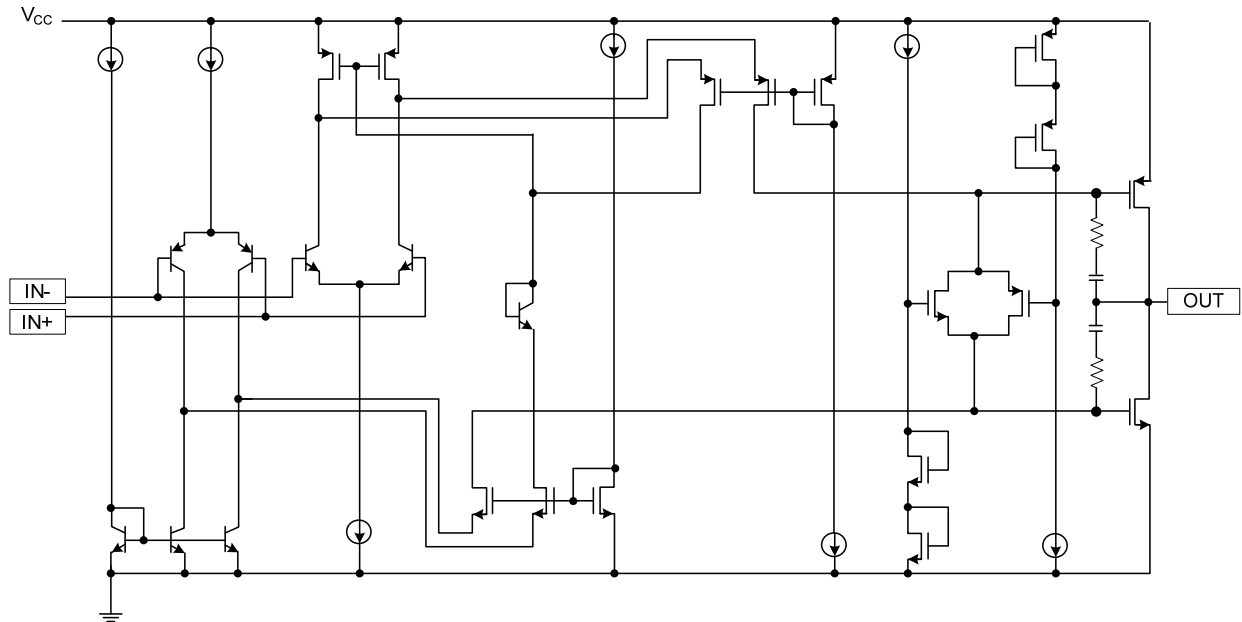


V2464



■ BLOCK DIAGRAM(Cont.)

Internal simple circuit (one channel):



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage (Note 1)		V _{DD}	6	V
Differential Input Voltage		V _{ID}	-0.2~V _{DD} +0.2	V
Output Current		I _O	±175	mA
Power Dissipation	T _A ≤ 25 °C	SOP-8/MSOP-8	710	mW
		SOP-14	1022	
	T _A < 125 °C	SOP-8/MSOP-8	142	
		SOP-14	204.4	
Operating Free-Air Temperature		T _A	-40~125	°C
Junction Temperature		T _J	150	°C
Storage Temperature		T _{STG}	-60~150	°C

Notes: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

1. All voltage values, except differential voltages, are with respect to GND.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8/MSOP-8	θ _{JA}	176	°C/W
	SOP-14		122.6	°C/W
Junction to Case	SOP-8/MSOP-8	θ _{JC}	38.3	°C/W
	SOP-14		26.9	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage	Single supply	V _{DD}	2.7 ~ 6	V
	Split supply		±1.35 ~ ±3	V
Common-Mode Input Voltage		V _{ICR}	0 ~ V _{DD}	V
Operating Free-Air Temperature		T _A	-40 ~ 125	°C

Note: 1. Relative to voltage on the GND terminal of the device.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

V_{DD}=3V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input Offset Voltage	V _{IO}	V _{DD} =3V, V _{IC} =1.5V, V _O =1.5V, R _S =50Ω	T _A =25°C		500	2000	μV
			(Note 1)			2200	
Input Offset Current	I _{IO}	V _{DD} =3V, V _{IC} =1.5V, V _O =1.5V, R _S =50Ω	T _A =25°C		2.8	7	nA
			(Note 1)			75	
Input Bias Current	I _{IB}	V _{DD} =3V, V _{IC} =1.5V, V _O =1.5V, R _S =50Ω	T _A =25°C		4.4	14	nA
			(Note 1)			75	
High-Level Output Voltage	V _{OH}	I _{OH} = -2.5mA	T _A =25°C		2.9		V
			(Note 1)	2.8			
		I _{OH} =-10mA	T _A =25°C		2.7		
			(Note 1)	2.5			
Low-Level Output Voltage	V _{OL}	V _{IC} =1.5V, I _{OL} =2.5mA	T _A =25°C		0.1		V
			(Note 1)			0.2	
		V _{IC} =1.5V, I _{OL} =10mA	T _A =25°C		0.3		
			(Note 1)			0.5	
Short-Circuit Output Current	I _{OS}	Sourcing	T _A =25°C		50		mA
			(Note 1)	20			
		Sinking	T _A =25°C		40		
			(Note 1)	20			

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output Current	I_O	Measured 1V form rail, $T_A=25^\circ\text{C}$		± 40		mA	
Large-Signal Differential Voltage Amplification	A_{VD}	$R_L=10\text{k}\Omega$, $V_{O(PP)}=1\text{V}$	$T_A=25^\circ\text{C}$	90	105	dB	
			(Note 1)	89			
Differential Input Resistance	$r_{i(D)}$	$T_A=25^\circ\text{C}$		10^9		Ω	
Common-Mode Input Capacitance	$C_{i(C)}$	$f=10\text{kHz}$, $T_A=25^\circ\text{C}$		7		pF	
Closed-Loop Output Impedance	Z_O	$f=100\text{kHz}$, $A_V=10$, $T_A=25^\circ\text{C}$		33		Ω	
Common-Mode Rejection Ratio	CMRR	$V_{ICR}=0\sim 3\text{V}$, $R_S=50\Omega$	$T_A=25^\circ\text{C}$	66	80	dB	
			(Note 1)	60			
Supply Voltage Rejection Ratio ($\Delta V_{DD}/\Delta V_{IO}$)	k_{SVR}	$V_{DD}=2.7\sim 6\text{V}$, $V_{IC}=V_{DD}/2$, No load	$T_A=25^\circ\text{C}$	80	85	dB	
			(Note 1)	75			
			$T_A=25^\circ\text{C}$	85	95		
Supply Current (Per Channels)	I_{DD}	$V_O=1.5\text{V}$, No load	$T_A=25^\circ\text{C}$		0.5	0.575	mA
			(Note 1)			0.9	

Note: 1. $T_A = -40^\circ\text{C}\sim 125^\circ\text{C}$.

$V_{DD}=5\text{V}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input Offset Voltage	V_{IO}	$V_{DD}=5\text{V}$, $V_{IC}=2.5\text{V}$, $V_O=2.5\text{V}$, $R_S=50\Omega$	$T_A=25^\circ\text{C}$		500	2000	μV
			(Note 1)			2200	
Input Offset Current	I_{IO}	$V_{DD}=5\text{V}$, $V_{IC}=2.5\text{V}$, $V_O=2.5\text{V}$, $R_S=50\Omega$	$T_A=25^\circ\text{C}$		0.3	7	nA
			(Note 1)			60	
Input Bias Current	I_{IB}	$T_A=25^\circ\text{C}$ (Note 1)			1.3	14	nA
						60	
High-Level Output Voltage	V_{OH}	$I_{OH}=-2.5\text{mA}$ $I_{OH}=-10\text{mA}$	$T_A=25^\circ\text{C}$		4.9	V	
			(Note 1)	4.8			
Low-Level Output Voltage	V_{OL}	$V_{IC}=2.5\text{V}$, $I_{OL}=2.5\text{mA}$ $V_{IC}=2.5\text{V}$, $I_{OL}=10\text{mA}$	$T_A=25^\circ\text{C}$		0.1	V	
			(Note 1)		0.2		
Short-Circuit Output Current	I_{OS}	Sourcing Sinking	$T_A=25^\circ\text{C}$		145	mA	
			(Note 1)	60	100		
Output Current	I_O	Measured 1V form rail			± 48	mA	
Large-Signal Differential Voltage Amplification	A_{VD}	$V_{IC}=2.5\text{V}$, $R_L=10\text{k}\Omega$, $V_O=1\sim 4\text{V}$	$T_A=25^\circ\text{C}$	92	109	dB	
			(Note 1)	90			
Differential Input Resistance	$r_{i(D)}$	$T_A=25^\circ\text{C}$		10^9		Ω	
Common-Mode Input Capacitance	$C_{i(C)}$	$f=10\text{kHz}$, $T_A=25^\circ\text{C}$		7		pF	
Closed-Loop Output Impedance	Z_O	$f=100\text{kHz}$, $A_V=10$, $T_A=25^\circ\text{C}$		29		Ω	
Common-Mode Rejection Ratio	CMRR	$V_{ICR}=0\sim 5\text{V}$, $R_S=50\Omega$	$T_A=25^\circ\text{C}$	71	85	dB	
			(Note 1)	60			
Supply Voltage Rejection Ratio ($\Delta V_{DD}/\Delta V_{IO}$)	k_{SVR}	$V_{DD}=2.7\sim 6\text{V}$, $V_{IC}=V_{DD}/2$, No load	$T_A=25^\circ\text{C}$	80	85	dB	
			(Note 1)	75			
			$T_A=25^\circ\text{C}$	85	95		
Supply Current (Per Channels)	I_{DD}	$V_O=2.5\text{V}$, No load	$T_A=25^\circ\text{C}$		0.55	0.65	mA
			(Note 1)			1	

Note: 1. $T_A = -40^\circ\text{C}\sim 125^\circ\text{C}$.

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

V_{DD}=3V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew Rate at Unity Gain	SR	V _{O(PP)} =0.8V, R _L =10kΩ, C _L =160pF, T _A =25°C (Note 1)	0.9	1.6		V/μs
Equivalent Input Noise Voltage	V _N	f=100Hz		16		nV/√Hz
		f=1kHz		11		
Equivalent Input Noise Current	I _N	f=1kHz		0.13		pA/√Hz
Total Harmonic Distortion Plus Noise	THD+N	V _{O(PP)} =2V, R _L =10kΩ, f=1kHz		0.006		%
		A _V =1		0.02		
		A _V =10		0.08		
		A _V =100				
Gain-Bandwidth Product		f=10 kHz, C _L =160pF, R _L =10kΩ		5.2		MHz
Setting Time	t _s	V _{(STEP)PP} =2V, R _L =10kΩ, A _V = -1, C _L =10pF	0.1%	1.47		μs
		V _{(STEP)PP} =2V, R _L =10kΩ, A _V = -1, C _L =56pF	0.1%	1.78		
		V _{(STEP)PP} =2V, R _L =10kΩ, A _V = -1, C _L =10pF	0.1%	1.77		
		V _{(STEP)PP} =2V, R _L =10kΩ, A _V = -1, C _L =56pF	0.1%	1.98		
Phase Margin at Unity Gain	Φ _M	R _L =10kΩ, C _L =160pF		44°		
Gain Margin				7		dB

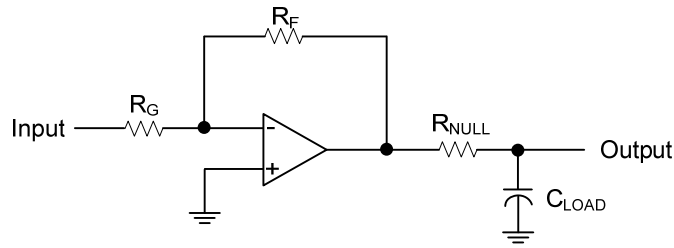
Note: 1. T_A=-40°C~125°C.

V_{DD}=5V

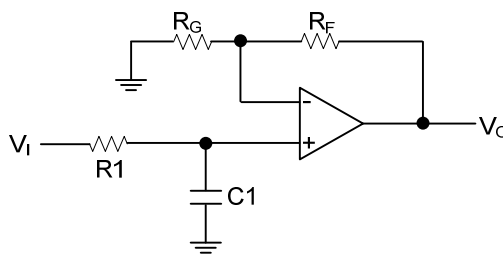
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew Rate at Unity Gain	SR	V _{O(PP)} =2V, C _L =160pF, R _L =10 kΩ, T _A =25°C (Note 1)	0.9	1.6		V/μs
Equivalent Input Noise Voltage	V _N	f=100Hz		14		nV/√Hz
		f=1kHz		11		
Equivalent Input Noise Current	I _N	f=1kHz		0.13		pA/√Hz
Total Harmonic Distortion Plus Noise	THD+N	V _{O(PP)} =4V, R _L =10kΩ, f=1kHz		0.004		%
		A _V =1		0.01		
		A _V =10		0.04		
		A _V =100				
Gain-Bandwidth Product		f=10 kHz, C _L =160pF, R _L =10kΩ		6.4		MHz
Setting Time	t _s	V _{(STEP)PP} =2V, R _L =10kΩ, A _V = -1, C _L =10pF	0.1%	1.53		μs
		V _{(STEP)PP} =2V, R _L =10kΩ, A _V = -1, C _L =56pF	0.1%	1.83		
		V _{(STEP)PP} =2V, R _L =10kΩ, A _V = -1, C _L =10pF	0.1%	3.13		
		V _{(STEP)PP} =2V, R _L =10kΩ, A _V = -1, C _L =56pF	0.1%	3.33		
Phase Margin at Unity Gain	Φ _M	R _L =10kΩ, C _L =160pF		45°		
Gain Margin				7		dB

Note: 1. T_A= -40°C~125°C.

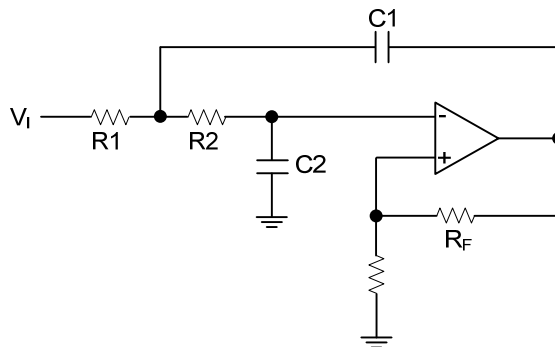
■ TYPICAL APPLICATION CIRCUIT



Driving a capacitive Load



Single-Pole Low-Pass Filter



2-Pole Low-Pass Sallen-Key Filter

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