TFT LCD Approval Specification

MODEL NO.: V315H1-LH3

Customer: _____

Approved by:_____

Note:

Approved By	TV Product Marketing & Management Div
	Chao-Chun Chung

Reviewed By	QA Dept.	Product Development Div.
	Hsin-Nan Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	Josh Chi	Cindy Yang

- CONTENTS -

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Jul. 14,09'	All	All	Approval Specification was first issued.
Ver 2.1	Jan. 11,10'	34-36	11	3D drawing update
		4	1	Updated OVERVIEW description
		30	8	Updated Manufactured Date definition

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315H1- LH3 s a 31.5" TFT Liquid Crystal Display module with 4U-type CCFL Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display **1.07G colors (10-bit/color)**. The inverter module for backlight is built-in.

1.2 FEATURES

-High brightness (450 nits)

- Ultra-high contrast ratio (4000:1)
- Fast response time (gray to gray average 4.5 ms)
- High color saturation NTSC 72%
- Ultra wide viewing angle : 176(H)/176(V) (CR≥20) with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Color reproduction (nature color)
- Low color shift function

1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	698.4(H) x 392.85 (V)	mm	
Bezel Opening Area	703.8 (H) x 398.4 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.12125 (H) x 0.36375 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	1.07G	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Glare coating,Hard coating (3H)	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	759	760	761	mm	
	Vertical(V)	449	450	451	mm	
	Depth(D)	31.5	32.5	33.5	mm	To Rear
	Depth(D)	53.2	54.2	55.2	mm	To Inverter Cover
	Depth(D)	46.5	47.5	48.5	mm	To PCB cover
Weight		-	5760	-	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

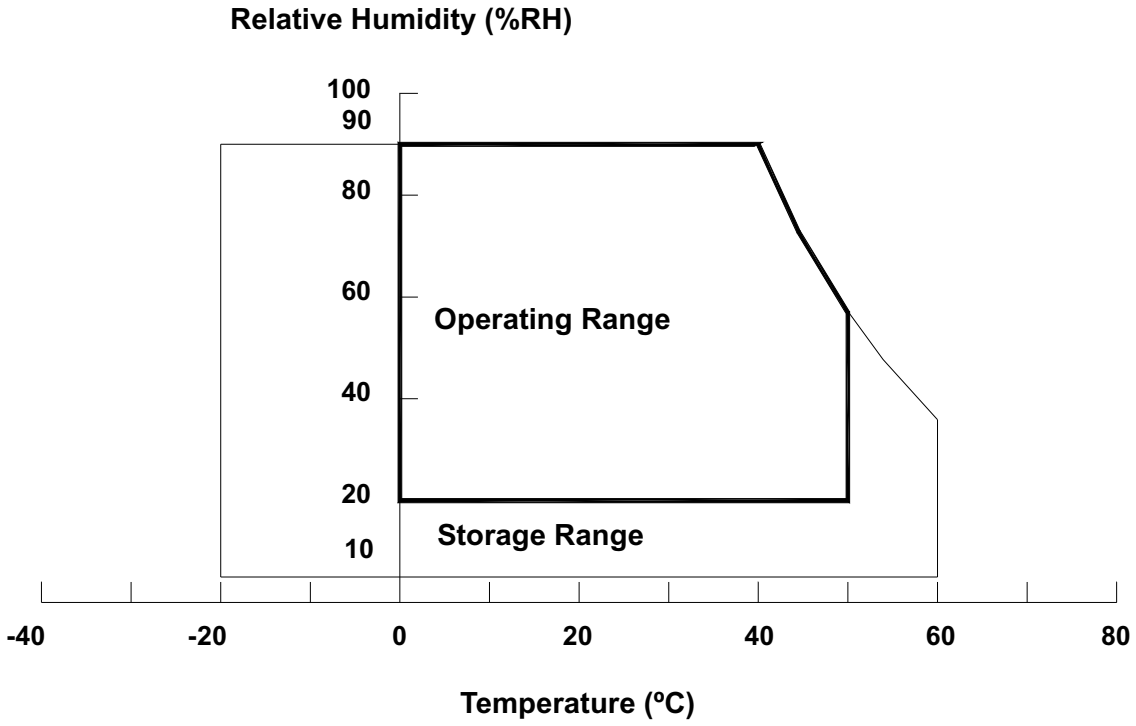
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 Package storage

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

(b)The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.5	V	
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes Backlight On/Off Control, I_PWM Control, E_PWM Control and ERR signal for inverter status output.

3. ELECTRICAL CHARACTERISTICS

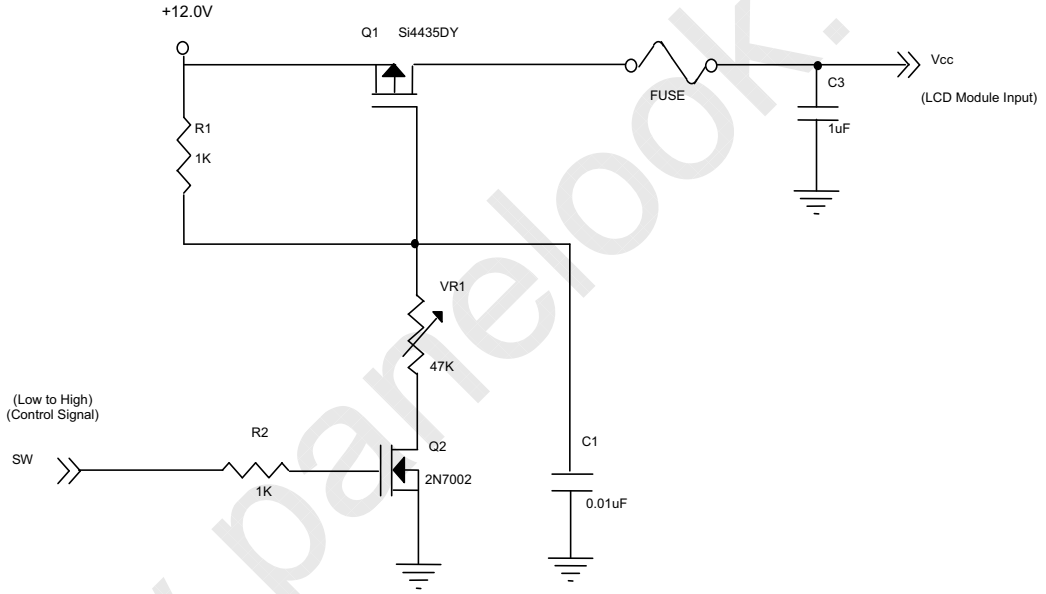
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

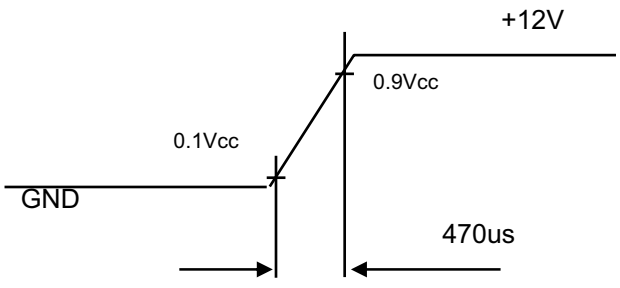
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	350	mV	
Rush Current		I_{RUSH}	-	-	4.8	A	(2)
Power Supply Current	White	I_{CC}	-	2	2.6	A	(3)
	Black		-	1.6		A	
	Vertical Stripe		-	2.1		A	
LVDS interface	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc =12V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

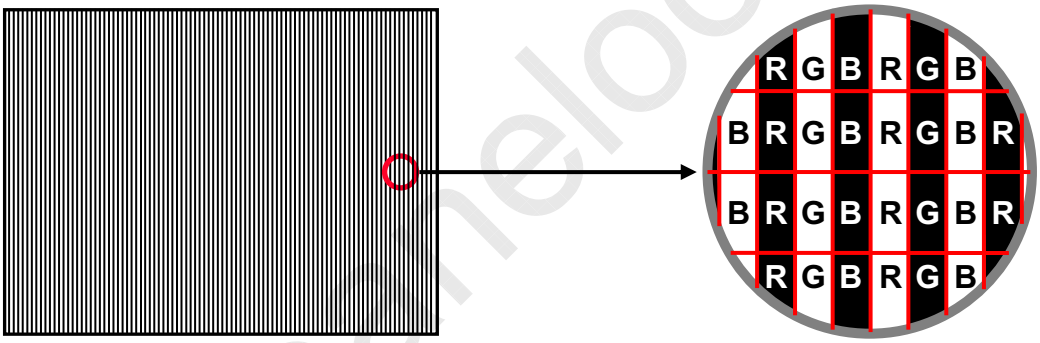
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT INVERTER UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	1470	-	V_{RMS}	I_L = 12.3mA
Lamp Current	I_L	11.8	12.3	12.8	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	2760	V_{RMS}	(2), Ta = 0 ºC
		-	-	2300	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_O	40	-	80	KHz	(3)
Lamp Life Time	L_{BL}	50,000		-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	79	81	W	(5),(6), I_L = 12.3mA
Input Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Input Current	I_{BL}	-	3.29	3.38	A	Non Dimming
Input Ripple Noise	-	-	-	912	mV_{P-P}	V_{BL}=22.8V
Oscillating Frequency	F_W	60	63	66	kHz	(3)
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

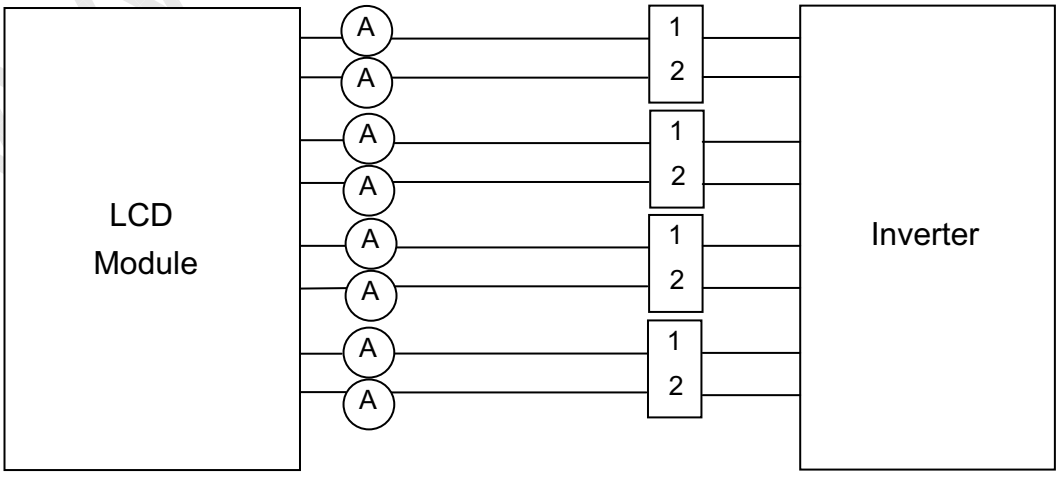
Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2 ℃ and I_L = 11.8~ 12.8mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 31.5" backlight unit under input voltage 24V, average lamp current 12.6 mA and lighting 30 minutes later.



3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	—	2.85	3.0	3.15	V	Maximum duty ratio
	MIN			—	0	—	V	Minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	—	2.0	—	5.0	V	Duty on
	LO			0	—	0.8	V	Duty off
Error Signal		ERR	—	—	—	—	V	
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V_{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
PWM Delay Time		T_{PWM}	—	100		—	ms	
BLON Delay Time		T_{on}	—	300	—	—	ms	
		T_{on1}	—	300	—	—	ms	
BLON Off Time		T_{off}	—	300	—	—	ms	

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

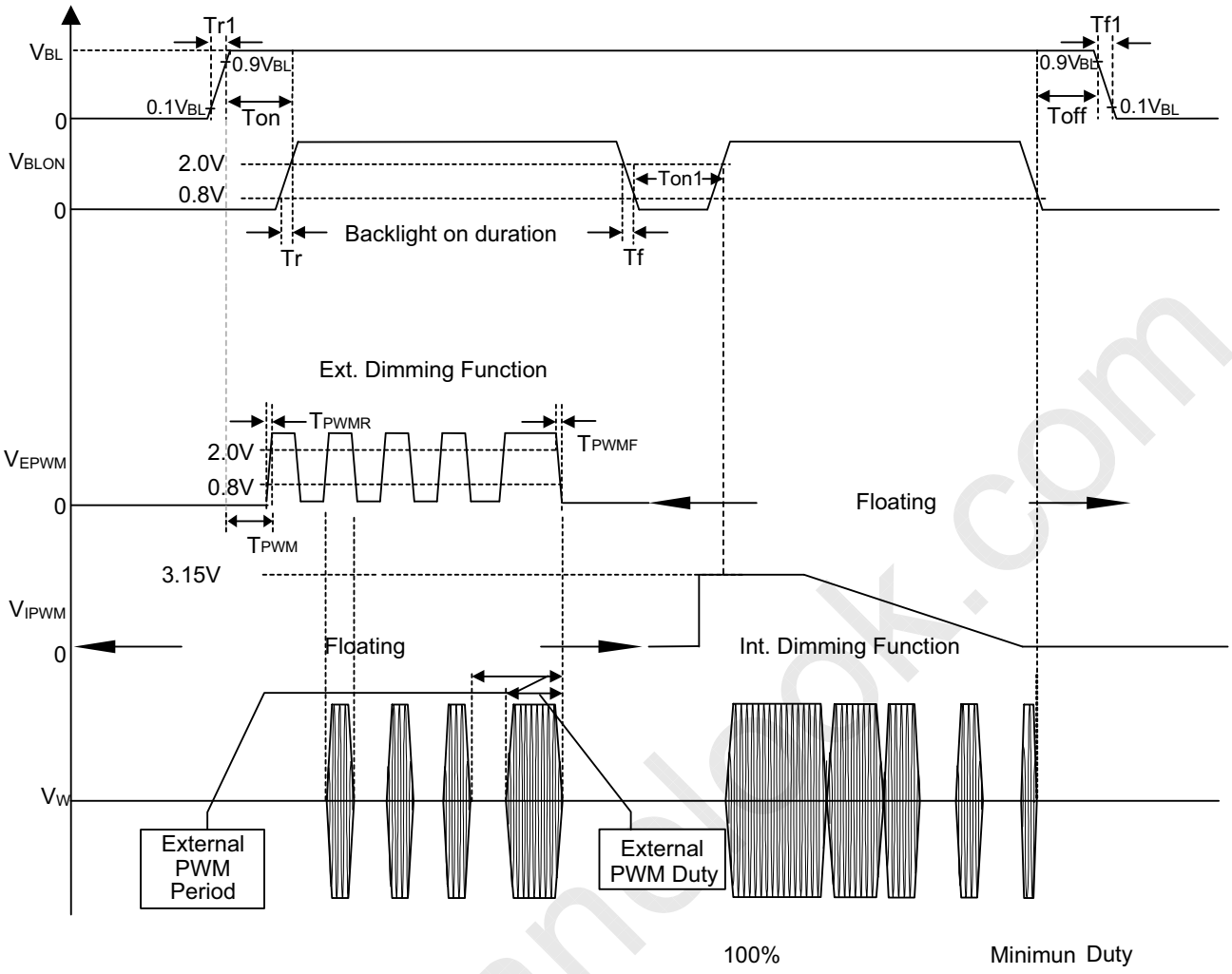
Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

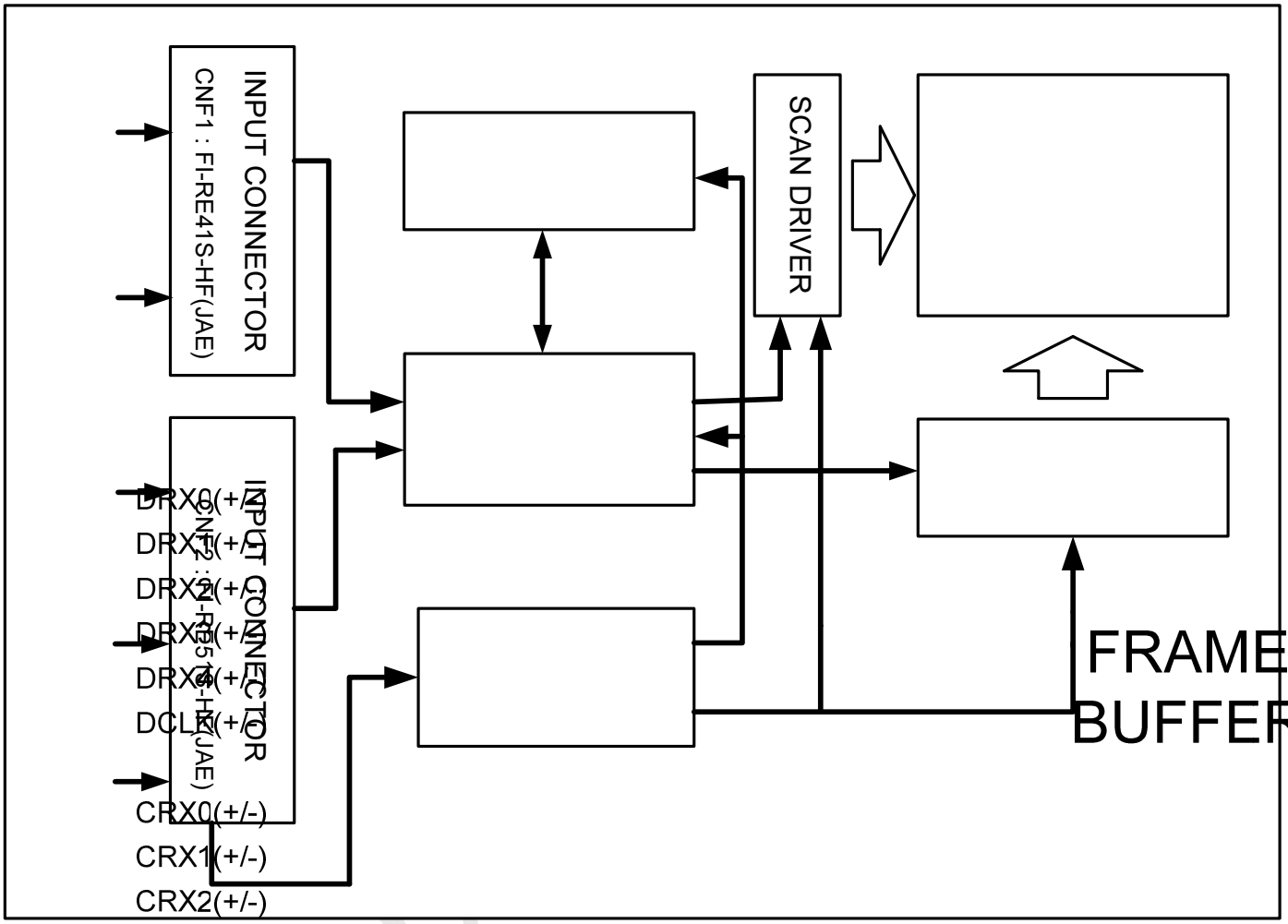
Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When inverter protective function is triggered, ERR will output open collector status; In normal operation, the signal of ERR will output a low level voltage.



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF2 Connector Pin Assignment (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	(1)
11	GND	Ground	
12	ARX0-	First pixel Negative LVDS differential data input. Channel 0	
13	ARX0+	First pixel Positive LVDS differential data input. Channel 0	
14	ARX1-	First pixel Negative LVDS differential data input. Channel 1	
15	ARX1+	First pixel Positive LVDS differential data input. Channel 1	
16	ARX2-	First pixel Negative LVDS differential data input. Channel 2	
17	ARX2+	First pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ACLK-	First pixel Negative LVDS differential clock input.	
20	ACLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ARX3-	First pixel Negative LVDS differential data input. Channel 3	
23	ARX3+	First pixel Positive LVDS differential data input. Channel 3	
24	ARX4-	First pixel Negative LVDS differential data input. Channel 4	
25	ARX4+	First pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	(1)

28	BRX0-	Second pixel Negative LVDS differential data input. Channel 0	
29	BRX0+	Second pixel Positive LVDS differential data input. Channel 0	
30	BRX1-	Second pixel Negative LVDS differential data input. Channel 1	
31	BRX1+	Second pixel Positive LVDS differential data input. Channel 1	
32	BRX2-	Second pixel Negative LVDS differential data input. Channel 2	
33	BRX2+	Second pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	BCLK-	Second pixel Negative LVDS differential clock input.	
36	BCLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	BRX3-	Second pixel Negative LVDS differential data input. Channel 3	
39	BRX3+	Second pixel Positive LVDS differential data input. Channel 3	
40	BRX4-	Second pixel Negative LVDS differential data input. Channel 4	
41	BRX4+	Second pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF1 Connector Pin Assignment (FI-RE41S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)

6	N.C.	No Connection	(1)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	(1)
9	GND	Ground	
10	CRX0-	Third pixel Negative LVDS differential data input. Channel 0	
11	CRX0+	Third pixel Positive LVDS differential data input. Channel 0	
12	CRX1-	Third pixel Negative LVDS differential data input. Channel 1	
13	CRX1+	Third pixel Positive LVDS differential data input. Channel 1	
14	CRX2-	Third pixel Negative LVDS differential data input. Channel 2	
15	CRX2+	Third pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	CCLK-	Third pixel Negative LVDS differential clock input.	
18	CCLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CRX3-	Third pixel Negative LVDS differential data input. Channel 3	
21	CRX3+	Third pixel Positive LVDS differential data input. Channel 3	
22	CRX4-	Third pixel Negative LVDS differential data input. Channel 4	
23	CRX4+	Third pixel Positive LVDS differential data input. Channel 4	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	(1)
26	DRX0-	Fourth pixel Negative LVDS differential data input. Channel 0	
27	DRX0+	Fourth pixel Positive LVDS differential data input. Channel 0	
28	DRX1-	Fourth pixel Negative LVDS differential data input. Channel 1	
29	DRX1+	Fourth pixel Positive LVDS differential data input. Channel 1	
30	DRX2-	Fourth pixel Negative LVDS differential data input. Channel 2	
31	DRX2+	Fourth pixel Positive LVDS differential data input. Channel 2	
32	GND	Ground	
33	DCLK-	Fourth pixel Negative LVDS differential clock input.	
34	DCLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	DRX3-	Fourth pixel Negative LVDS differential data input. Channel 3	

37	DRX3+	Fourth pixel Positive LVDS differential data input. Channel 3	
38	DRX4-	Fourth pixel Negative LVDS differential data input. Channel 4	
39	DRX4+	Fourth pixel Positive LVDS differential data input. Channel 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	(1)

Note (1) Please be reserved to open.

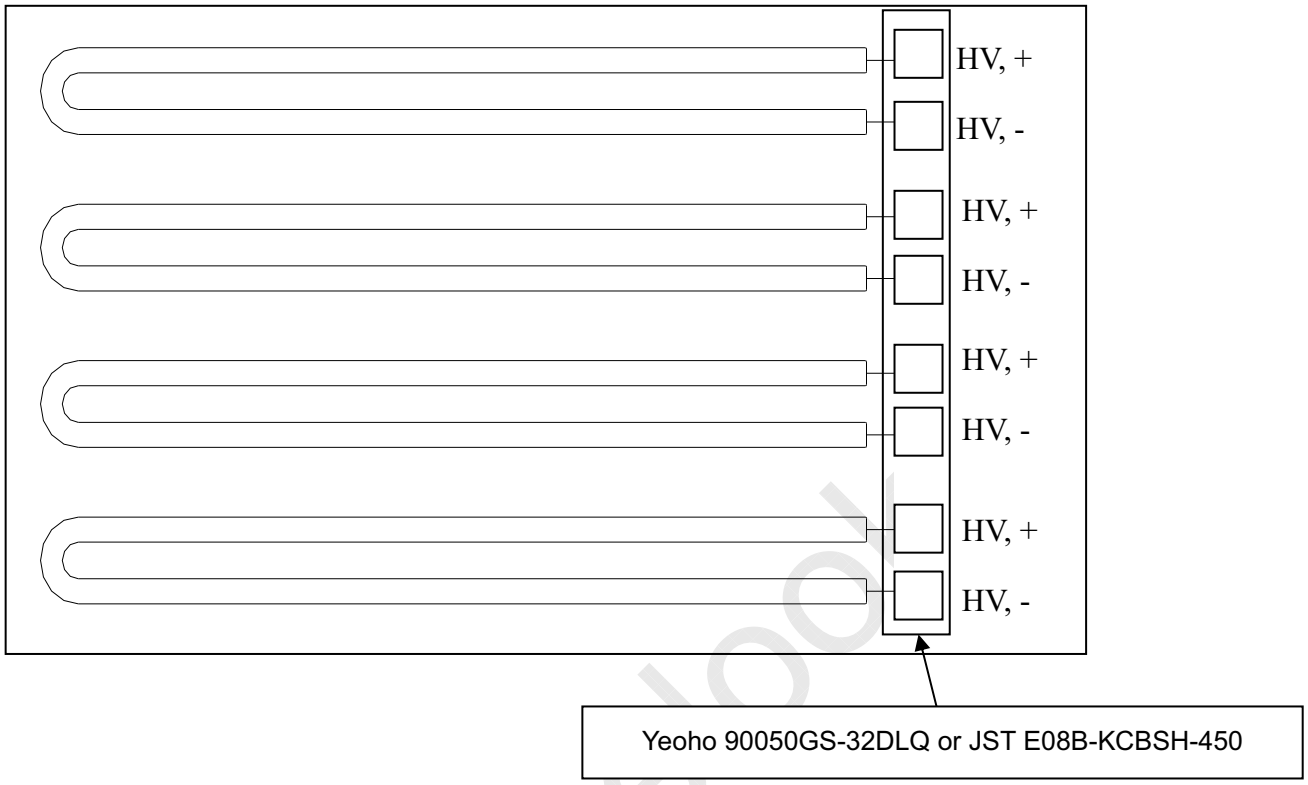
Note (2) Low or Open: VESA Format (Default), High: JEIDA Format.

Note (3) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

5.2 BACKLIGHT UNIT

The backlight interface for high voltage side is Yeoho 90050GS-32DLQ or JST E08B-KCBSH-450



5.3 INVERTER UNIT

CN1(Header): CviLux CI0114M1HR0-LA

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (open collector)
12	BLON	Backlight on/off control
13	I_PWM	Internal PWM control signal
14	E_PWM	External PWM control signal

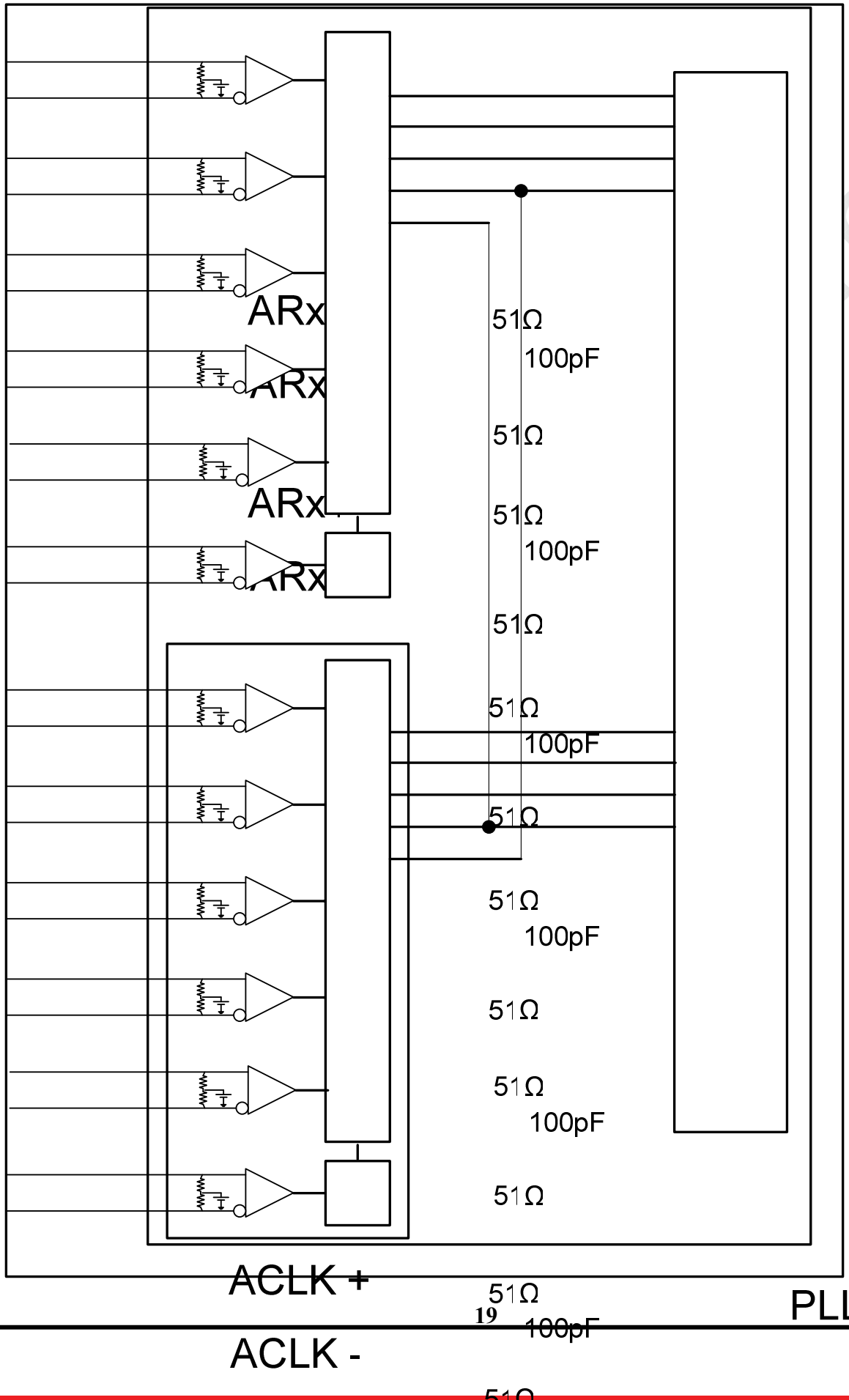
Notice:

#PIN 13: Internal PWM control (Use Pin 13): Pin 14 must open.

#PIN 14: External PWM control (Use Pin 14): Pin 13 must open.

#Pin 13(I_PWM) and Pin 14(E_PWM) can not open in same period.

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data
AG0~AG9: First pixel G data
AB0~AB9: First pixel B data
BR0~BR9: Second pixel R data
BG0~BG9: Second pixel G data
BB0~BB9: Second pixel B data
DE: Data enable signal
DCLK: Data clock signal

The third and fourth pixel are followed the same rules.
CR0~CR9: Third pixel R data
CG0~CG9: Third pixel G data
CB0~CB9: Third pixel B data
DR0~DR9: Fourth pixel R data
DG0~DG9: Fourth pixel G data
DB0~DB9: Fourth pixel B data

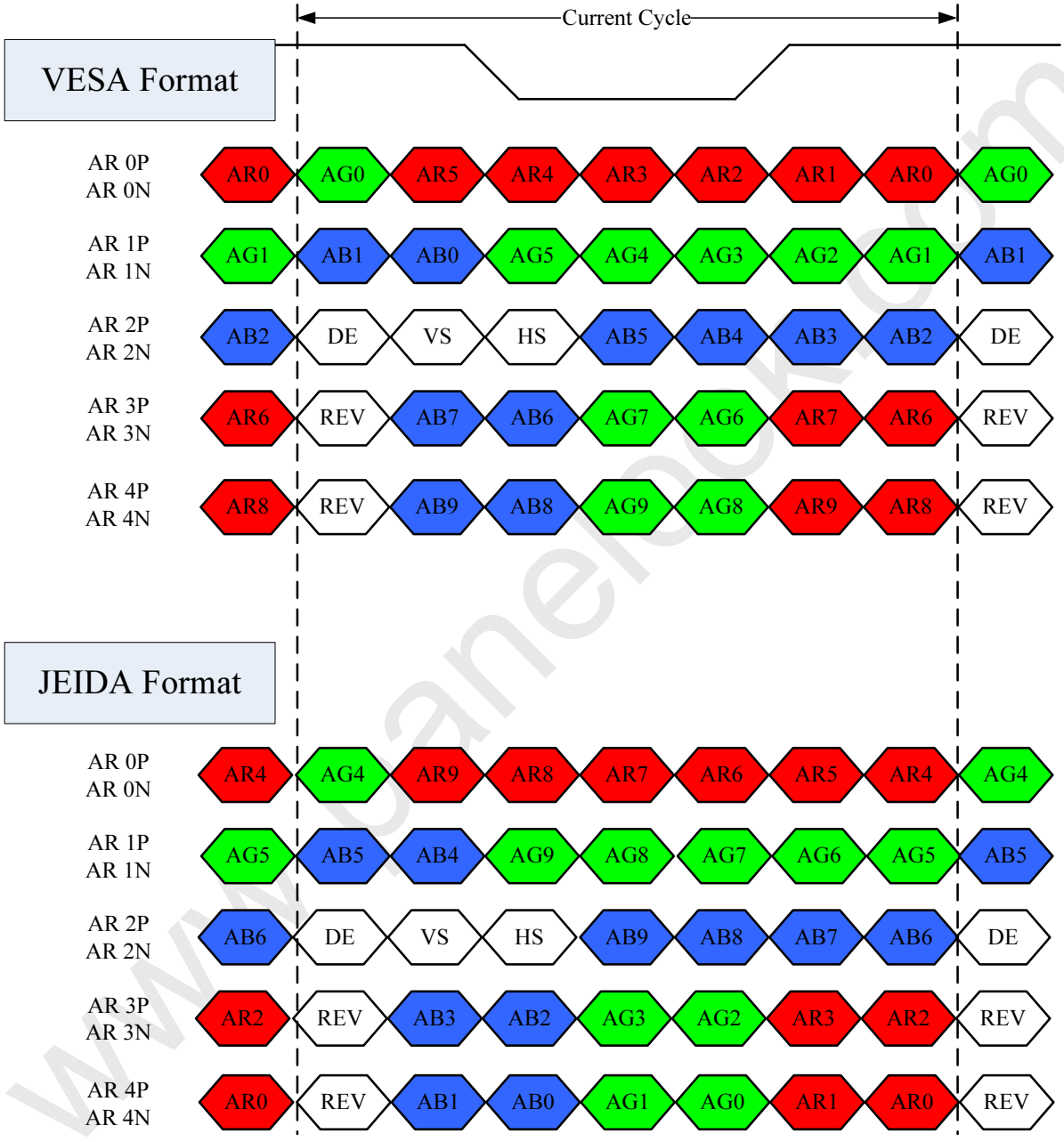
Note (1) A ~ D channel are first, second, third and fourth pixel respectively.
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	;	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:

	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

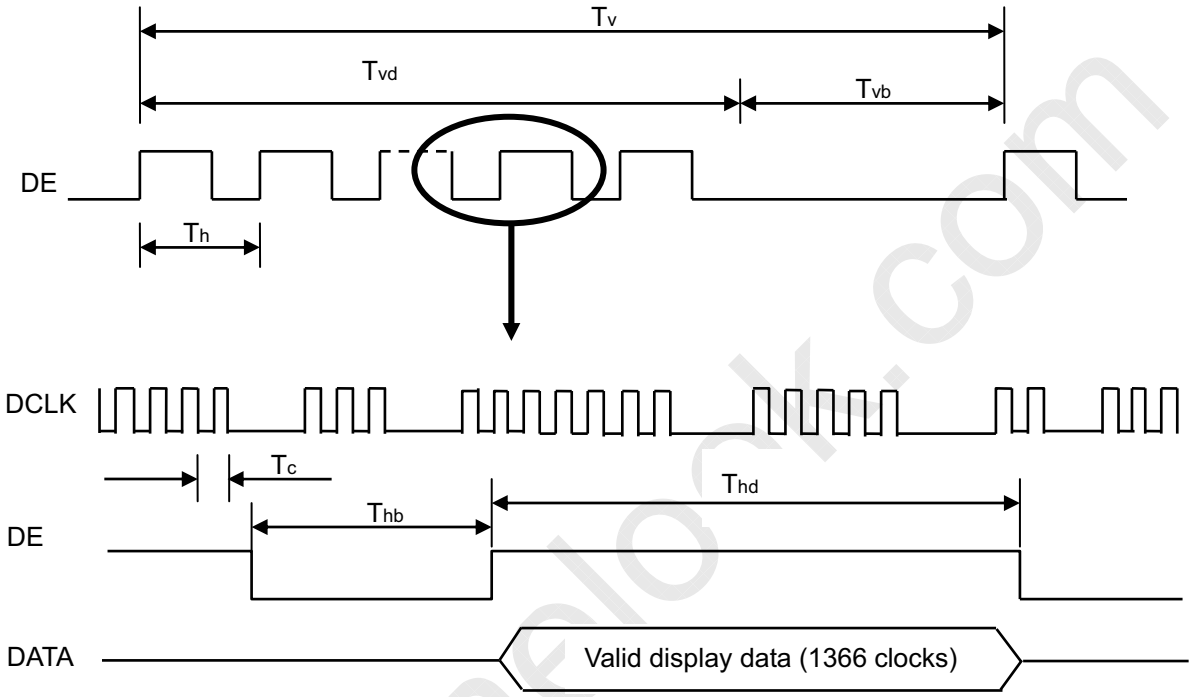
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	80	MHz	(1)
	Input cycle to cycle jitter	Trcl	-	-	200	ps	(1)
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(1)
	Hold Time	Tlvhd	600	-	-	ps	(1)
Vertical Active Display Term	Frame Rate	Fr5		120		Hz	(2)
		Fr6		100		Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	525	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	45	70	95	Tc	-

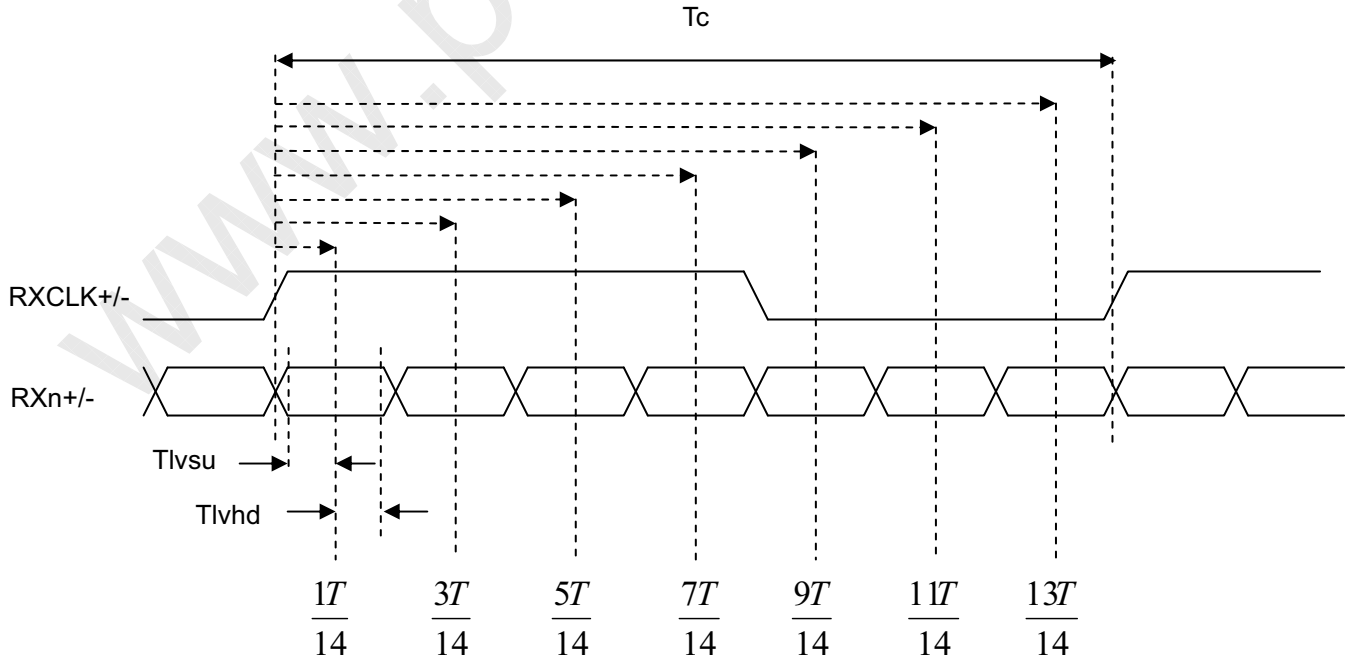
Note (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

(2) Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM



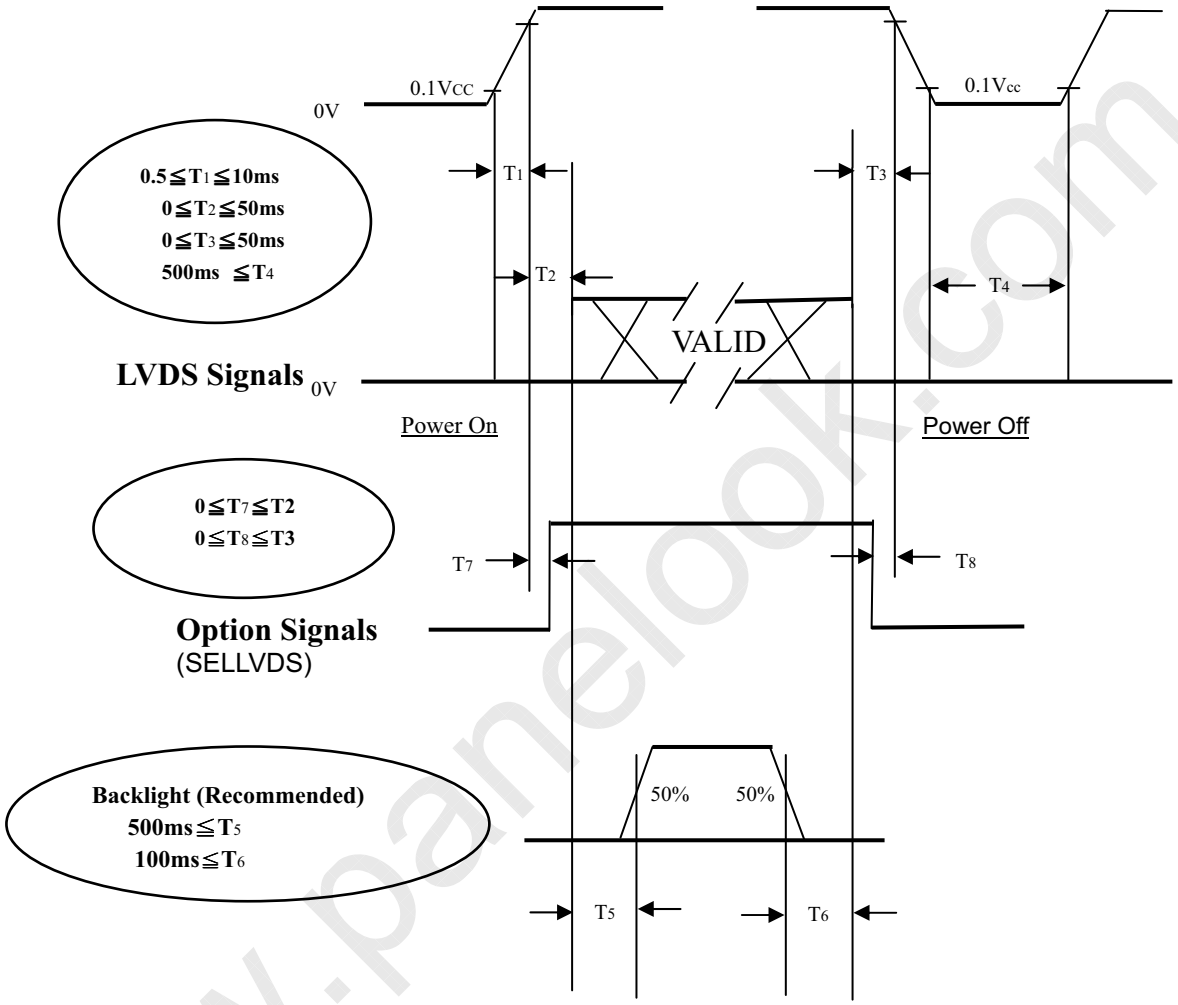
LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1):The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2):Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note(3):In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4):T4 should be measured after the module has been fully discharged between power off and on period.

Note (5): Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	12.3 ± 0.5	mA
Oscillating Frequency (Inverter)	F_W	63±3	KHz
Frame rate	Fr	60	Hz

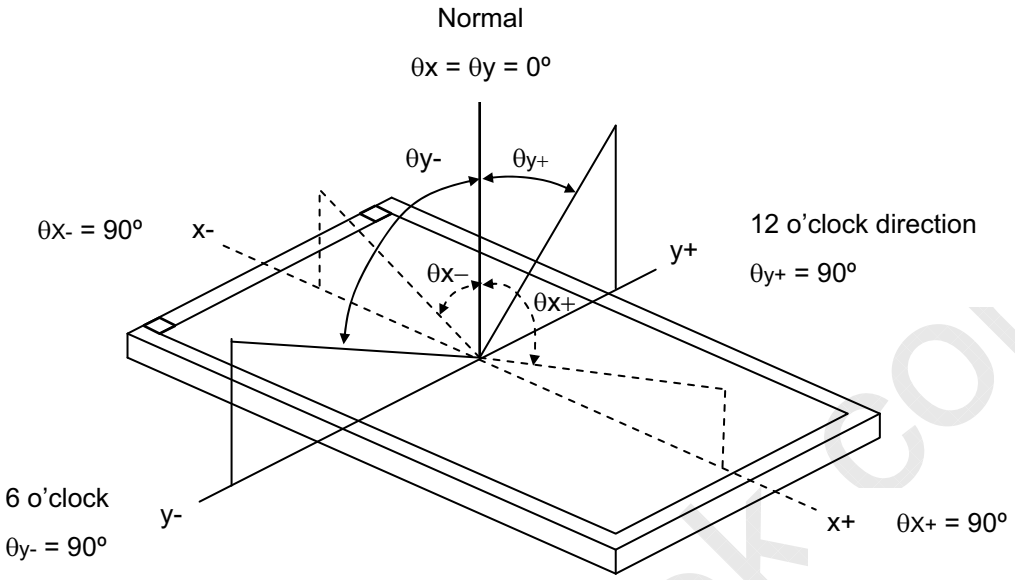
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction	3000	4000		-	(2)
Response Time		Gray to gray average			4.5	9	ms	(3)
Center Luminance of White		L_C		360	450		cd/m^2	(4)
White Variation		δW		-	-	1.3	-	(7)
Cross Talk		CT		-	-	4.0	%	(5)
Color Chromaticity	Red	Rx		Typ -0.03	0.633	Typ +0.03	-	(6)
		Ry			0.322		-	
	Green	Gx			0.288		-	
		Gy			0.603		-	
	Blue	Bx			0.146		-	
		By			0.055		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut	CG		68	72		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	(1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

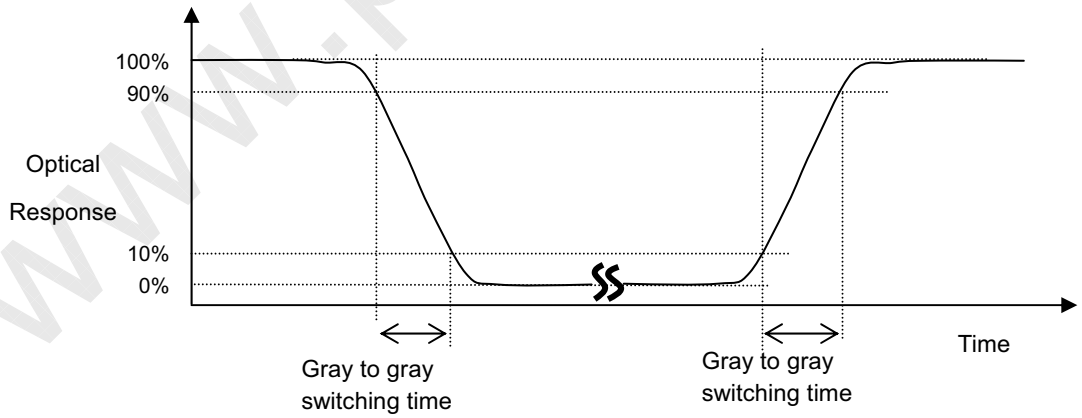
Contrast Ratio (CR) = L1023 / L0

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 255, 511, 767, 1023

Gray to gray average time means the average switching time of gray level 0, 255, 511, 767, 1023 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

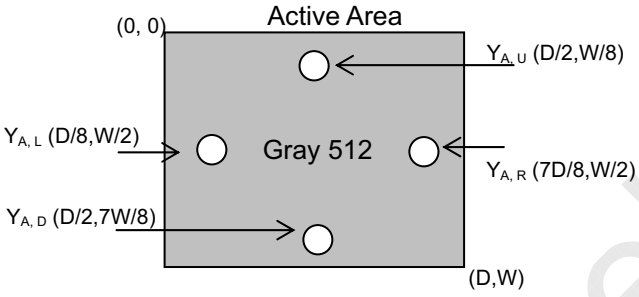
$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

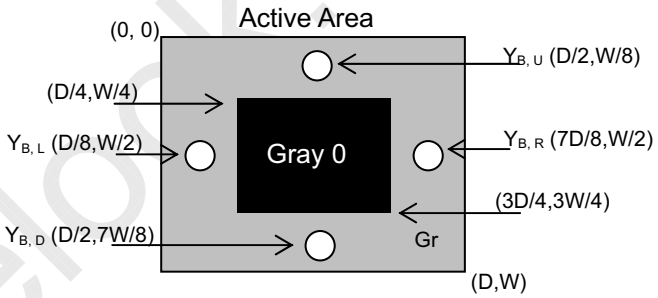
Where:

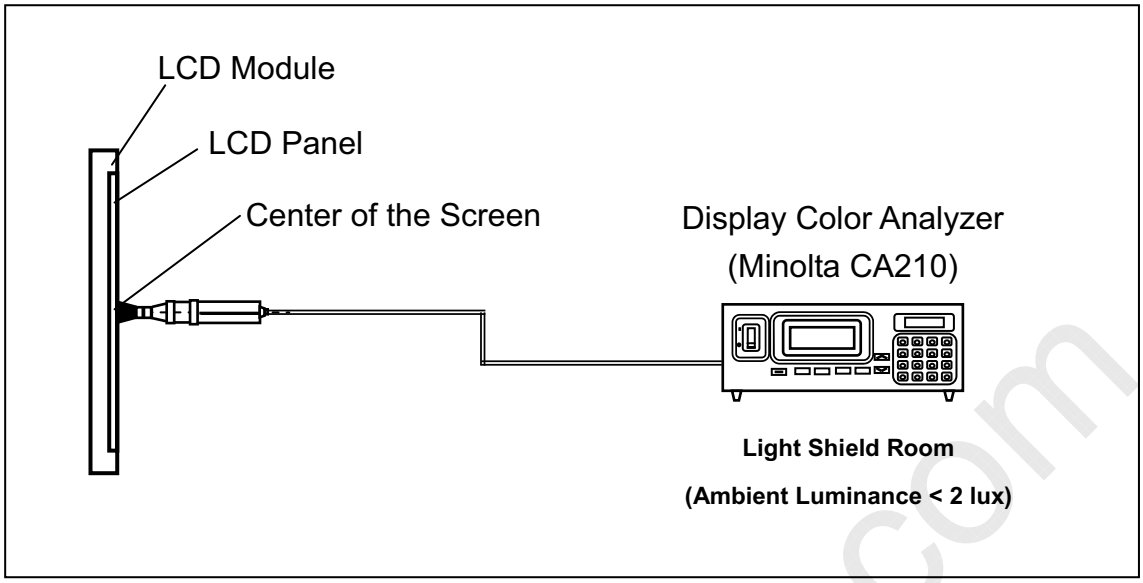
(a)

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



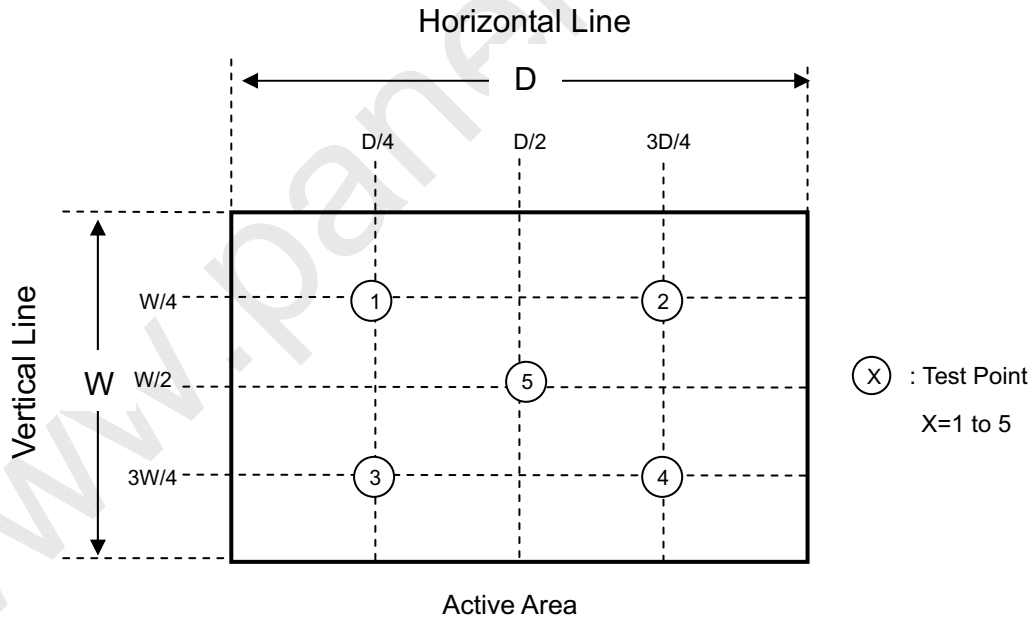




Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

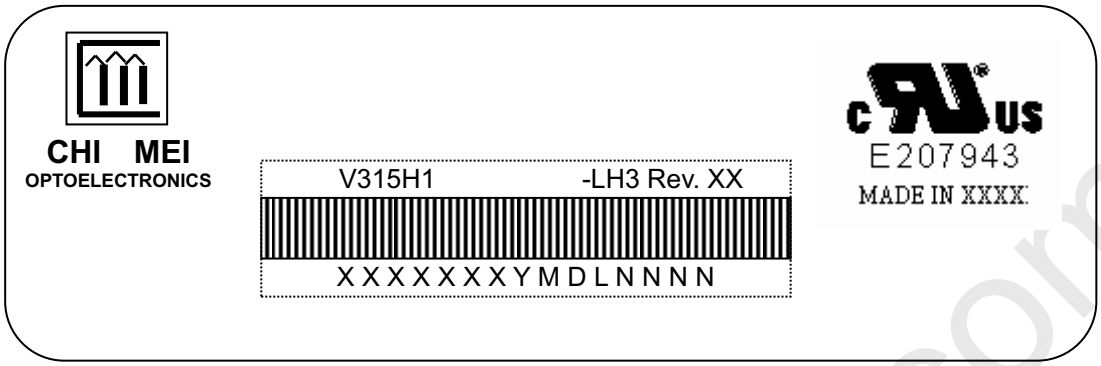
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

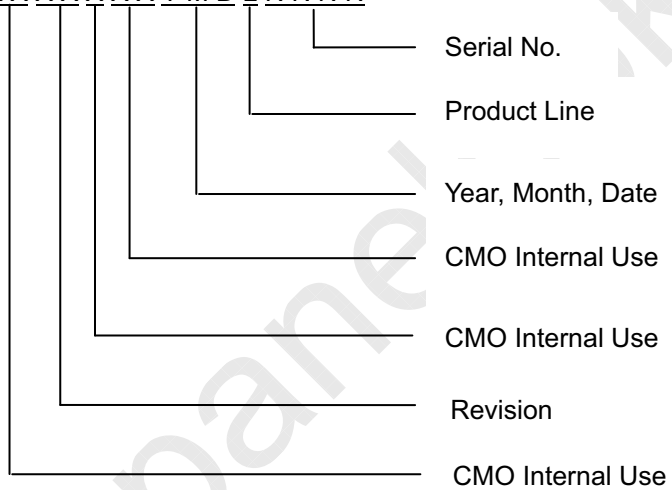
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V315H1-LH3

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



(d) Production Location:XXXX, for example:TAIWAN or CHINA .

Serial ID includes the information as below:

(a) Manufactured Date: 2001=1, 2002=2, 2003=3, 2004=4…2010=0,2011=1,2012=2....

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 5 LCD TV modules / 1 Box

(2) Box dimensions : 826(L) X 376 (W) X 540 (H)

(3) Weight : approximately 30Kg (5 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

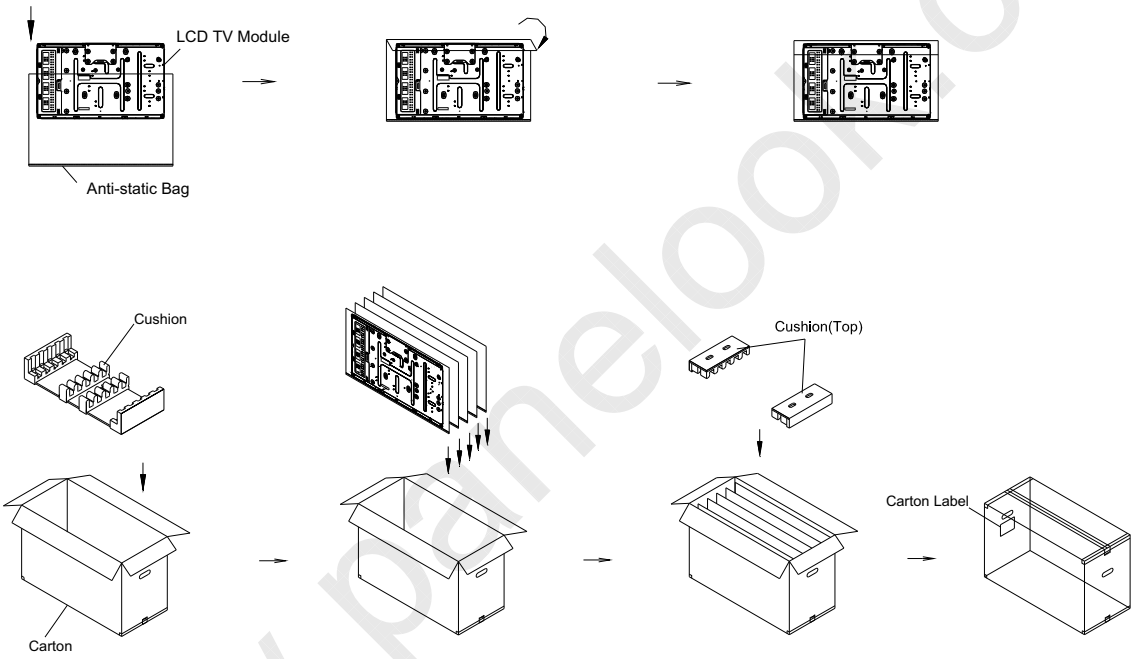
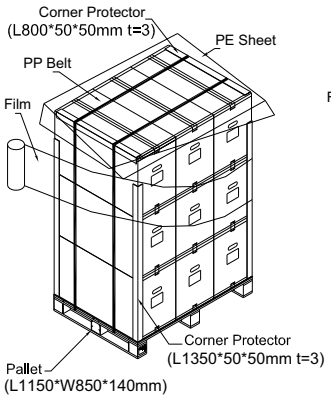
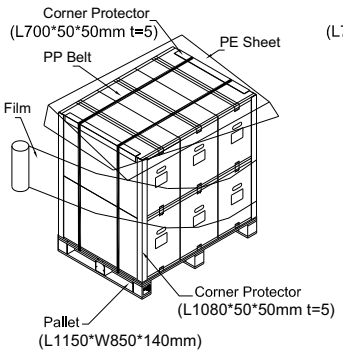


Figure.9-1 packing method

Sea / Land Transportation
(40ft Container)
Gross:285kg



Air Transportation
Gross:195kg



Sea / Land Transportation
(40ft HQ Container)
Gross:390kg

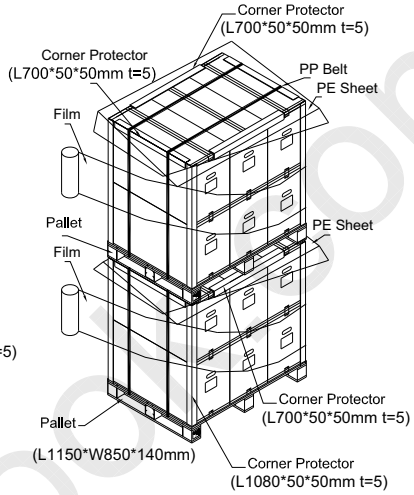


Figure.9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

10.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL 60950-1: 2003
	cUL	CAN/CSA C22.2 No.60950-1-03
	CB	IEC 60950-1:2001
Audio/Video Apparatus	UL	UL 60065: 2003
	cUL	CAN/CSA C22.2 No.60065-03
	CB	IEC 60065:2001

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

11. MECHANICAL CHARACTERISTICS