

TFT LCD Preliminary Specification

MODEL NO.:V315H3-LE2

Customer: _____

Approved by: _____

Note:

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CONTENTS -

1. GENERAL DESCRIPTION.....	5
1.1 OVERVIEW.....	5
1.2 FEATURES.....	5
1.3 APPLICATION.....	5
1.4 GENERAL SPECIFICATIONS.....	5
1.5 MECHANICAL SPECIFICATIONS.....	5
2. ABSOLUTE MAXIMUM RATINGS.....	6
2.1 ABSOLUTE RATINGS OF ENVIRONMENT.....	6
2.2 PACKAGE STORAGE.....	6
2.3 ELECTRICAL ABSOLUTE RATINGS.....	7
3. ELECTRICAL CHARACTERISTICS.....	8
3.1 TFT LCD MODULE.....	8
3.2 BACKLIGHT UNIT.....	10
4. BLOCK DIAGRAM OF INTERFACE.....	13
4.1 TFT LCD MODULE.....	13
5. INTERFACE PIN CONNECTION.....	14
5.1 TFT LCD MODULE.....	14
5.2 BACKLIGHT UNIT.....	17
5.3 CONVERTER UNIT.....	17
5.4 BLOCK DIAGRAM OF INTERFACE.....	19
5.5 LVDS INTERFACE.....	21
5.6 COLOR DATA INPUT ASSIGNMENT.....	22
6. INTERFACE TIMING.....	23
6.1 INPUT SIGNAL TIMING SPECIFICATIONS.....	23
6.2 POWER ON/OFF SEQUENCE.....	26
7. OPTICAL CHARACTERISTICS.....	27
7.1 TEST CONDITIONS.....	27
7.2 OPTICAL SPECIFICATIONS.....	27
8. DEFINITION OF LABELS.....	31
8.1 CMI MODULE LABEL.....	31
9. PACKAGING.....	32
9.1 PACKING SPECIFICATIONS.....	32
9.2 PACKING METHOD.....	32
10. PRECAUTIONS.....	34
10.1 ASSEMBLY AND HANDLING PRECAUTIONS.....	34
10.2 SAFETY PRECAUTIONS.....	34

10.3 STORAGE PRECAUTIONS.....	34
11. REGULATORY STANDARDS.....	35
11.1 SAFETY	35
12. MECHANICAL CHARACTERISTIC.....	36

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0		All	All	Preliminary Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315H3- LE2 is a TFT Liquid Crystal Display module with LED Backlight unit and 2ch-LVDS interface. The display diagonal is 31.5". This module supports 1920 x 1080 Full HDTV format and can display true 16.7M colors (8-bit/color).

1.2 FEATURES

- Optimized Brightness 450nits
- Contrast Ratio (6000:1)
- Fast Response Time (8ms)
- Color Saturation NTSC 72%
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) Only Mode
- LVDS (Low Voltage Differential Signaling) Interface
- Viewing Angle: 176(H)/176(V) (CR>20) MVA Technology
- Color Reproduction (Nature Color)

1.3 APPLICATION

- TFT LCD TVs
- Optimized Brightness, Multi-Media Displays

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	698.4(H) x 392.85(V)	mm	(1)
Bezel Opening Area	705.4(H) x 399.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.12125 (H) x 0.36375 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally Black	-	-
Surface Treatment	Anti-Glare coating (Haze 11%) Hard Coating (3H)	-	(2)

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note	
Module Size	Horizontal (H)	740.4	741.4	742.4	mm	Module Size
	Vertical (V)	434.8	435.8	436.8	mm	
Weight	Depth (D)	14.2	15.2	16.2	mm	To Rear
		34.9	35.9	36.9	mm	To Boss
Weight		4310		g		

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

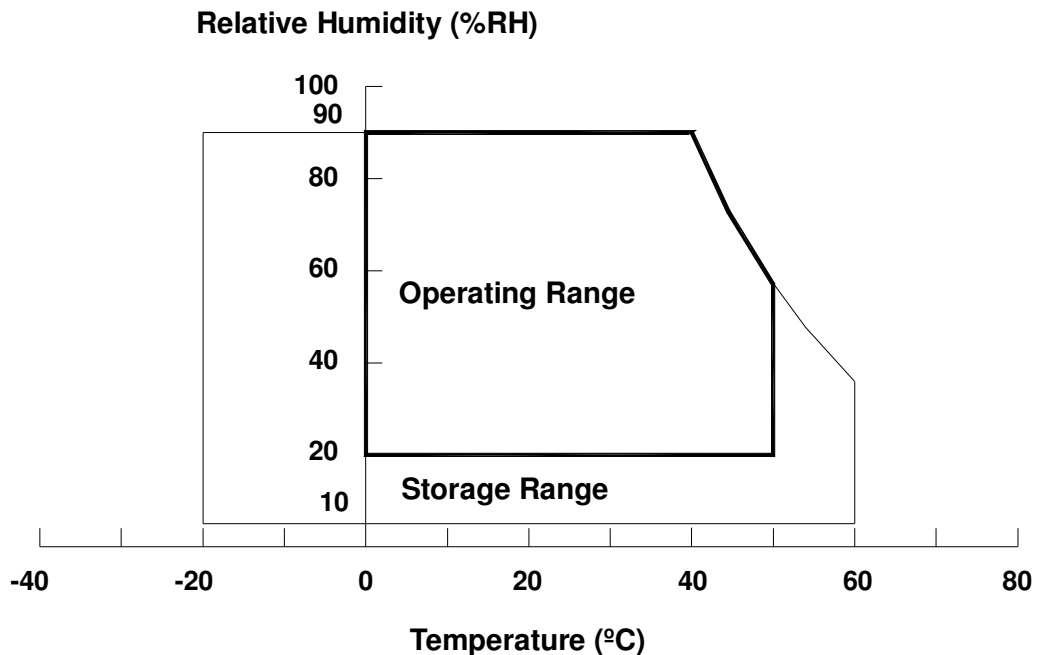
- (a) 90 %RH Max. ($T_a \leq 40$ °C).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 30 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	13.5	V	(1)
Input Signal Voltage	V _{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V _W	T _a = 25 °C	-	-	60	V	
Converter Input Voltage	V _{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

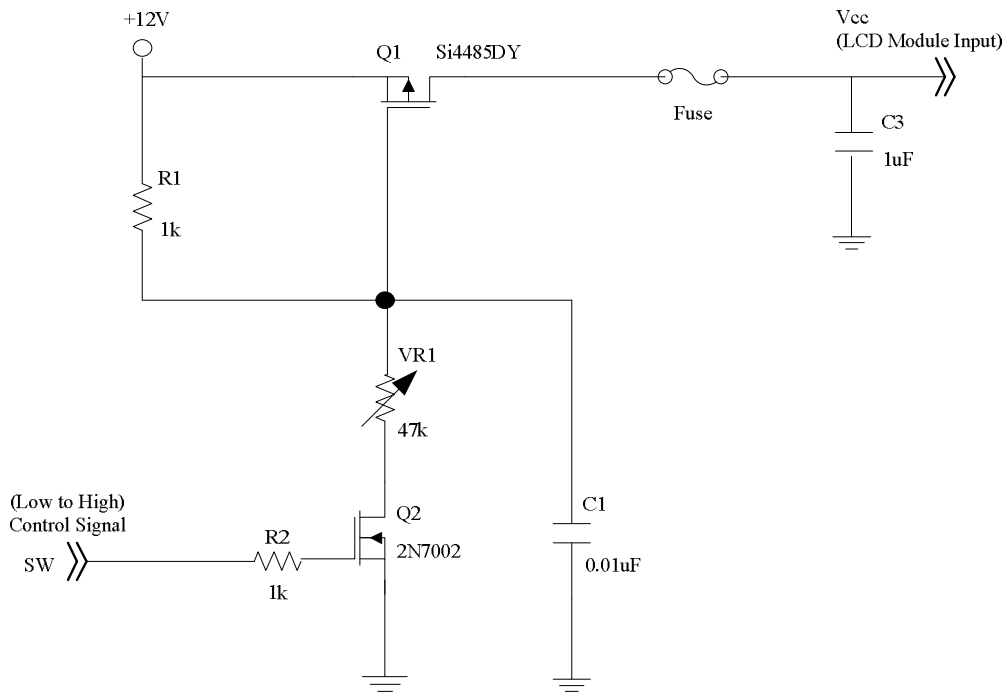
3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

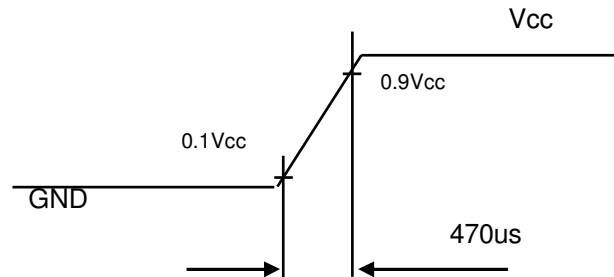
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	2.7	A	(2)
Power Supply Current	White Pattern	—	—	0.58	—	A	(3)
	Black Pattern	—	—	0.44	—	A	
	Horizontal Stripe	—	—	0.58	0.62	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^\circ\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



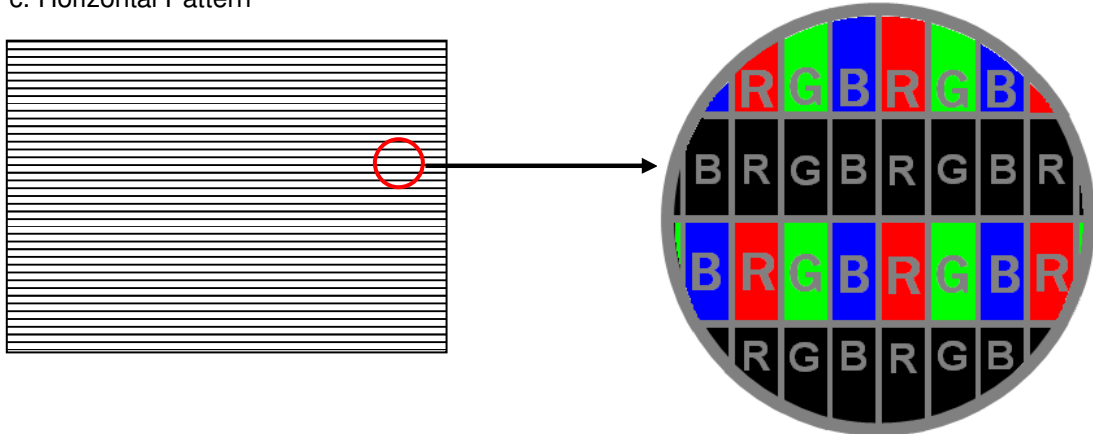
Active Area

b. Black Pattern

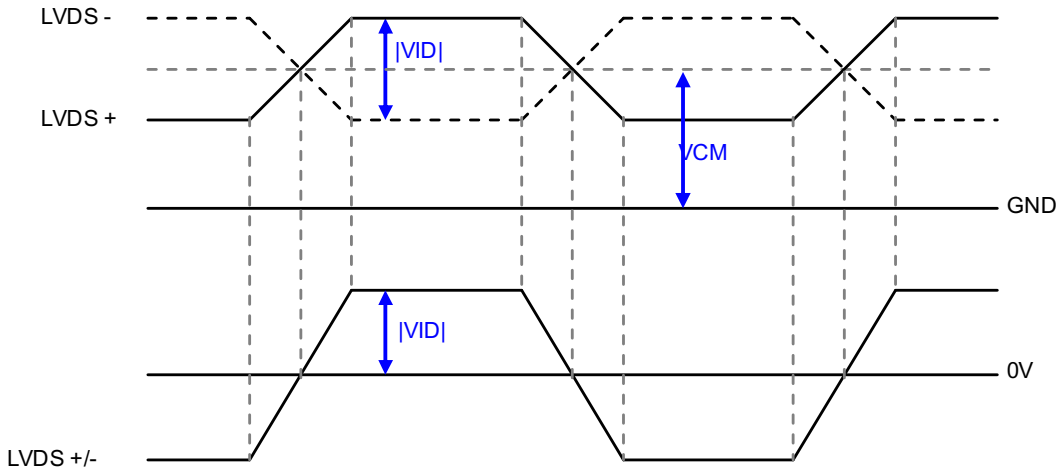


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT UNIT

3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Light Bar Voltage	V _W	-	-	47.6	V	I _L = 80mA
Forward Voltage	V _f	3.0	-	3.4	V	I _L = 80mA
LED Current	I _L	75.2	80	84.8	mA	

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL}	-	48.0	52.8	W	
Converter Input Voltage	V _{BL}	22.8	24	25.2	V _{DC}	
Converter Input Current	I _{BL}	-	2.0	2.2	A	
Dimming Frequency	F _B	150	160	170	Hz	
Minimum Duty Ratio	D _{MIN}	5	10	-	%	(1)

Note (1) 5% minimum duty ratio is only valid for electrical operation.

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter	Symbol	Test Condition	Value			Unit	Note	
			Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	3.0	3.15	3.3	V	maximum duty ratio
	MIN		—	—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on
	LO		—	0	—	0.8	V	Duty off
Error Signal	ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)	
VBL Rising Time	Tr1	—	30	—	—	ms	10%-90%V _{BL}	
VBL Falling Time	Tf1	—	30	—	—	ms		
Control Signal Rising Time	Tr	—	—	—	100	ms		
Control Signal Falling Time	Tf	—	—	—	100	ms		
PWM Signal Rising Time	TPWMR	—	—	—	50	us		
PWM Signal Falling Time	TPWMF	—	—	—	50	us		
Input Impedance	Rin	—	1	—	—	MΩ		
PWM Delay Time	TPWM	—	100	—	—	ms		
BLON Delay Time	T _{on}	—	300	—	—	ms		
	T _{on1}	—	300	—	—	ms		
BLON Off Time	Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

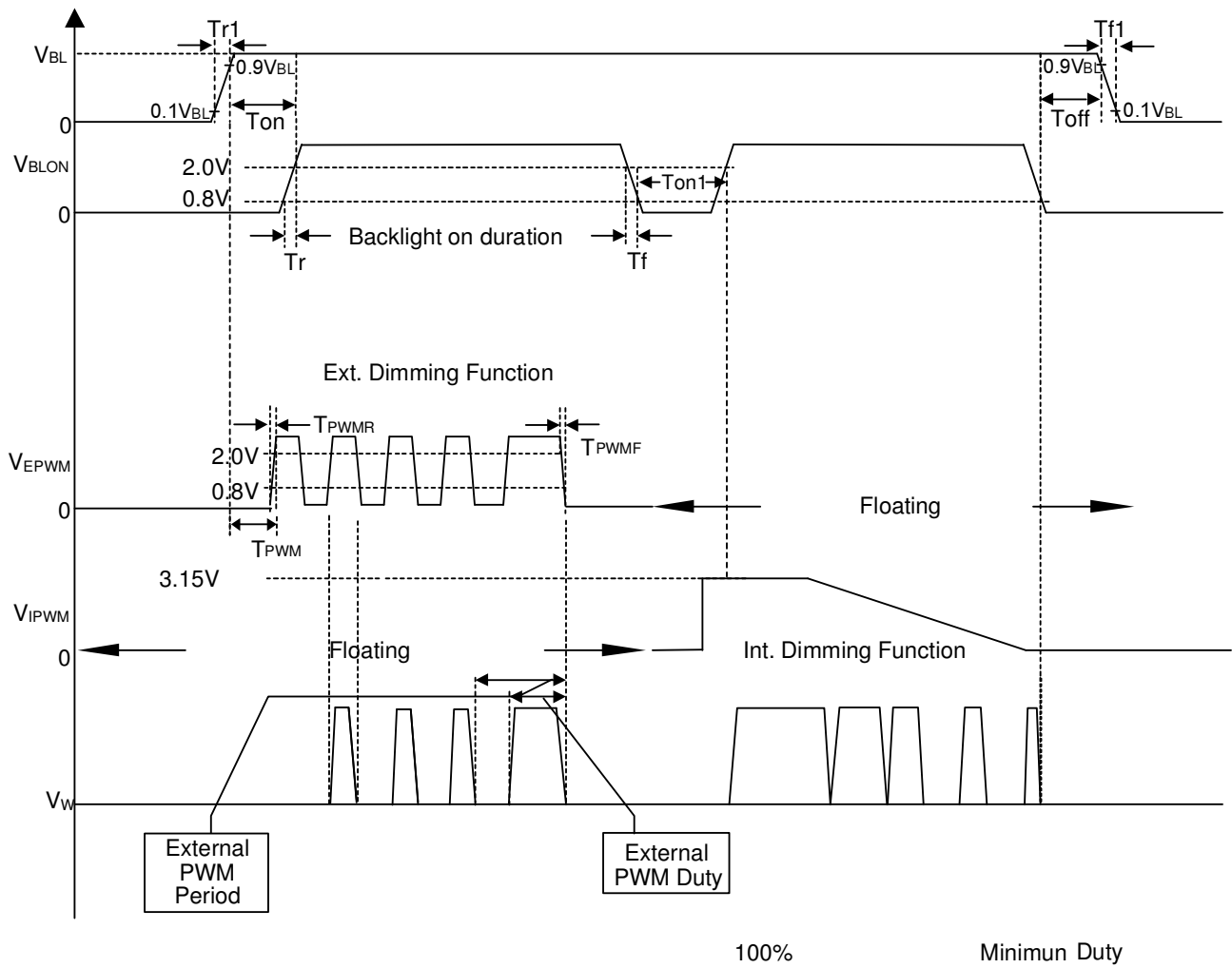
Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

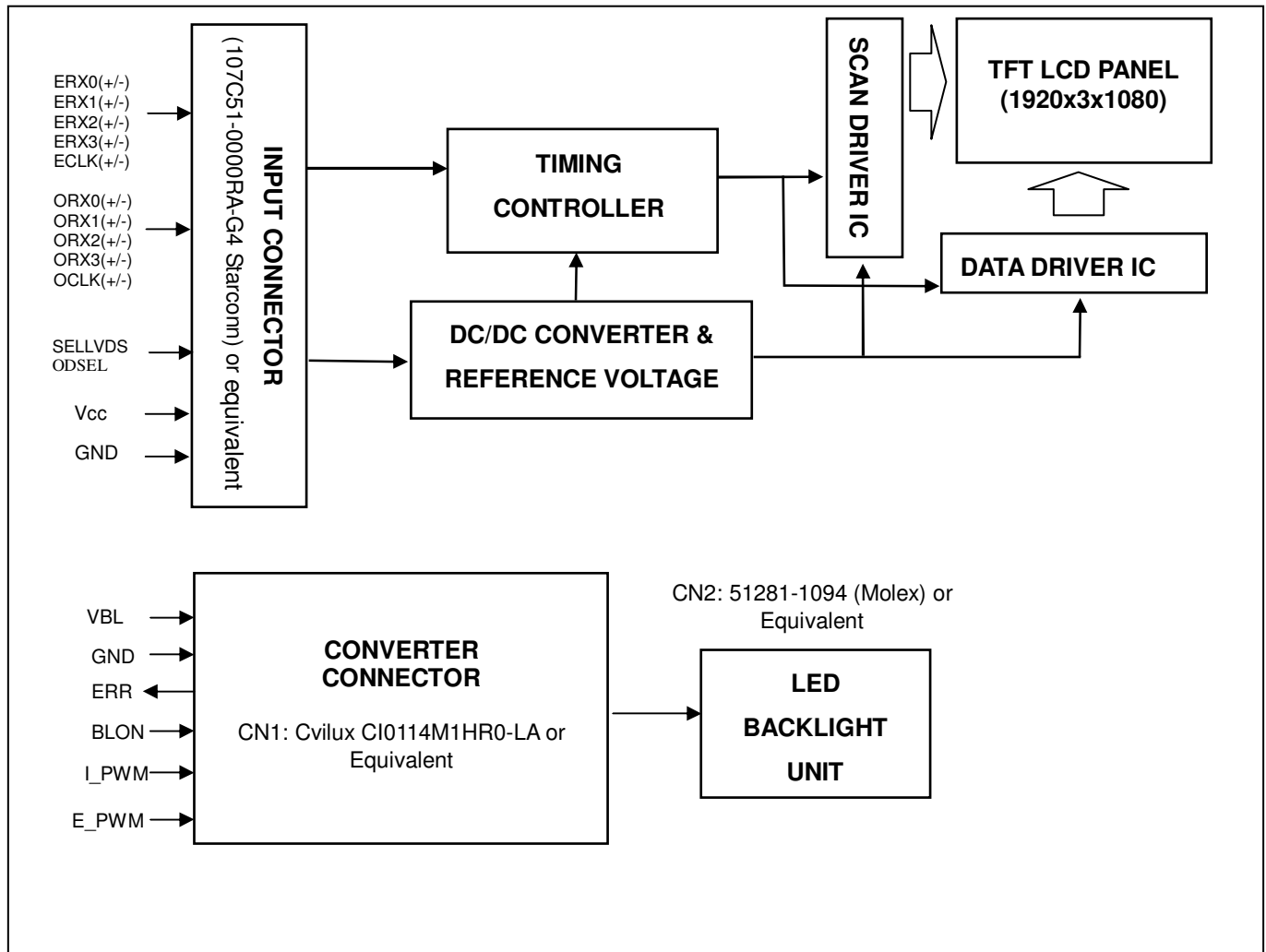
Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status.



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



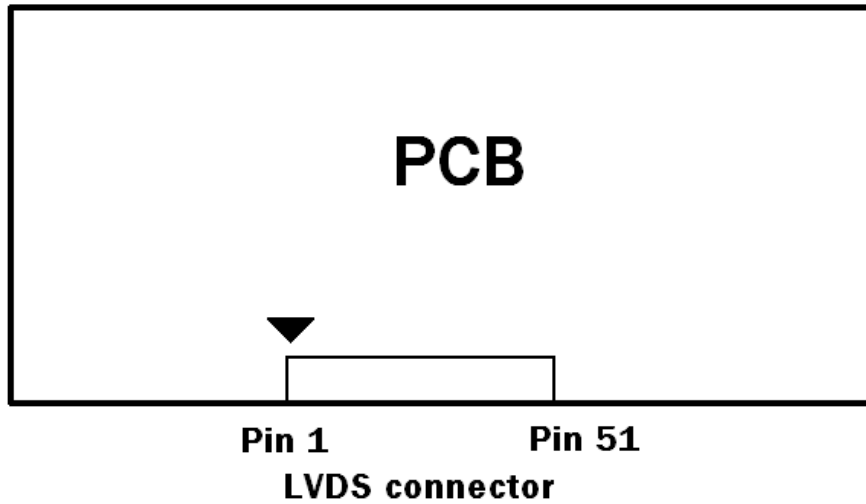
5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	(2)
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(3)(5)
8	N.C.	No Connection	(2)
9	ODSEL	Overdrive Lookup Table Selection	(4)(6)
10	N.C.	No Connection	(2)
11	GND	Ground	
12	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	
13	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	(7)
16	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	Even pixel Negative LVDS differential clock input.	
20	ECLK+	Even pixel Positive LVDS differential clock input.	(7)
21	GND	Ground	
22	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	
23	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	(7)
24	N.C.	No Connection	
25	N.C.	No Connection	(2)
26	GND	Ground	
27	GND	Ground	
28	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	
29	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	(7)
32	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	Odd pixel Negative LVDS differential clock input	
36	OCLK+	Odd pixel Positive LVDS differential clock input	(7)
37	GND	Ground	
38	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	
39	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	(7)
40	N.C.	No Connection	
41	N.C.	No Connection	(2)
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(2)
48	VCC	Power input (+12V)	
49	VCC	Power input (+12V)	
50	VCC	Power input (+12V)	
51	VCC	Power input (+12V)	

Note (1) LVDS connector pin order defined as follows



Note (2) Reserved for internal use. Please leave it open.

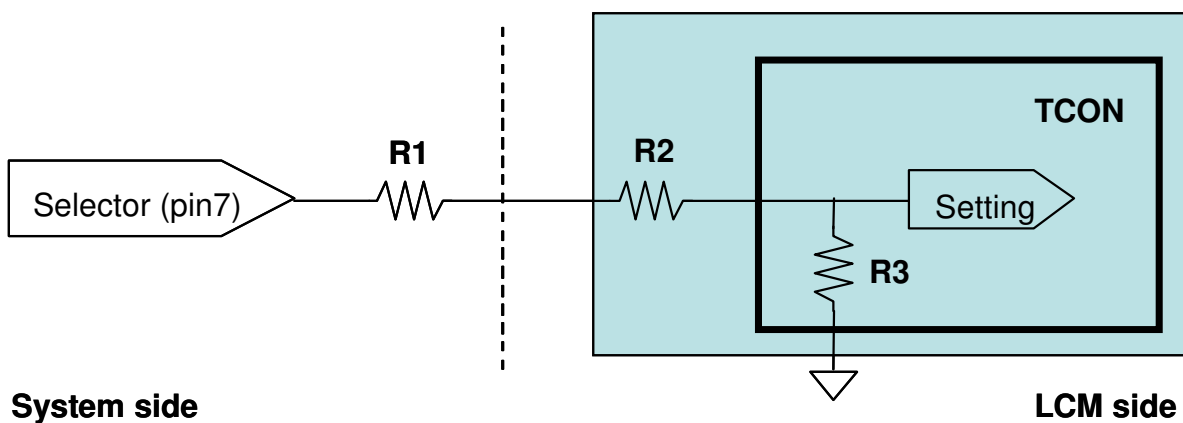
Note (3) Low = Open or connect to GND: VESA Format, High = Connect to +3.3V: JEIDA Format.

Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

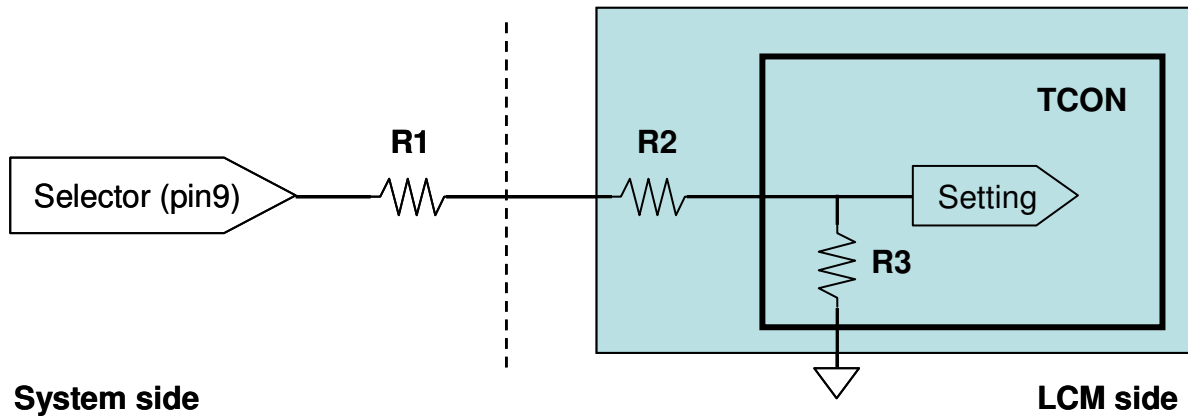
Low = Open or connect to GND, High = Connect to +3.3V

ODSEL	Note
L or open	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (5) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. ($R1 < 1K \text{ Ohm}$)



Note (6) ODSEL signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. ($R1 < 1K \text{ Ohm}$)



Note (7) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN: 51281-1094 (Molex) or Equivalent

Pin №	Symbol	Feature
1	VLED+	Positive of LED String
2		
3	NC	NC
4		
5	N1	Negative of LED String
6	N2	
7	N3	
8	N4	
9	N5	
10	N6	

5.3 CONVERTER UNIT

CN1(Header): Cvilux CI0114M1HR0-LA or Equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open collector)
12	BLON	BL ON/OFF
13	I_PWM	Internal PWM Control
14	E_PWM	External PWM Control

Note (1) PIN 13:Internal PWM Control (Use Pin 13): Pin 14 must open.

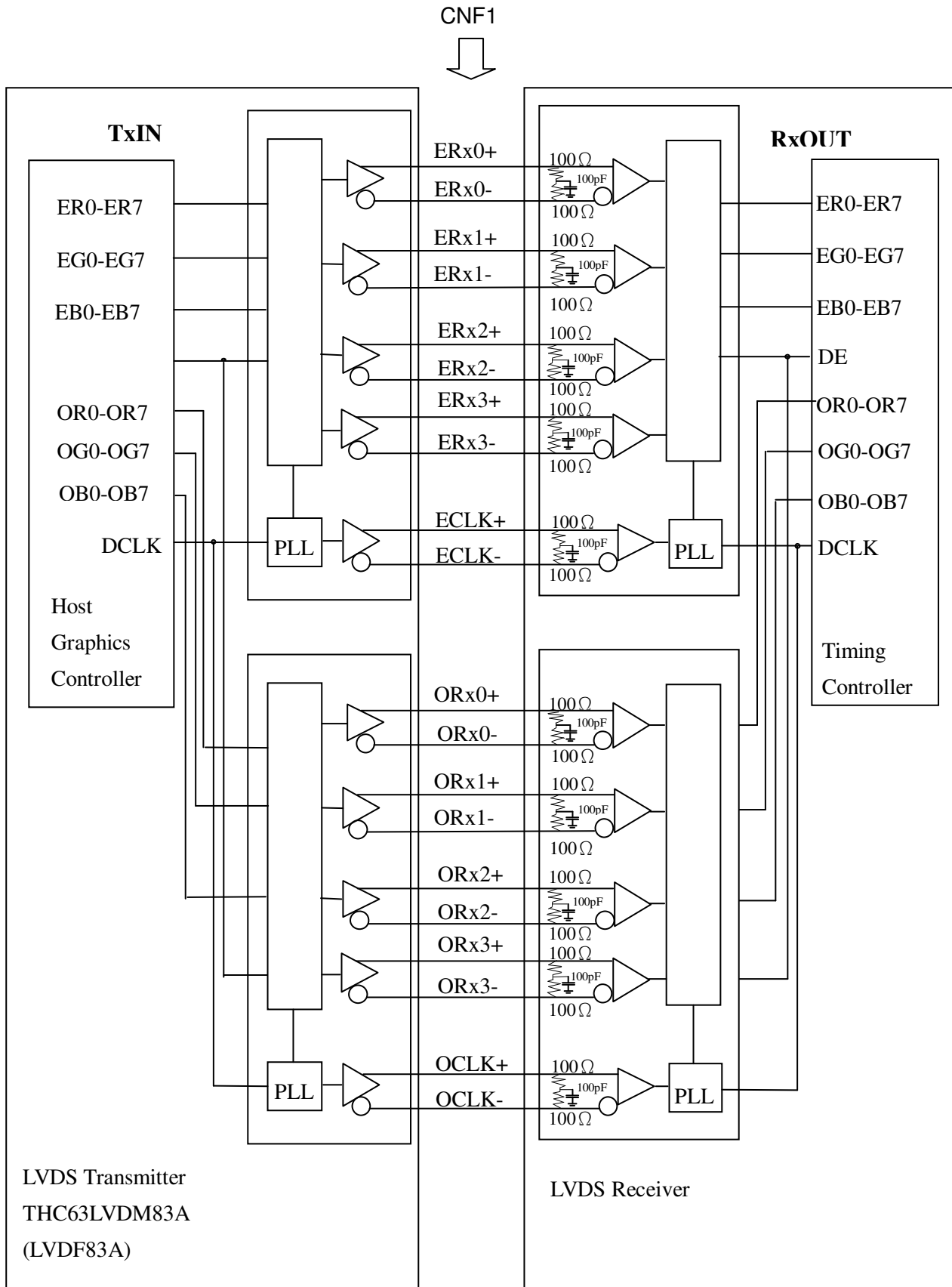
Note (2) PIN 14:External PWM Control (Use Pin 14): Pin 13 must open.

Note (3) Pin 13(I_PWM) and Pin 14(E_PWM) can't open in same period.

CN2(Header): 51281-1094 (Molex) or Equivalent

Pin №	Symbol	Feature
1	VLED+	Positive of LED String
2		
3	NC	NC
4		
5	N1	Negative of LED String
6	N2	
7	N3	
8	N4	
9	N5	
10	N6	

5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7: Even pixel R data
EG0~EG7: Even pixel G data
EB0~EB7: Even pixel B data
OR0~OR7: Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7: Odd pixel B data
DE: Data enable signal
DCLK: Data clock signal

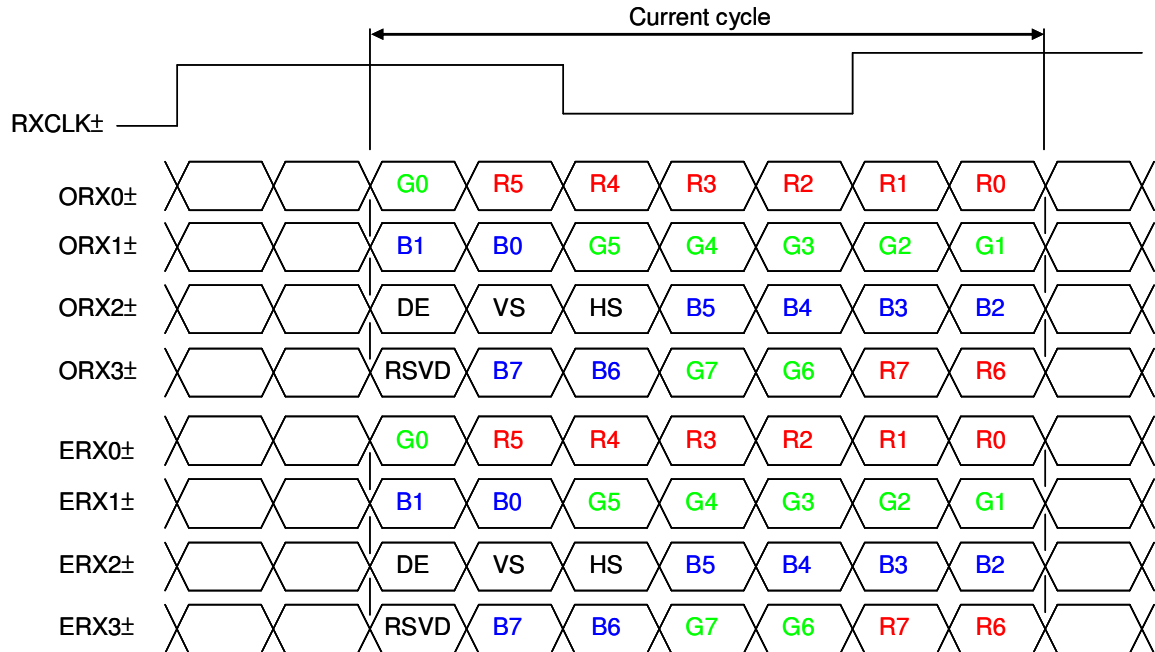
Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

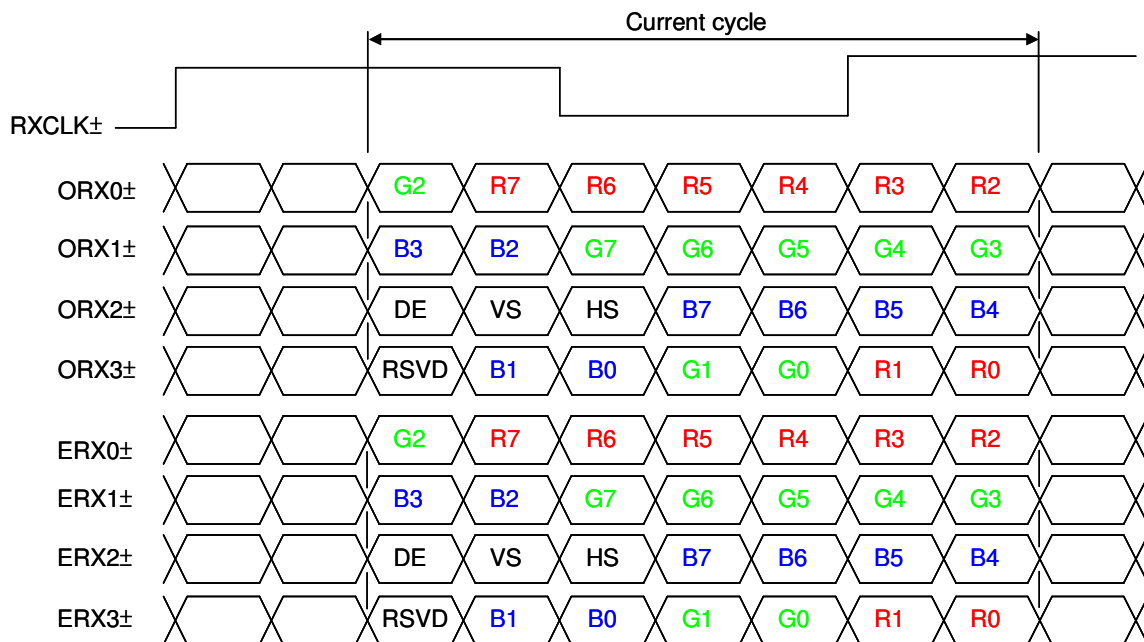
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.5 LVDS INTERFACE

VESA LVDS format : (SELLVDS pin=L or open)



JEDIA LVDS format : (SELLVDS pin=H)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color.
 The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
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	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{clk_{in}}$ (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcj}	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{clk_{in_mod}}$	$F_{clk_{in}}-2\%$	—	$F_{clk_{in}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Setup Time	T_{lvsu}	600	—	—	ps	(5)
	Hold Time	T_{lvhd}	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(6)
		F_{r6}	57	60	63	Hz	
	Total	T_v	1115	1125	1135	Th	$T_v=T_{vd}+T_{vb}$
	Display	T_{vd}	1080	1080	1080	Th	—
	Blank	T_{vb}	35	45	55	Th	—
Horizontal Active Display Term	Total	T_h	1050	1100	1150	Tc	$T_h=T_{hd}+T_{hb}$
	Display	T_{hd}	960	960	960	Tc	—
	Blank	T_{hb}	90	140	190	Tc	—

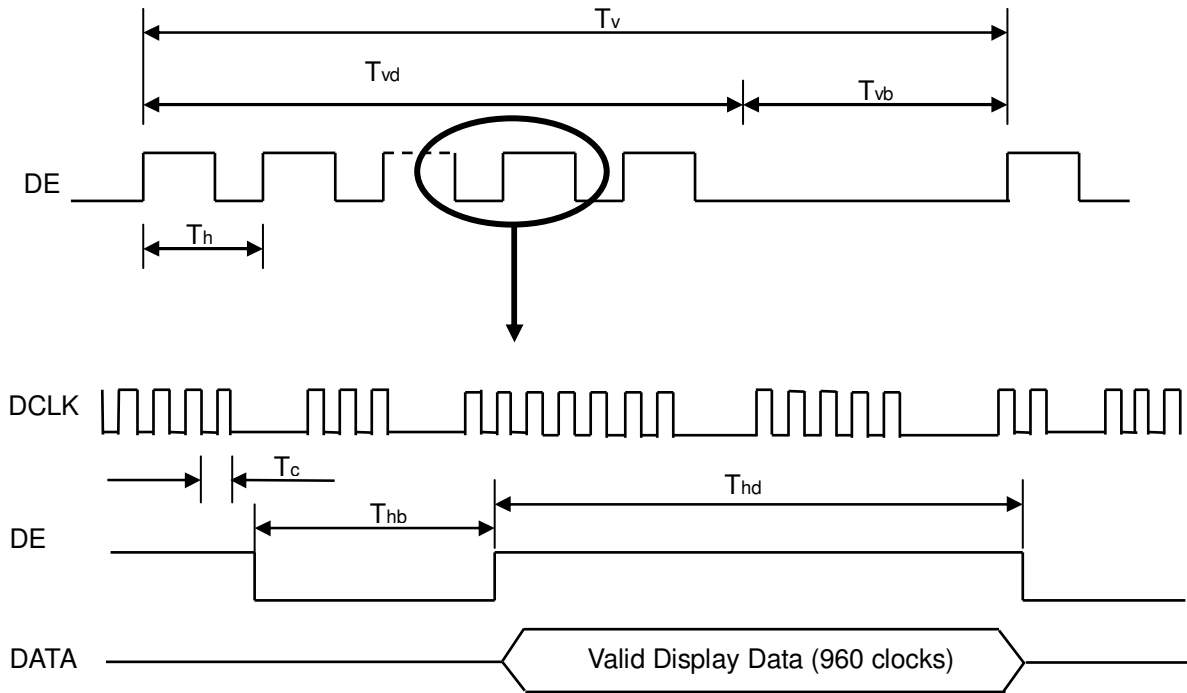
Note (1) Please make sure the range of pixel clock has follow the below equation :

$$F_{clk_{in}}(\max) \geq F_{r6} \times T_v \times T_h$$

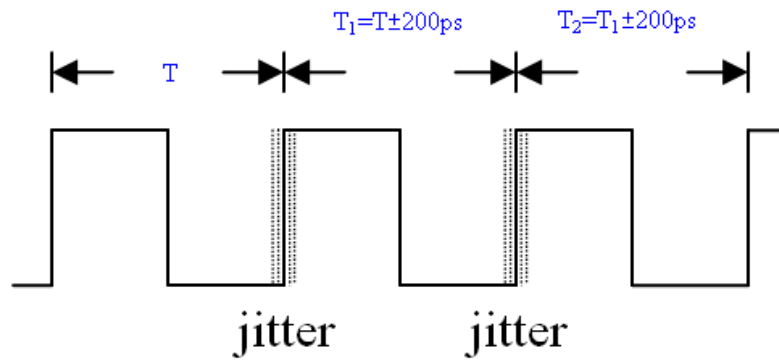
$$F_{r5} \times T_v \times T_h \geq F_{clk_{in}}(\min)$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

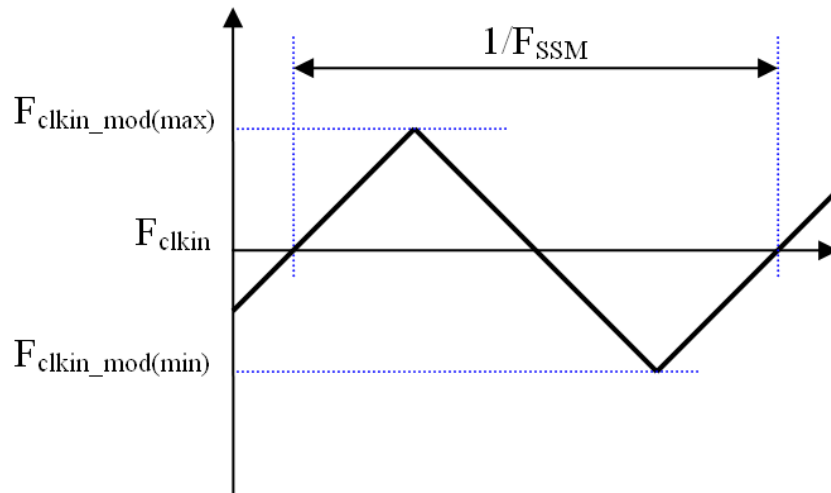
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$

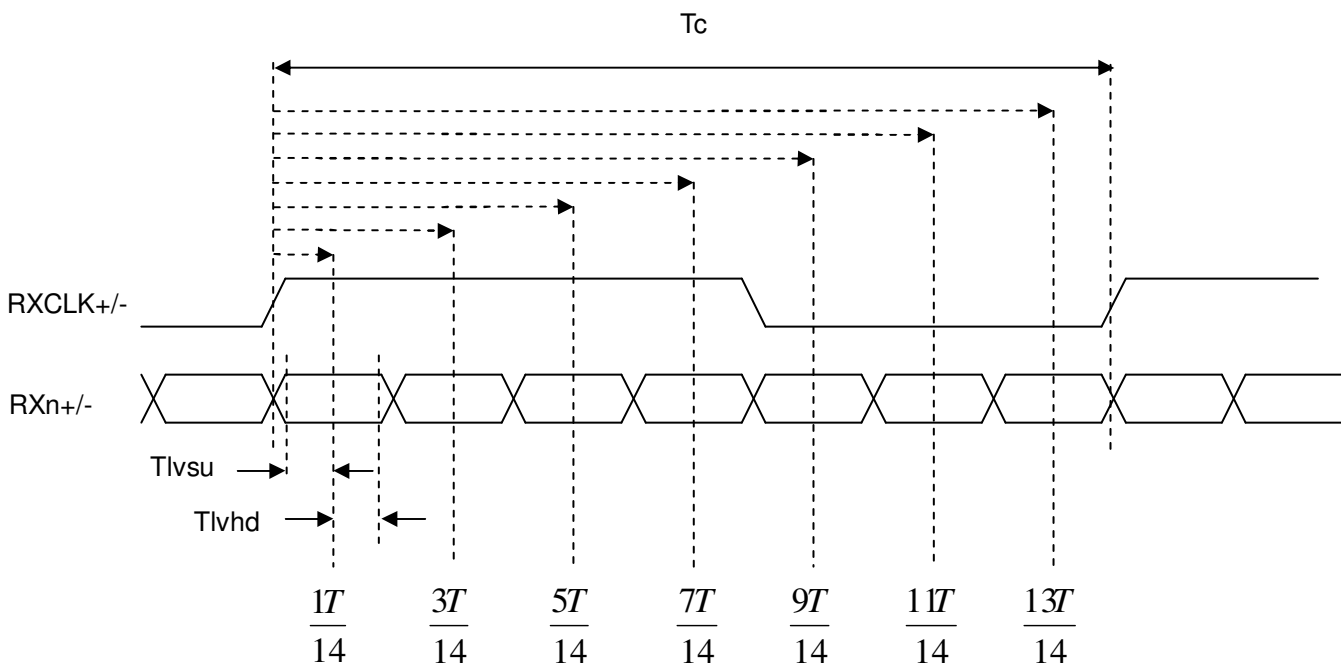


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

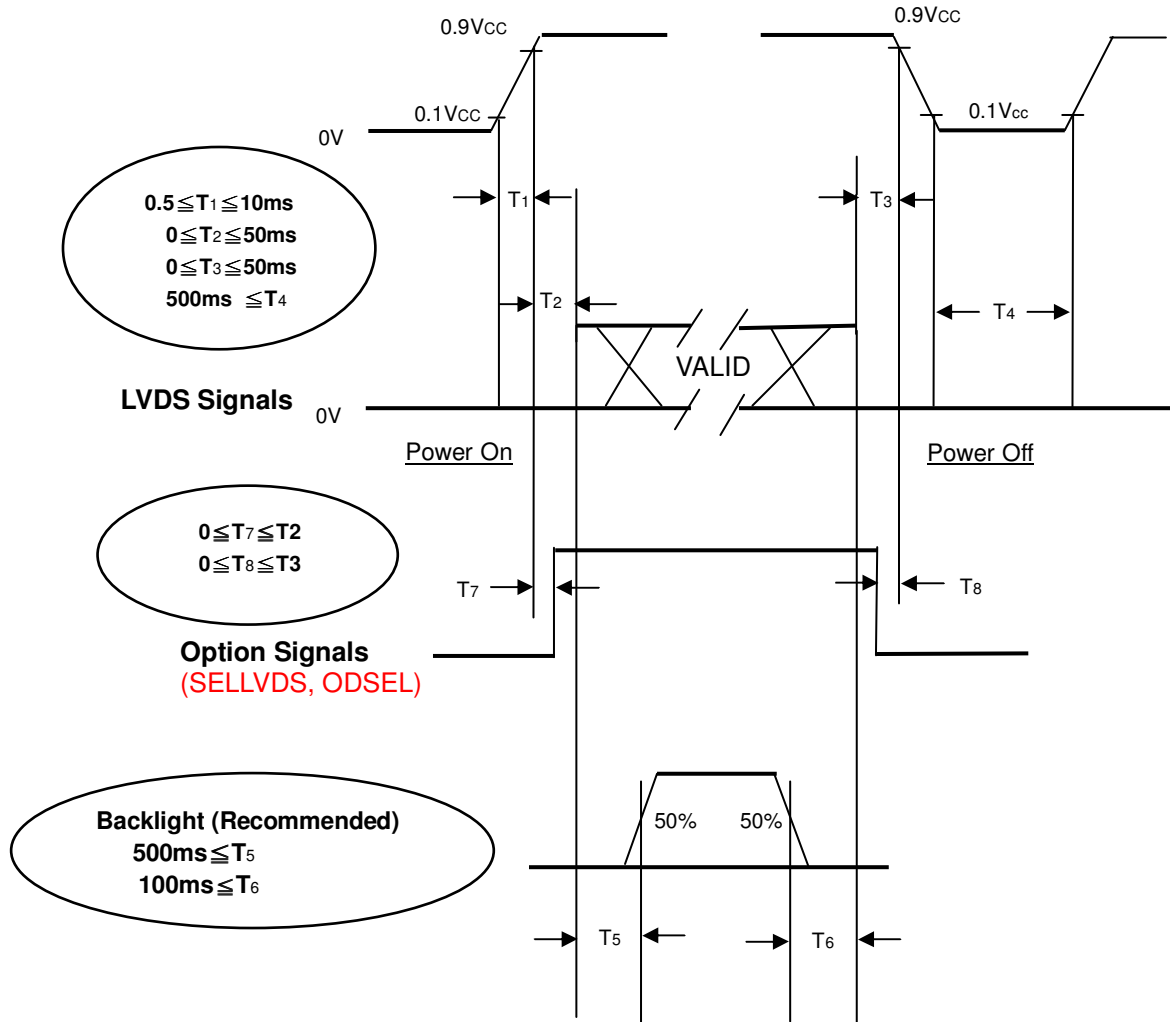


Note (6) (ODSEL) = H/L or open for 50/60Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

($T_a = 25 \pm 2 \text{ }^\circ\text{C}$)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

- Note (1) The supply voltage of the external system for the module input should follow the definition of V_{cc} .
- Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- Note (3) In case of V_{cc} is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.
- Note (4) T_4 should be measured after the module has been fully discharged between power off and on period.
- Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I _L	80±4.8	mA

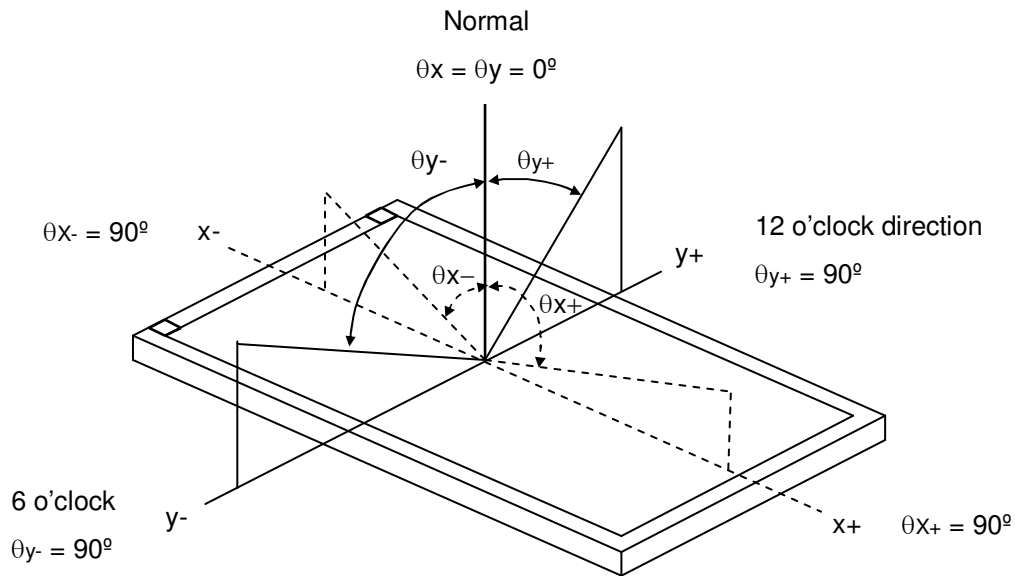
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Angle at Normal Direction	(4200)	(6000)		-	(2)	
Response Time		Gray to gray average		-	(8)	-	ms	(3)	
Center Luminance of White		L _c		(360)	(450)		cd/m ²	(4)	
White Variation		δW		-	-	1.3	-	(7)	
Cross Talk		CT		-	-	4.0	%	(5)	
Color Chromaticity	Red	Rx		Typ -0.03	(0.624)	Typ +0.03	-	-	(6)
		Ry							
	Green	Gx							
		Gy							
	Blue	Bx							
		By							
	White	Wx							
		Wy							
Color Gamut		CG		(72)		%	NTSC		
Viewing Angle	Horizontal	θ _{x+}	CR≥20	88	-	-	Deg.	(1)	
		θ _{x-}							
	Vertical	θ _{y+}							
		θ _{y-}							

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

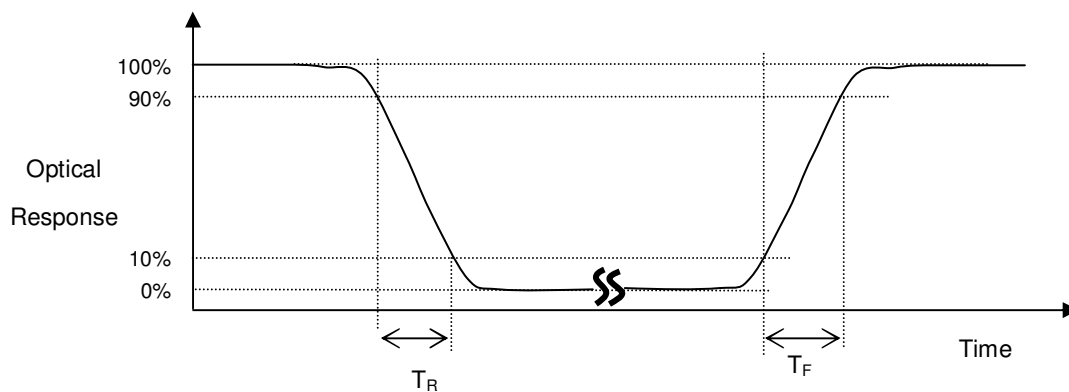
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7)

Note (3) Definition of Response Time (Gray to Gray switching time):



The driving signal means the signal of Gray 0, 31, 63, 95, 127, 159, 191, 223, 255. Gray to gray average time means the average switching time of gray 0, 31, 63, 95, 127, 159, 191, 223, 255 to each other.

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point.

$L_C = L(5)$, where $L(x)$ is corresponding to the luminance of the point X at the figure in Note (7).

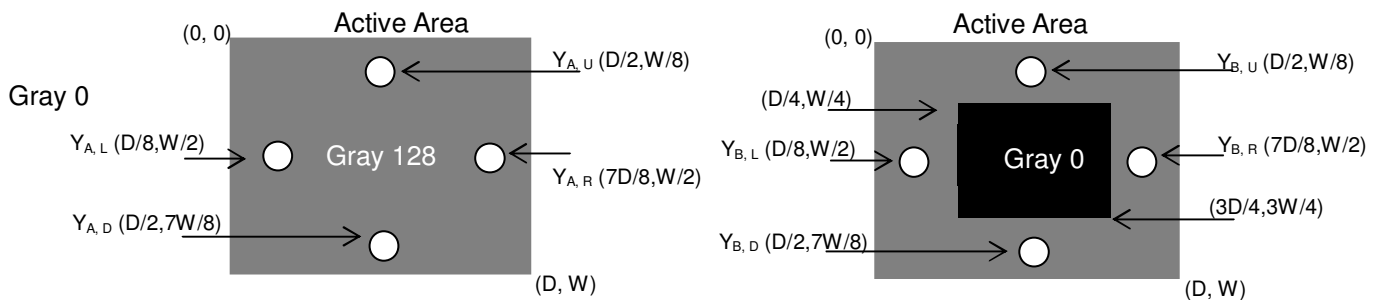
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

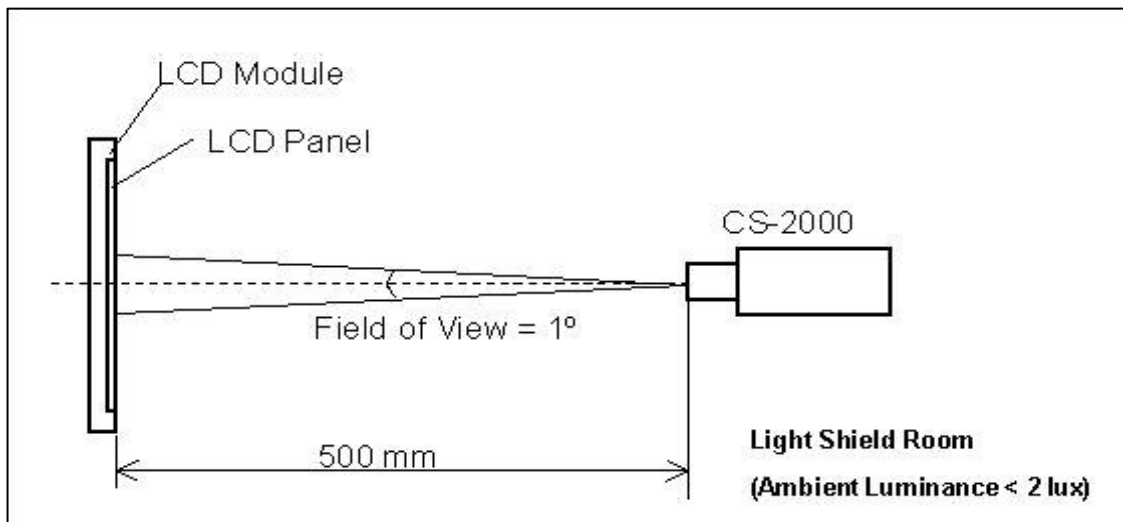
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

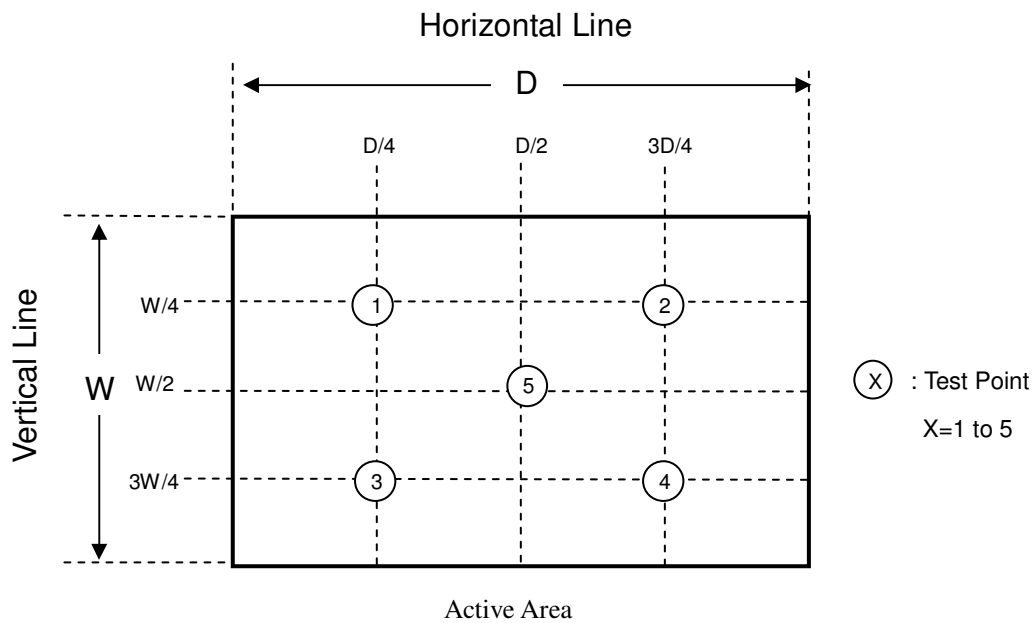
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

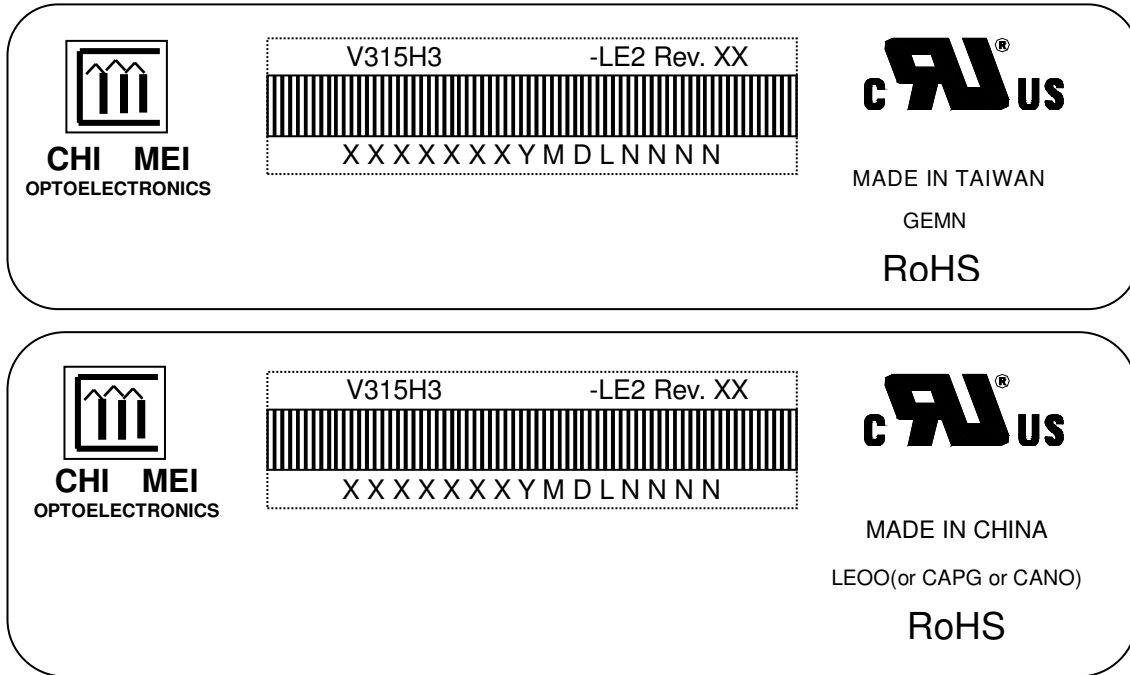
$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$



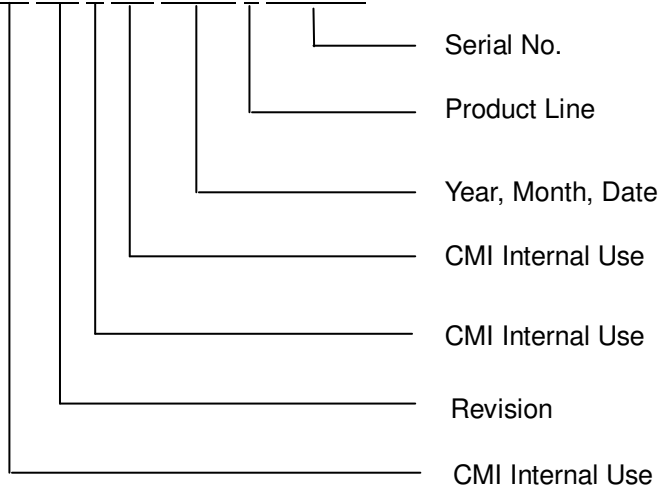
8. DEFINITION OF LABELS

8.1 CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V315H3-LE2
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Serial ID: XXXXXXXYMDLNNNN



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.
- (b) Revision Code: Cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

- (1) 7 LCD TV modules / 1 Box
- (2) Box dimensions : 826(L)x376(W)x540(H)mm
- (3) Weight : approximately 31 Kg (7 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

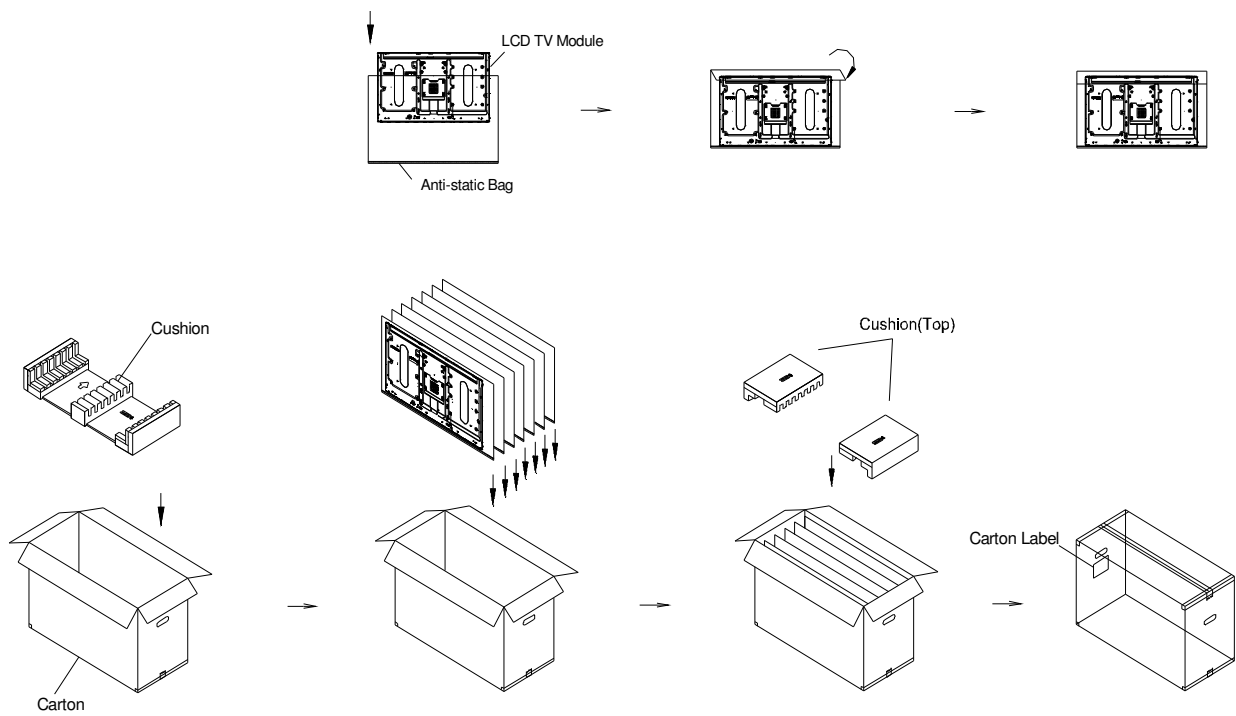
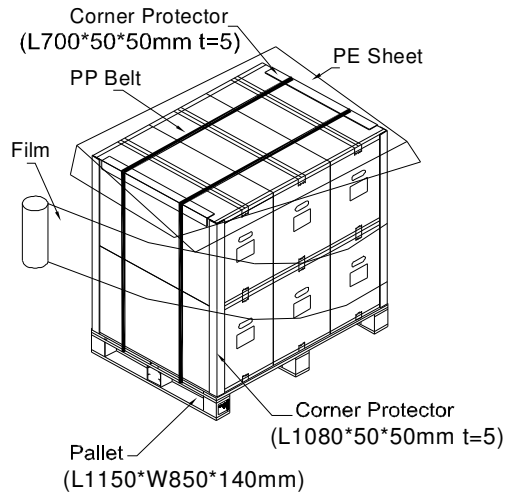
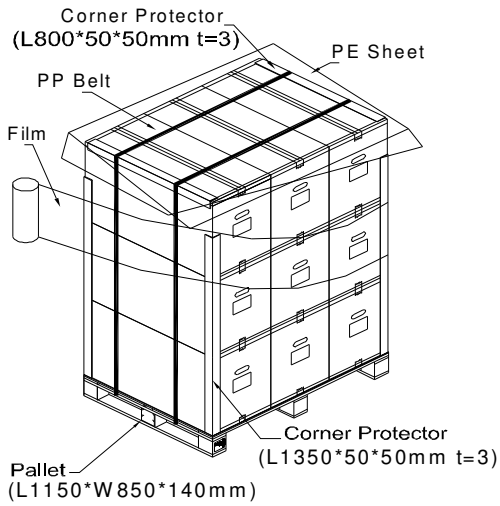


Figure.9-1 packing method

Sea / Land Transportation
(40ft Container)

Air Transportation



Sea / Land Transportation
(40ft HQ Container)

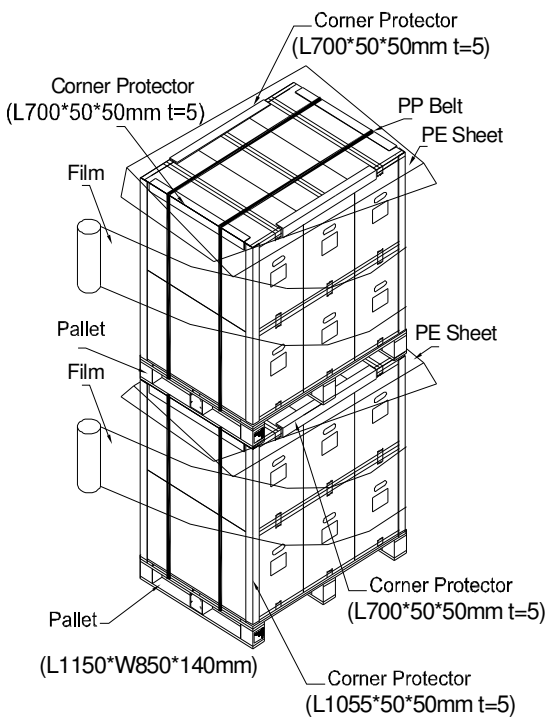


Figure. 9-2 Packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow.

10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

10.3 STORAGE PRECAUTIONS

When storing modules as spares for a long time, the following precaution is necessary.

- (1) Do not leave the module in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
- (2) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

11. REGULATORY STANDARDS

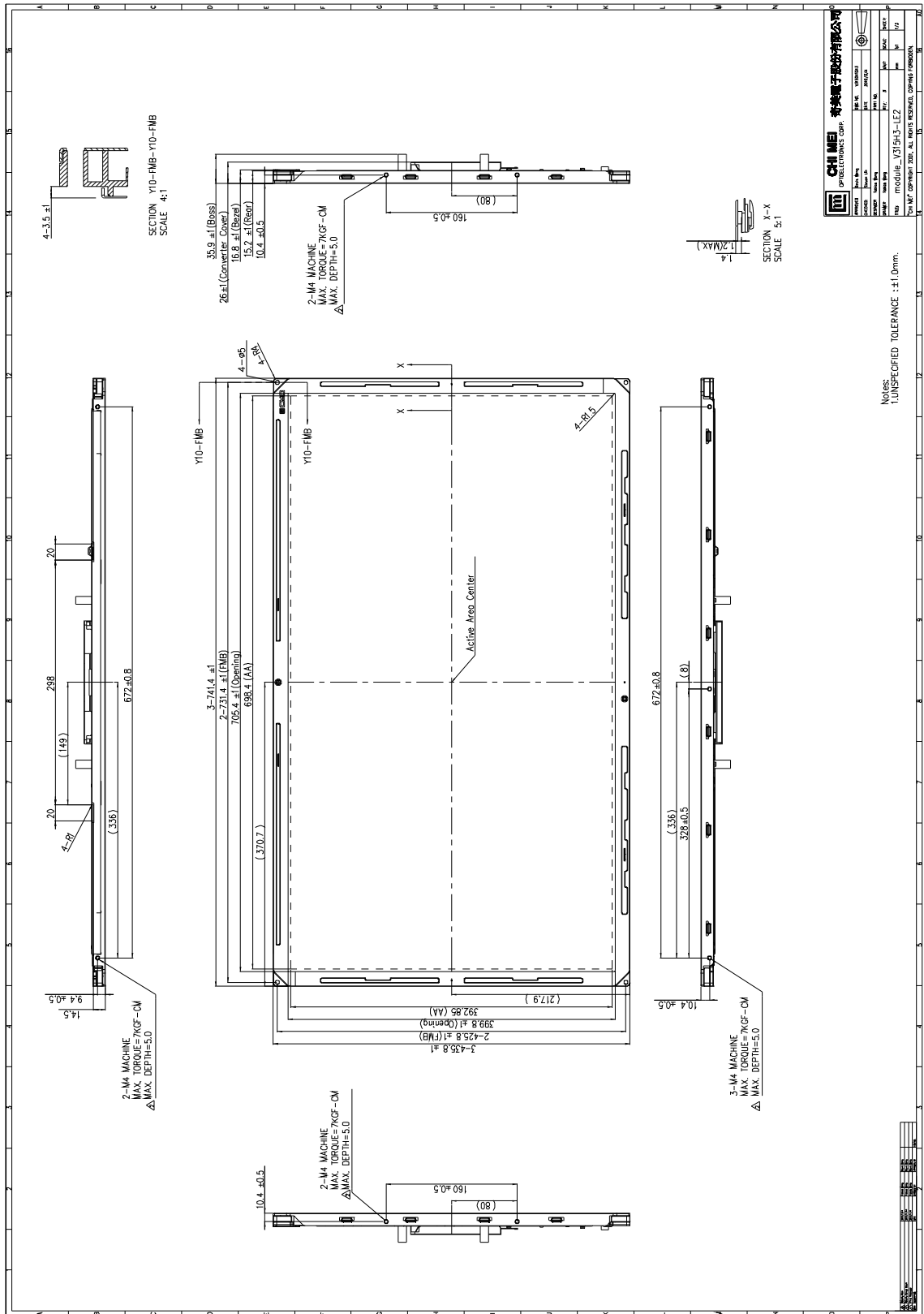
11.1 SAFETY

The LCD module should be certified with safety regulations as follows:

Requirement	Standard	Remark
UL	UL60950-1:2006 or Ed.2:2007	
	UL60065 Ed.7:2007	
cUL/CSA	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07	
	CAN/CSA C22.2 No.60065-03:2006 + A1:2006	
CB	IEC60950-1:2005 / EN60950-1:2006+ A11:2009	
	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006 + A11:2008	

Preliminary

12. MECHANICAL CHARACTERISTIC



Preliminary

