☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: V315H3
SUFFIX: LS5

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Vincent Chou	Perry Lin

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	July. 5, 2011	All	All	The approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315H3- LS5 is a 31.5" TFT Liquid Crystal Display module with LED Backlight and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 1.07G colors (8-bit + FRC). The converter module for backlight is built-in.

1.2 FEATURES

- High brightness (400 nits)
- Ultra-high contrast ratio (5000:1)
- Faster response time (gray to gray average 6 ms)
- High color saturation NTSC 72% (72%)
- Ultra wide viewing angle: 176(H)/176(V) (CR≥20) with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Low color shift function
- RoHs compliance

1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	698.4 (H) x 392.85 (V)	mm	(1)
Bezel Opening Area	705.4 (H) x 400 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.12125 (H) x 0.36375 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Power Consumption	(49.2 W) (LVDS input Power 13.2W + LED Backlight Power 36W)	Watt	(2)
Display Colors	1.07G	color	
Display Operation Mode	Transmissive mode / Normally Black	-	
Surface Treatment	Anti-Glare Coating (Haze 11%) Hard Coating (3H)	-	(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) Please refer sec 3.1 and 3.2 for more information of Power consumption

Note (3) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	724.2	725.2	726.2	mm	(1)
	Vertical(V)	420.9	421.9	422.9	mm	(1)
	Depth(D)	14.1	15.1	16.1	mm	
	Depth(D)	22.6	23.6	24.6	mm	To converter cover
Weight			4220		g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

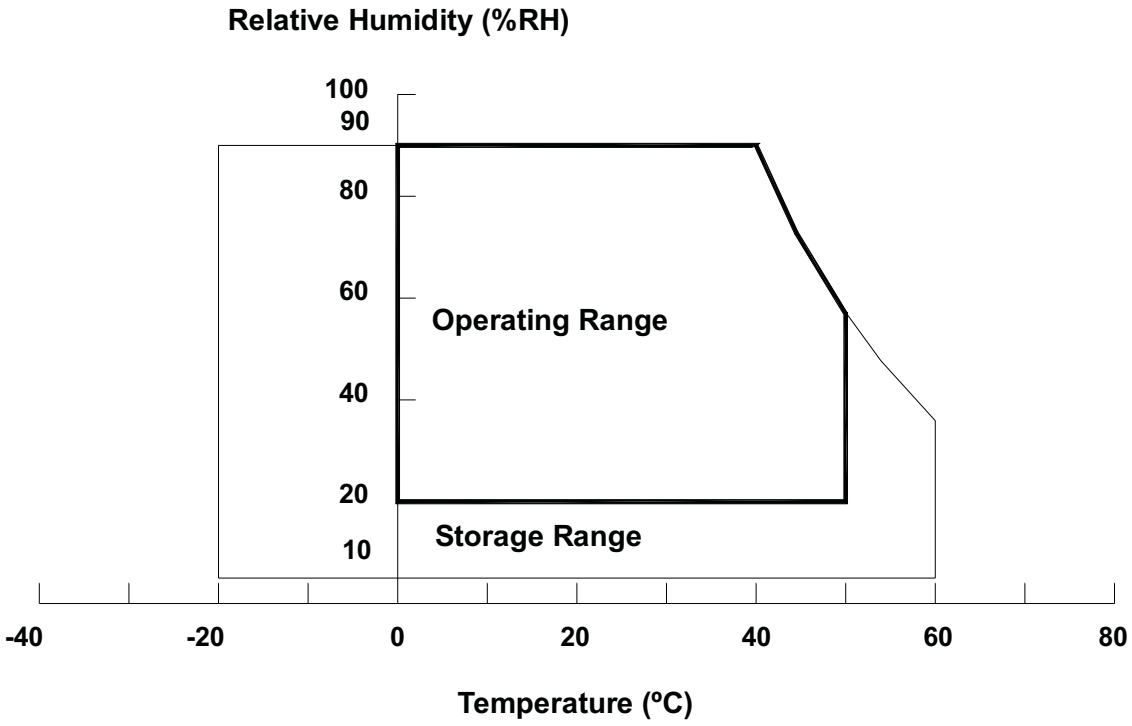
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.5	V	
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V_W	Ta = 25 ℃	-	-	60	V_{RMS}	3D Mode
Converter Input Voltage	V_{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

3. ELECTRICAL CHARACTERISTICS

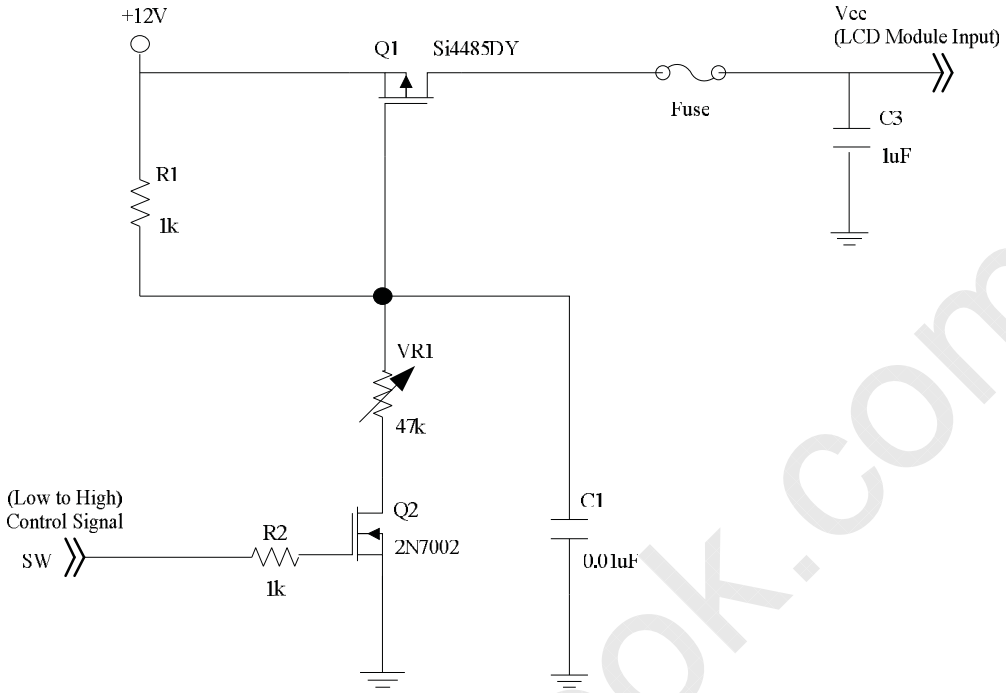
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

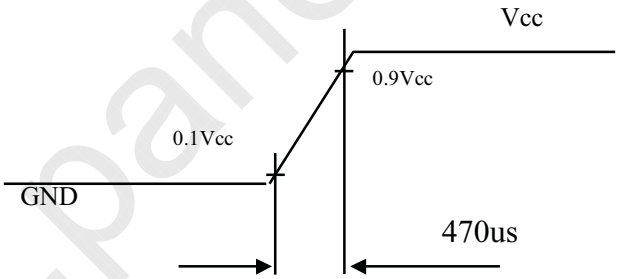
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	1.96	A	(2)
Power Consumption	White Pattern	-		6.0	6.5	W	(3)
	Horizontal Stripe	-		10.9	13.2	W	
	Black Pattern	-		5.9	6.3	W	
Power Supply Current	White Pattern	-	-	0.50	0.54	A	
	Horizontal Stripe	-	-	0.91	1.1	A	
	Black Pattern	-	-	0.49	0.53	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power consumption and power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, fv = 120 Hz, whereas a power dissipation check pattern below is displayed.

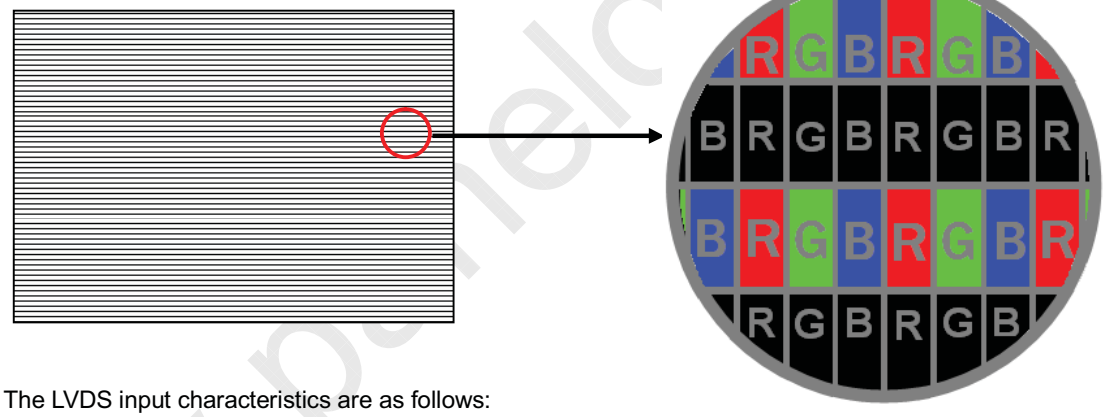
a. White Pattern

Active Area

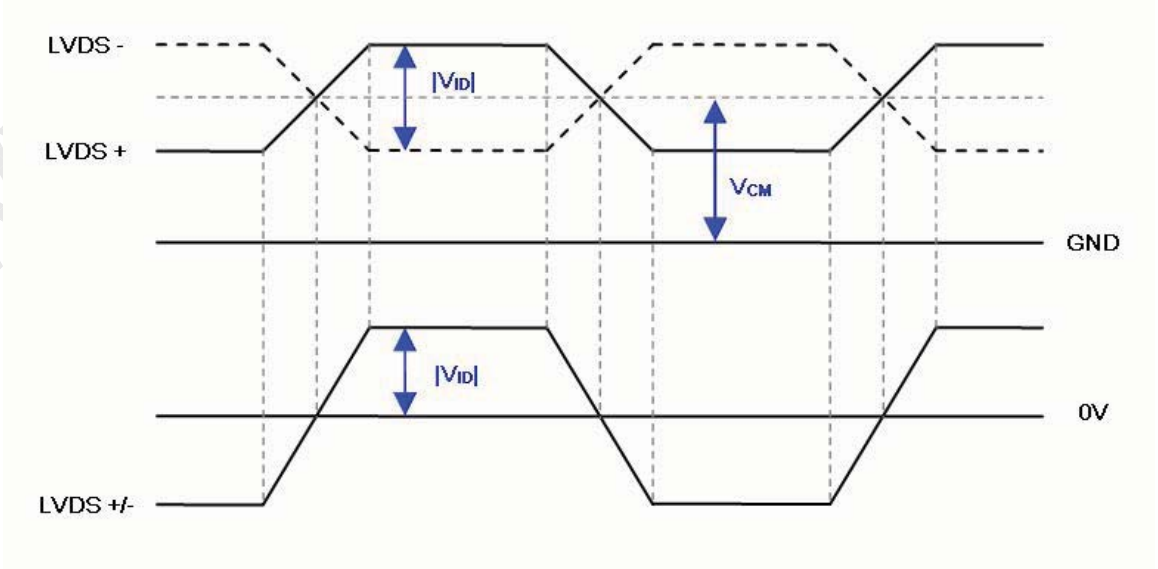
b. Black Pattern

Active Area

c. Horizontal Stripe Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT CONVERTER UNIT

3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 ºC)

The backlight unit contains 2 pcs light bar.

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Current (12 String)	If	-	1200.0	1272.0	mA	
One String Current	$I_{L(2D)}$	-	100.0	106.0	mA	
	$I_{L(3D)}$	-	300.0	318.0	mApeak	3D ENA=ON
One String Voltage	V_W	24.3	-	30.6	V_{DC}	I_L =100mA
One String Voltage Variation	$\triangle V_W$	-	-	2	V	
Life time	-	30,000	-	-	Hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2℃, IL =100mA

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	$P_{BL(2D)}$	-	36.0	41.4	W	(1), (2) IL = 100 mA
	$P_{BL(3D)}$	-	27.0	32.0	W	(1), (2) IL=3*typ.
Converter Input Voltage	VBL	22.8	24.0	25.2	VDC	
Converter Input Current	$I_{BL(2D)}$	1.2	1.5	1.73	A	Non Dimming
	$I_{BL(3D)}$	0.9	1.13	1.33	A	
Input Inrush Current	$I_{R(2D)}$	-	-	2.33	Apeak	V_{BL}=22.8V,(IL=typ.) (3), (6)
	$I_{R(3D)}$	-	-	4.2	Apeak	V_{BL}=22.8V,(IL=3*typ.) (3), (6)
Dimming Frequency	FB	150	160	170	Hz	(5)
Minimum Duty Ratio	DMIN	5	10	-	%	(4), (5)

Note (1) The power supply capacity should be higher than the total converter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 31.5" backlight unit under input voltage 24V, average LED current 106 mA at 2D Mode (LED current 318 mApeak at 3D Mode) and lighting 1 hour later.

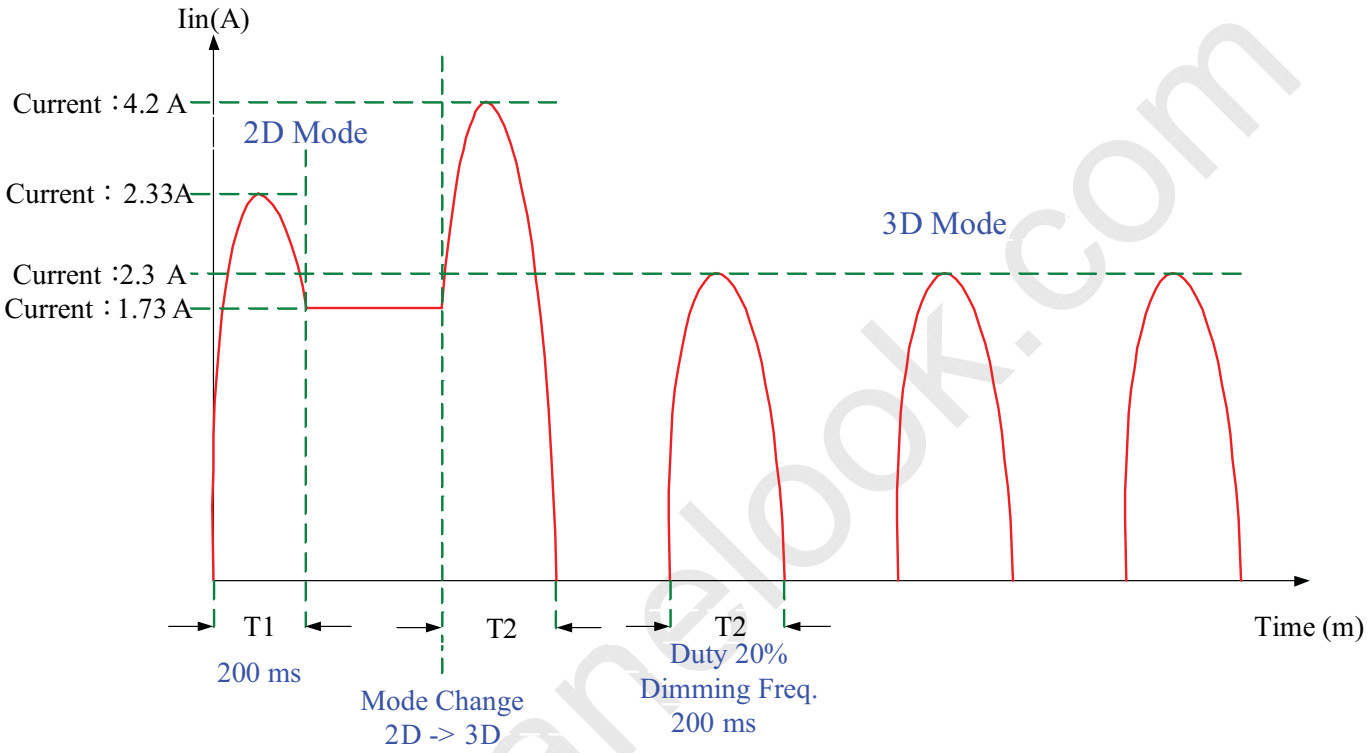
Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 30ms.

Note (4) 5% minimum duty ratio is only valid for electrical operation.

Note (5) FB and DMIN are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.

Test Condition: V_{BL}=22.8V, IL=100mA at 2D Mode/ IL=(300)mApeak at 3D Mode



3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V	Duty on	(5), (6)
	LO		—	0	—	0.8	V	Duty off	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)	
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V_{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us	(6)	
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms	(6)	
BLON Delay Time		T_{on}	—	300	—	—	ms		
		T_{on1}	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.2.

Note (6) EPWM is available only at 2D Mode.

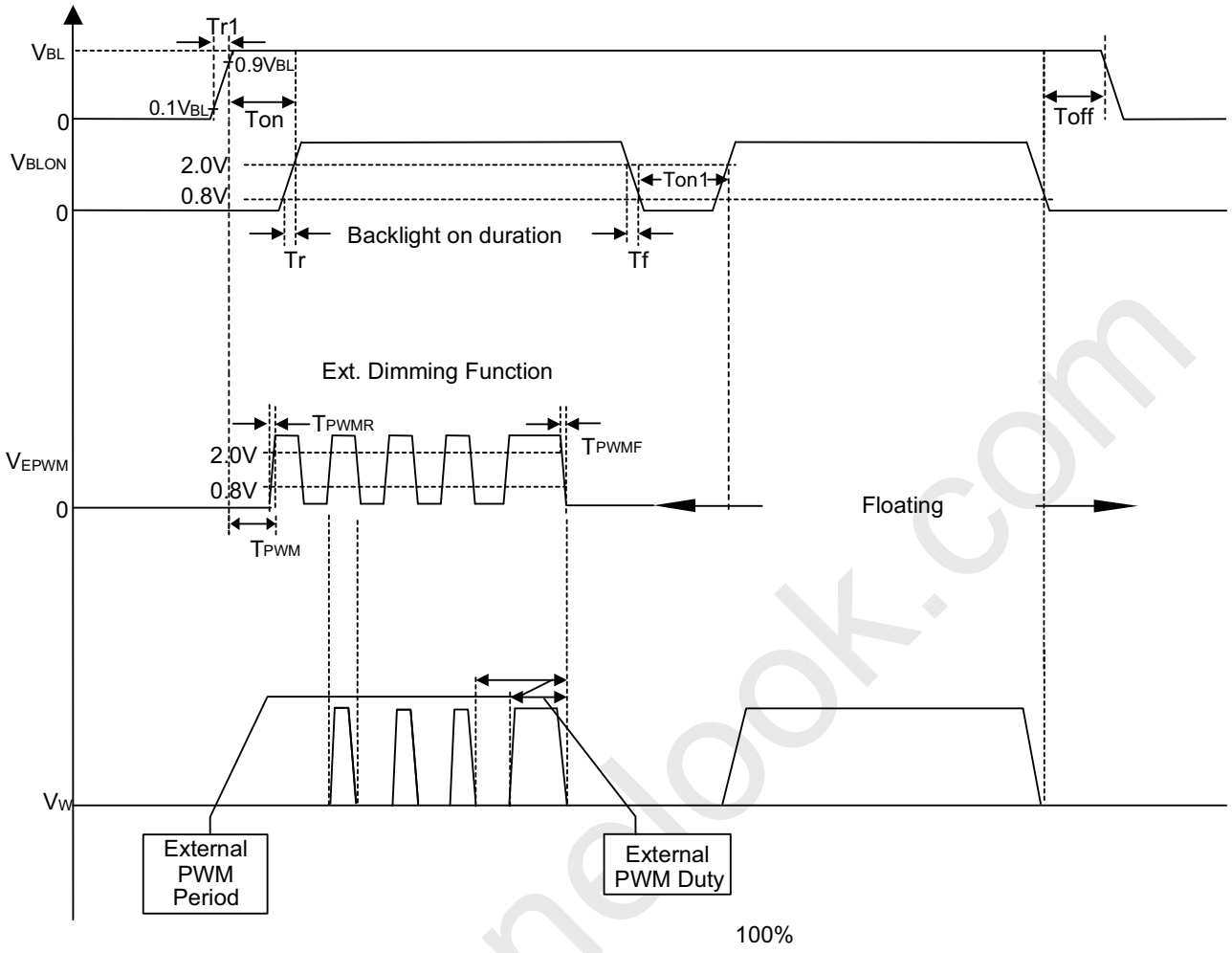


Fig. 1

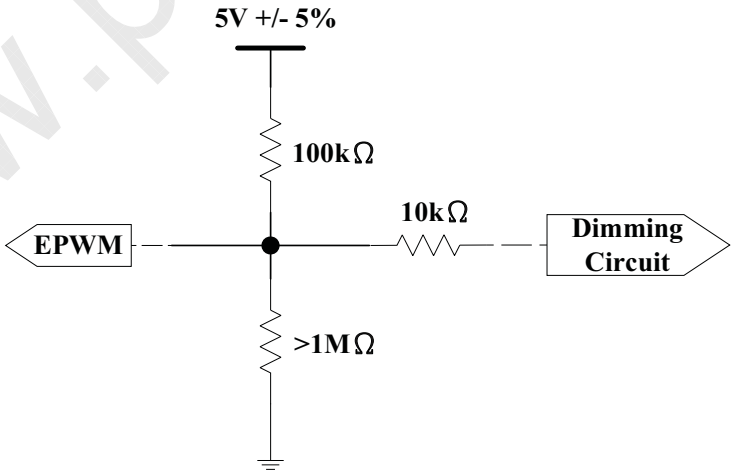
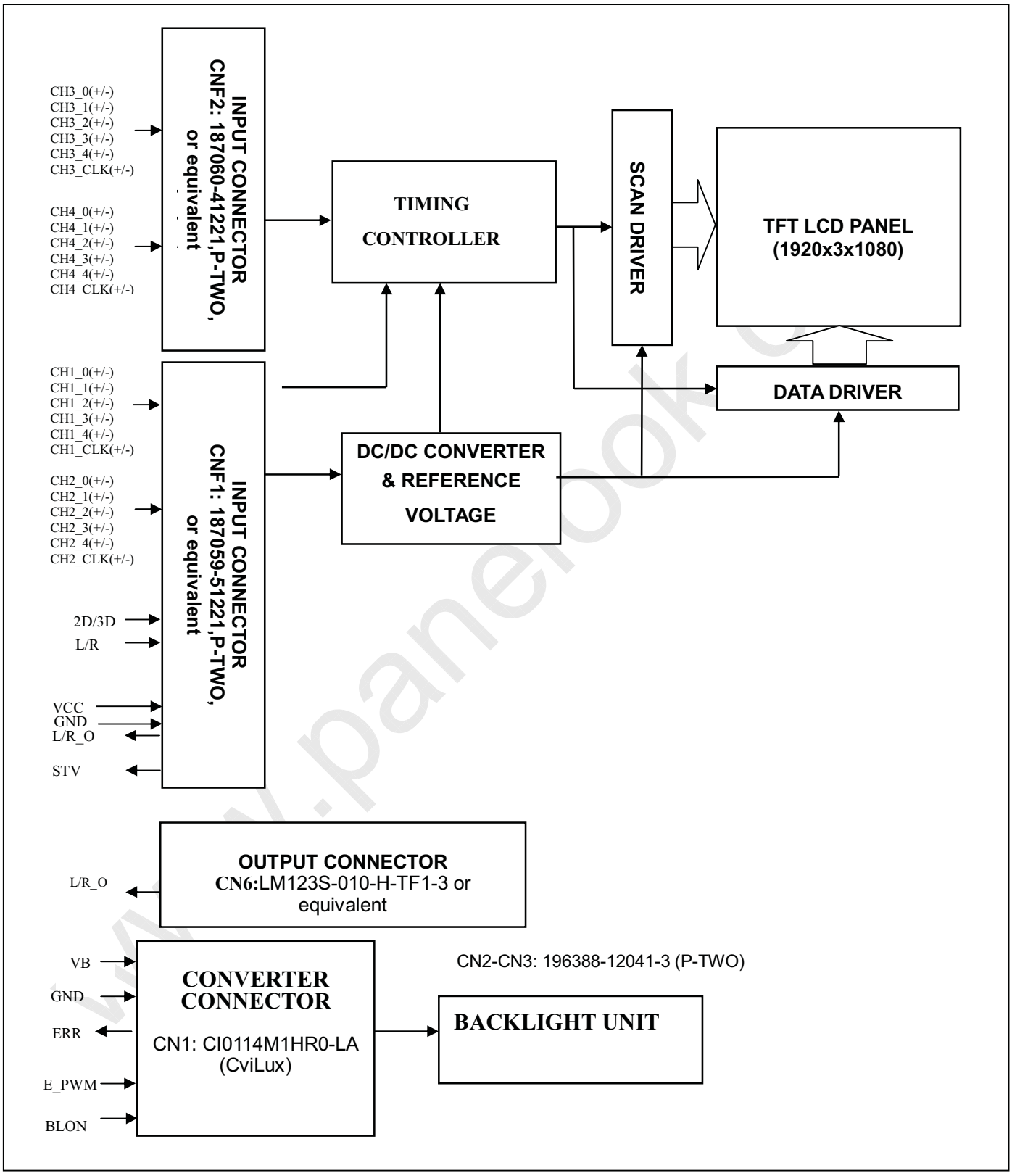


Fig. 2

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment: (187059-51221, P-TWO or equivalent)

Pin	Name	Description	Note
1	Vin	Power input (+12V)	
2	Vin	Power input (+12V)	
3	Vin	Power input (+12V)	
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	
6	N.C.	No Connection	(1)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	(6)
11	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
12	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
13	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
14	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
15	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH2CLK-	Second pixel Negative LVDS differential clock input.	(6)
18	CH2CLK+	Second pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	(6)
21	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
22	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
23	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	(6)
26	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
27	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
28	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
29	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
30	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	(6)
33	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
34	GND	Ground	
35	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	(6)

36	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	(6)
37	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
38	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	
42	2D/3D	Input signal for 2D/3D Mode Selection	(3)(5)
43	N.C.	No Connection	(1)
44	NC	No Connection	(1)
45	STV	Output signal from Tcon Real Vertical out for panel	
46	N.C.	No Connection	(1)
47	N.C.	No Connection	
48	L/R	Input signal for Left Right eye frame synchronous	(4) (5)
49	L/R_O	Output signal for Left Right Glasses control	(7)
50	N.C.	No Connection	
51	N.C.	No Connection	(1)

CNF2 Connector Pin Assignment (187060-41221(P-TWO) or equivalent)

Pin	Name	Description	Note
1	Vin	Power input (+12V)	
2	Vin	Power input (+12V)	
3	Vin	Power input (+12V)	
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	
6	N.C.	No Connection	(1)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	(6)
11	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
12	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
13	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
14	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
15	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH1CLK-	First pixel Negative LVDS differential clock input.	(6)
18	CH1CLK+	First pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	(6)
21	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	

22	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	(6)
23	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	(6)
26	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
27	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
28	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
29	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
30	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	CH3CLK-	Third pixel Negative LVDS differential clock input.	(6)
33	CH3CLK+	Third pixel Positive LVDS differential clock input.	
34	GND	Ground	
35	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	(6)
36	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
37	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
38	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	

CN6 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(7)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND or Open, H=Connect to +3.3V

SELLVDS	Note
L or Open	JEDIA Format
H	VESA Format

Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

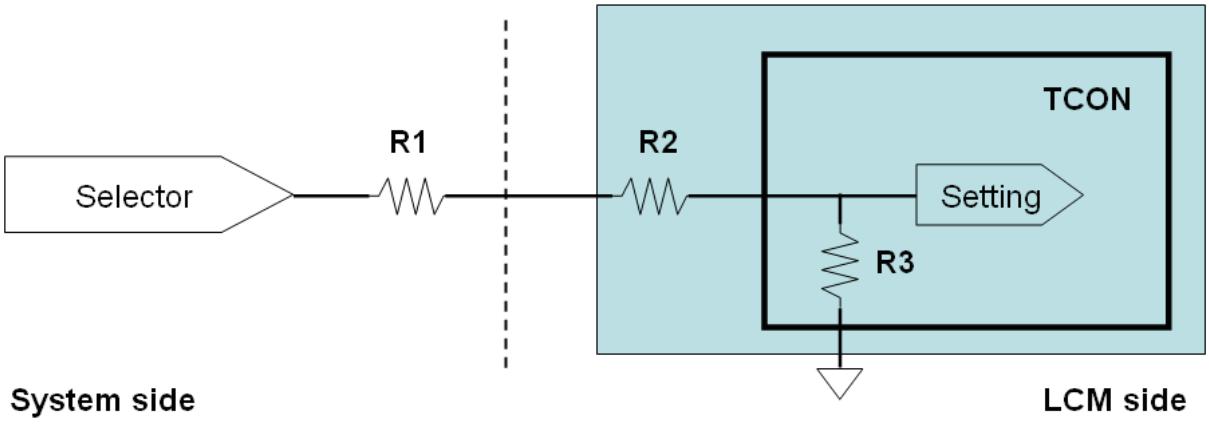
Note (4) Input signal for Left Right eye frame synchronous

V_{IL}=0~0.8 V, V_{IH}=2.0~3.3 V

L/R	Note
L	Right synchronous signal
H	Left synchronous signal

Note (5) 2D/3D, L/R signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



System side: R1 < 1K

Note (6) LVDS 4-port Data Mapping

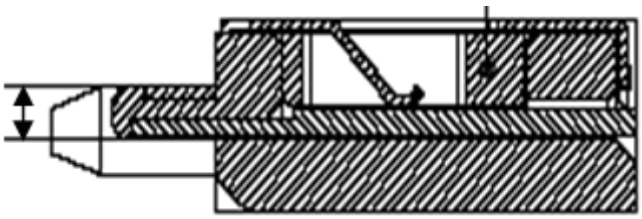
Port	Channel of LVDS	Data Stream
1st Port	Second Pixel	2, 6, 10, ….1914, 1918
2nd Port	Fourth Pixel	4, 8, 12, ….1916, 1920
3rd Port	First Pixel	1, 5, 9, ……1913, 1917
4th Port	Third Pixel	3, 7, 11, ….1915, 1919

Note (7) The definition of L/R_O signal as follows

L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

Note (8) LVDS connector mating dimension range request is 0.93mm~1.0mm as follow



5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2-CN3 (Housing): 196388-12041-3 (P-TWO) or equivalent

Pin №	Symbol	Feature
1	VLED-	Negative of LED String
2	VLED-	
3	VLED-	
4	VLED-	
5	VLED-	
6	VLED-	
7	NC	No Connection
8	NC	
9	NC	
10	NC	
11	VLED+	Positive of LED String
12	VLED+	

5.3 CONVERTER UNIT

CN1(Header): CI0114M1HR0-LA (CviLux)

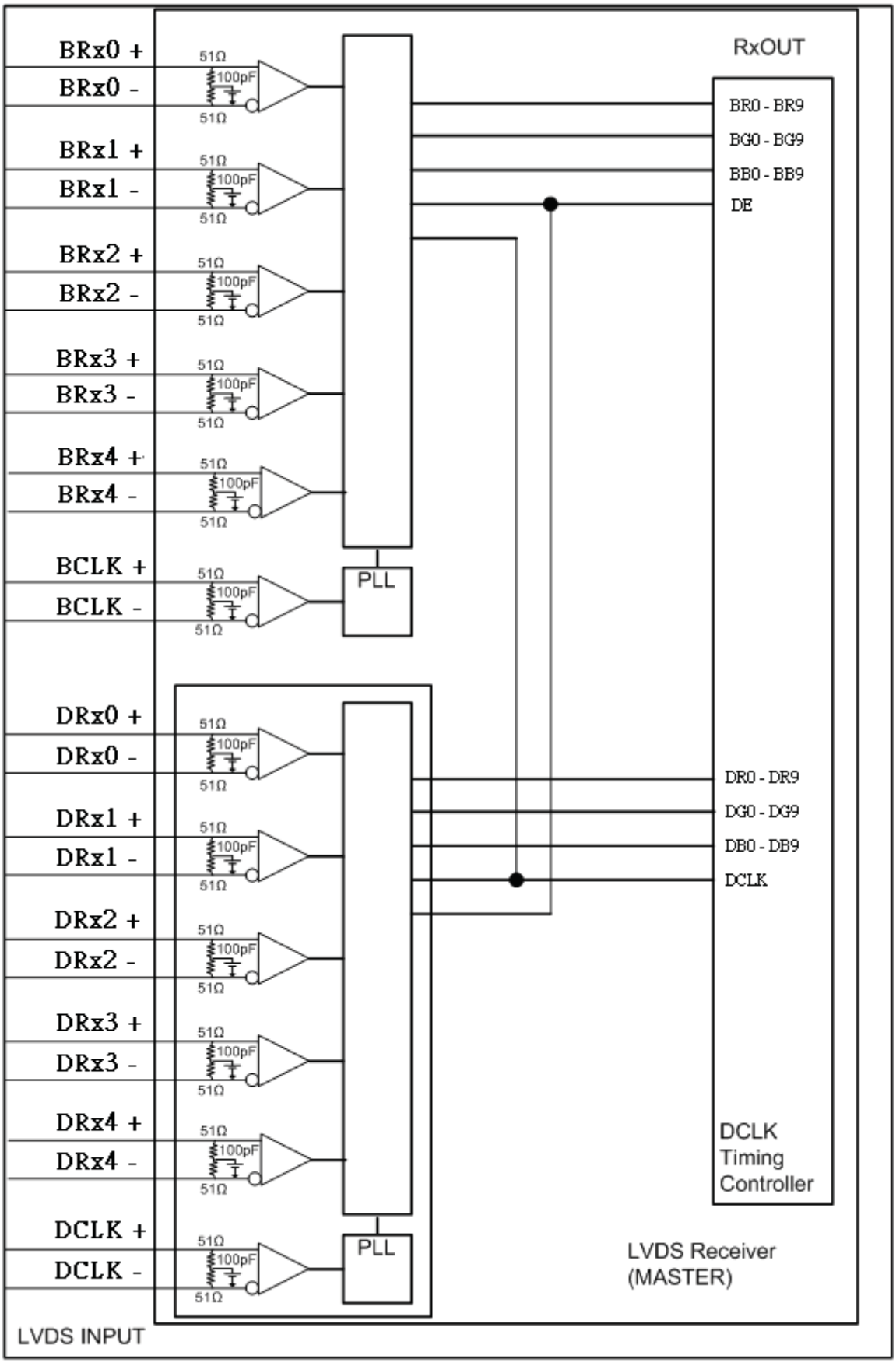
Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

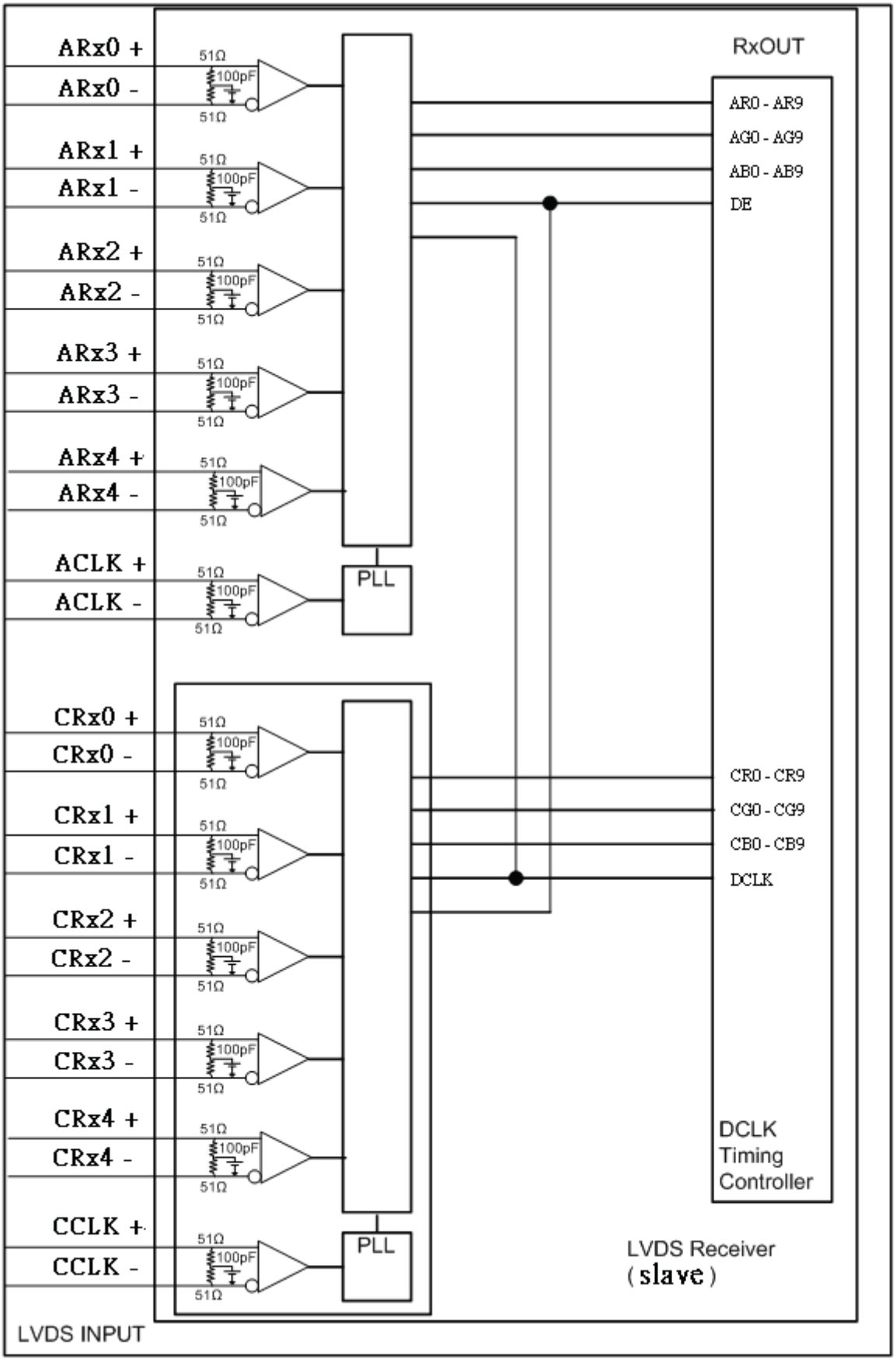
Notice (1) If Pin14 is open, E_PWM is 100% duty.

CN2 ~ CN3 : 196388-12041-3 (P-TWO)

Pin №	Symbol	Feature
1	VLED-	Negative of LED String
2	VLED-	
3	VLED-	
4	VLED-	
5	VLED-	
6	VLED-	
7	NC	No Connection
8	NC	
9	NC	
10	NC	
11	VLED+	Positive of LED String
12	VLED+	

5.4 BLOCK DIAGRAM OF INTERFACE





BR0~BR9	Second Pixel R Data	DR0~DR9	Fourth Pixel R data
BG0~BG9	Second Pixel G Data	DG0~DG9	Fourth Pixel G data
BB0~BB9	Second Pixel B Data	DB0~OB9	Fourth Pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

The third and fourth pixel are followed the same rules.

AR0~AR9	First Pixel R Data	CR0~CR9	Third Pixel R data
AG0~AG9	First Pixel G Data	CG0~CG9	Third Pixel G data
AB0~AB9	First Pixel B Data	CB0~CB9	Third Pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

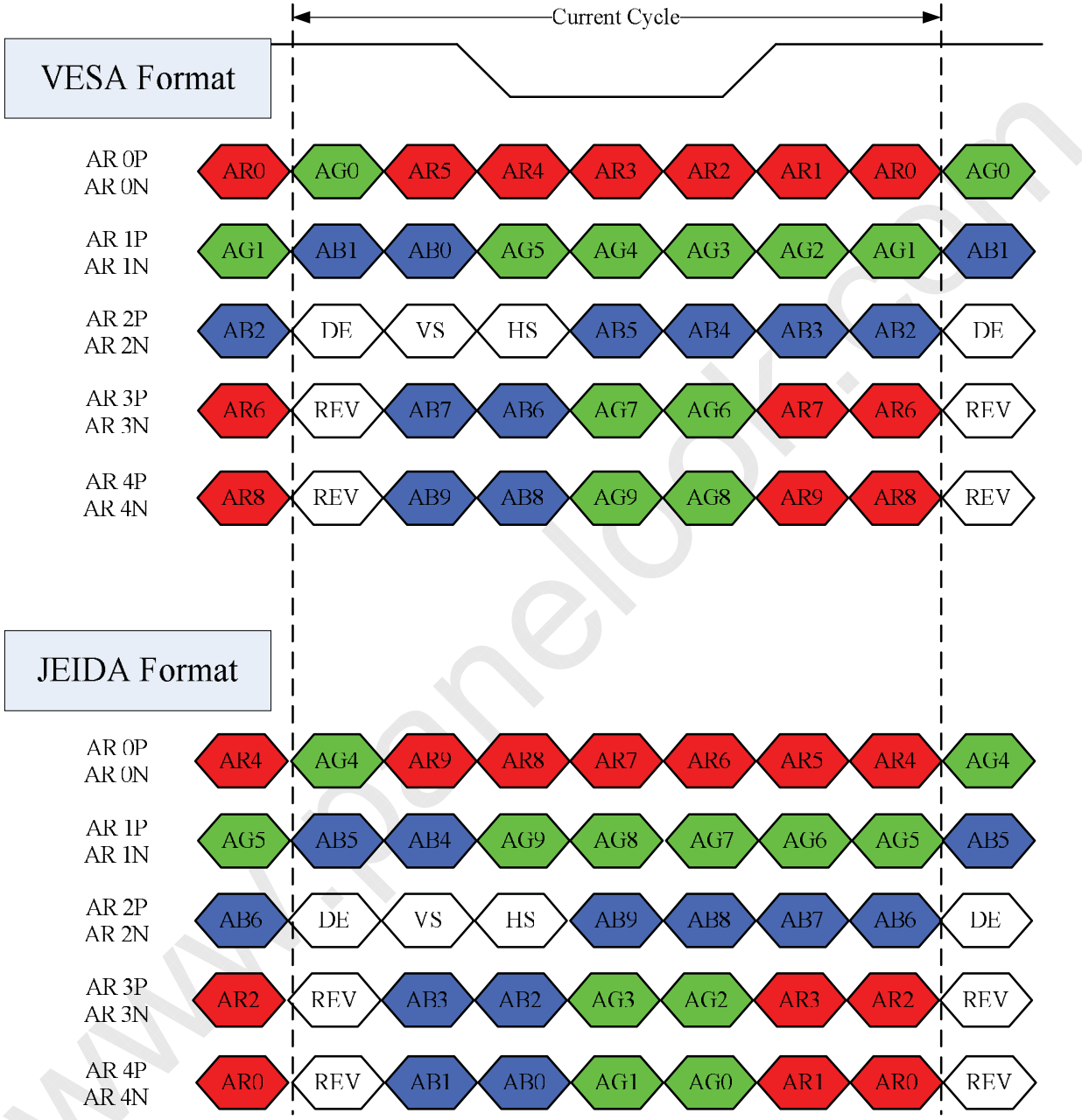
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

JEIDA Format : SELLVDS = L or Open

VESA Format : SELLVDS = H



AR0~AR9	First Pixel R Data (9; MSB, 0; LSB)	DE	Data enable signal
AG0~AG9	First Pixel G Data (9; MSB, 0; LSB)	DCLK	Data clock signal
AB0~AB9	First Pixel B Data (9; MSB, 0; LSB)	RSVD	Reserved

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	;	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1

	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	

6.1.1 Timing spec for Frame Rate = 100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	94	100	106	Hz	
	3D mode		F_{r5}	100	100	100	Hz	(7)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1350	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	–
		Blank	Tvb	10	270	315	Th	–
	3D Mdoe	Total	Tv	1350			Th	(6) (8)
		Display	Tvd	1080			Th	
		Blank	Tvb	270			Th	
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	–
		Blank	Thb	40	70	190	Tc	–
	3D Mdoe	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	–
		Blank	Thb	40	70	190	Tc	–

6.1.2 Timing spec for Frame Rate = 120Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	114	120	126	Hz	
	3D mode		F_{r6}	120	120	120	Hz	(7)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1125	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	45	315	Th	—
	3D Mdoe	Total	Tv	1125				(6)(8)
		Display	Tvd	1080				
		Blank	Tvb	45				
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—
	3D Mdoe	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—

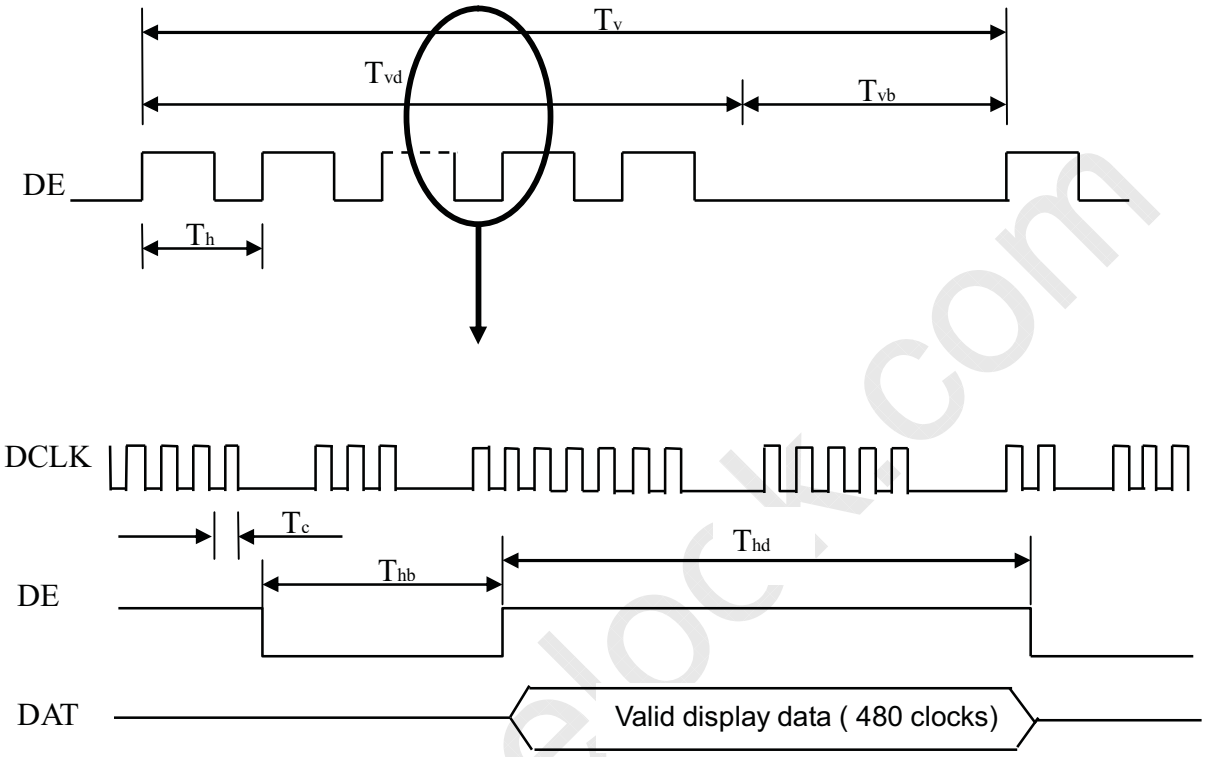
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

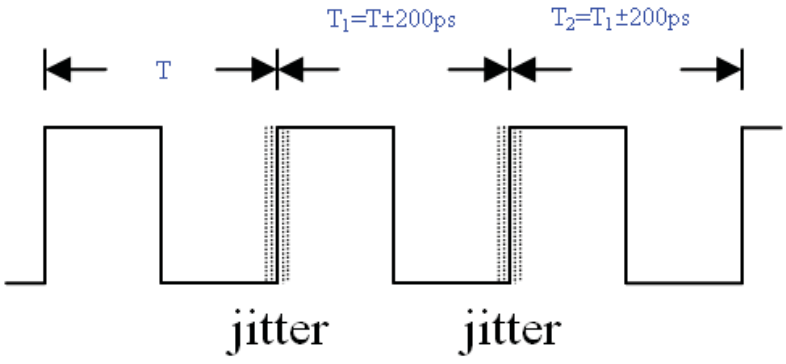
Fclkin(max) ≧ Fr6 × Tv × Th

Fr5 × Tv × Th ≧ Fclkin(min)

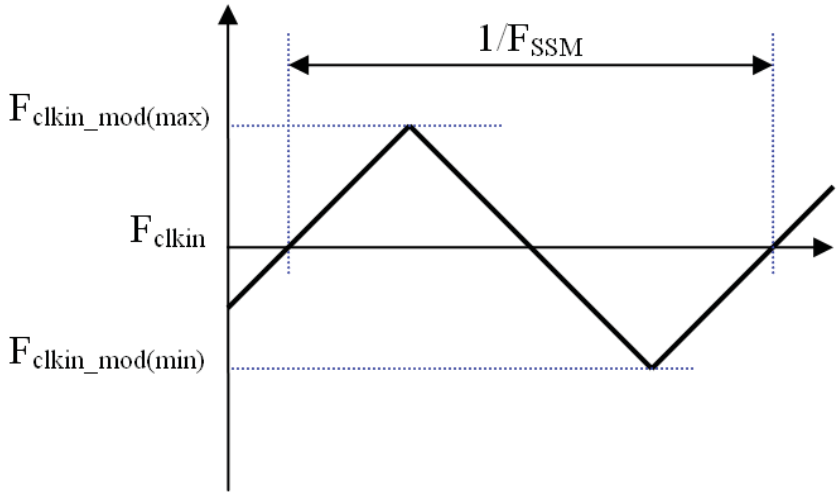
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T1 – TI

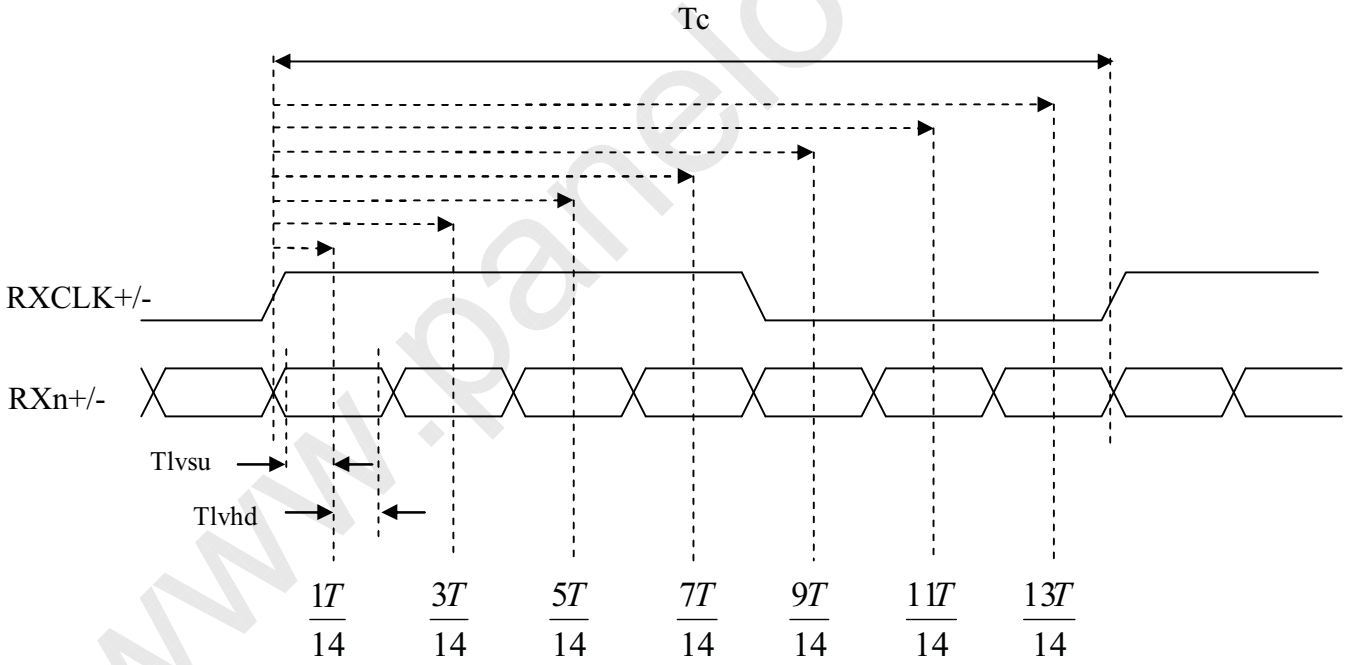


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) Please fix the Vertical timing (Vertical Total =1350 / Display =1080 / Blank = 270) in 100Hz 3D mode and Vertical timing (Vertical Total =1125 / Display =1080 / Blank = 45) in 120Hz 3D mode.

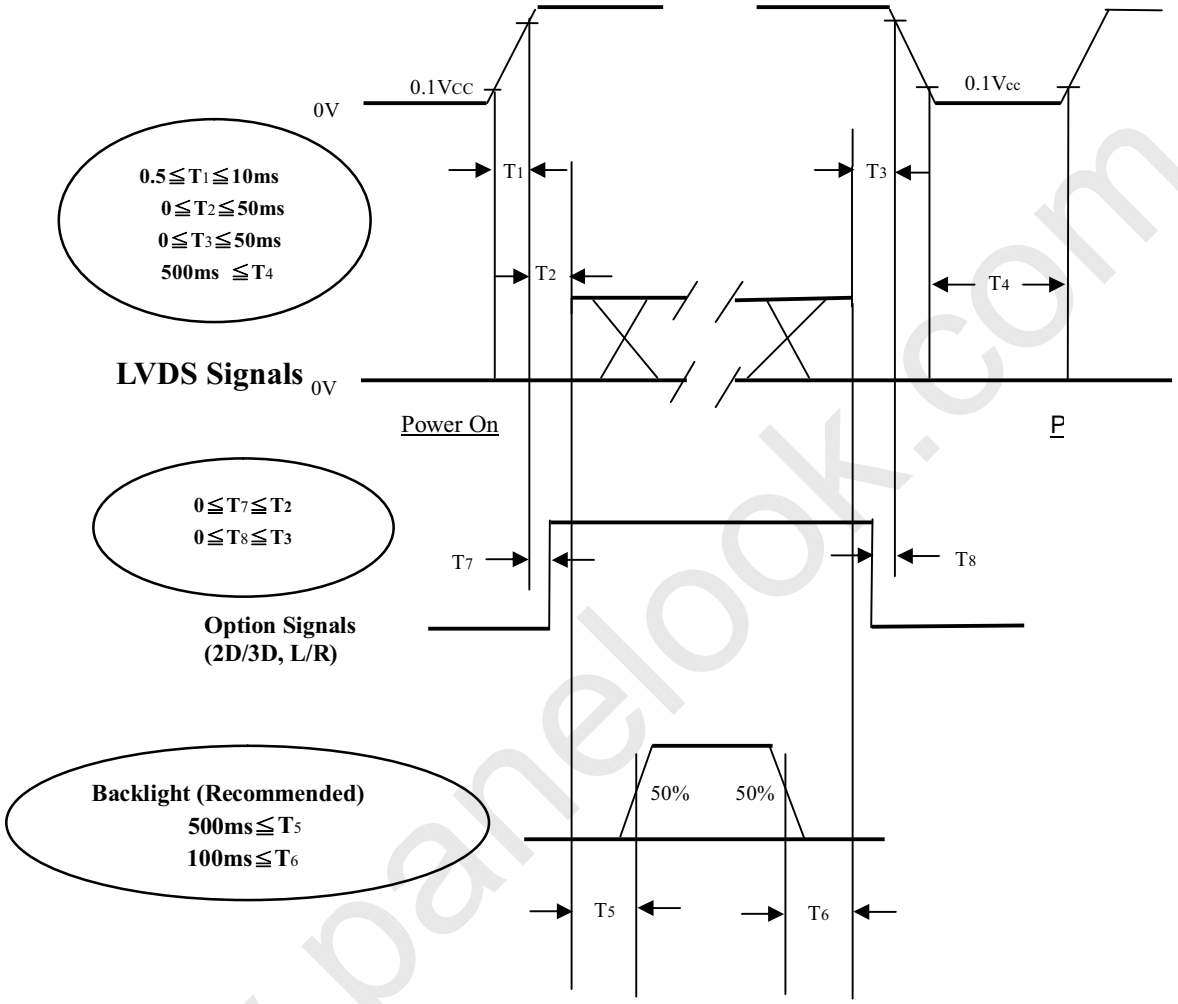
Note (7) In 3D mode, the set up Fr5 and Fr6 in Typ. ±3 HZ .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

Note (8) In 3D mode, the set up Tv and Tvb in Typ. ±30.In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

6.2 POWER ON/OFF SEQUENCE

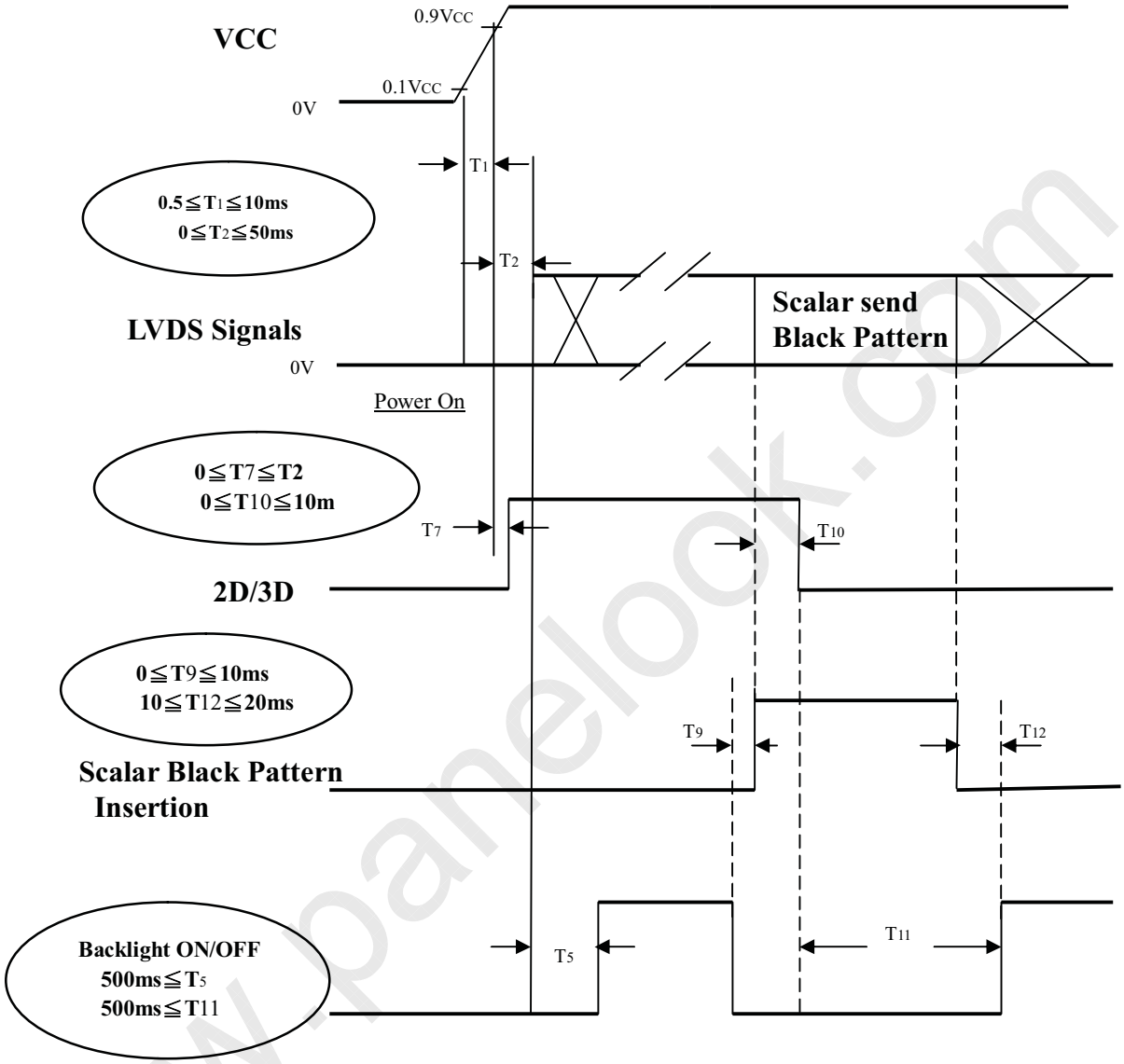
6.2.1 POWER ON/OFF SEQUENCE(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

6.2.2 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

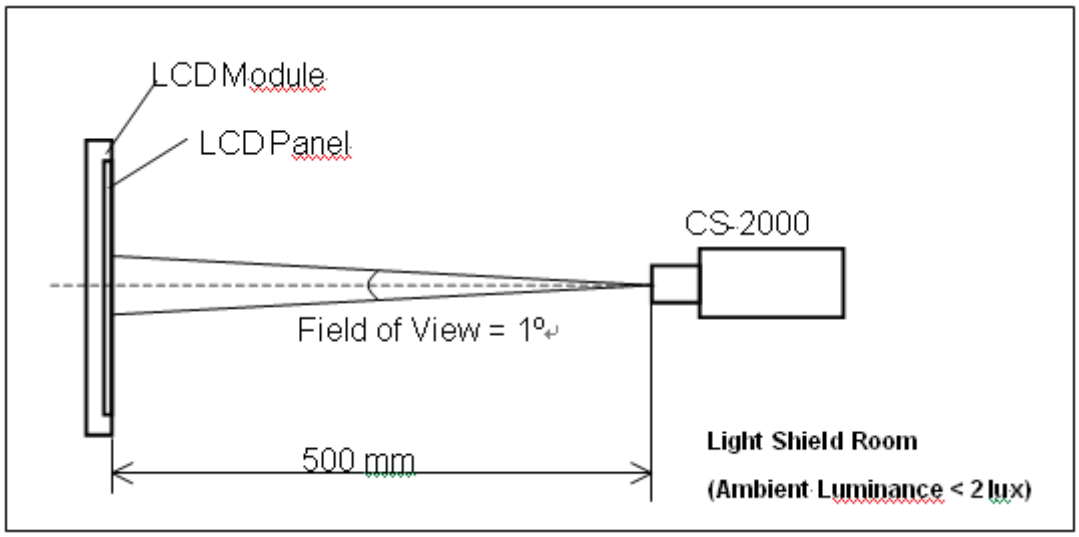
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	100	mA
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



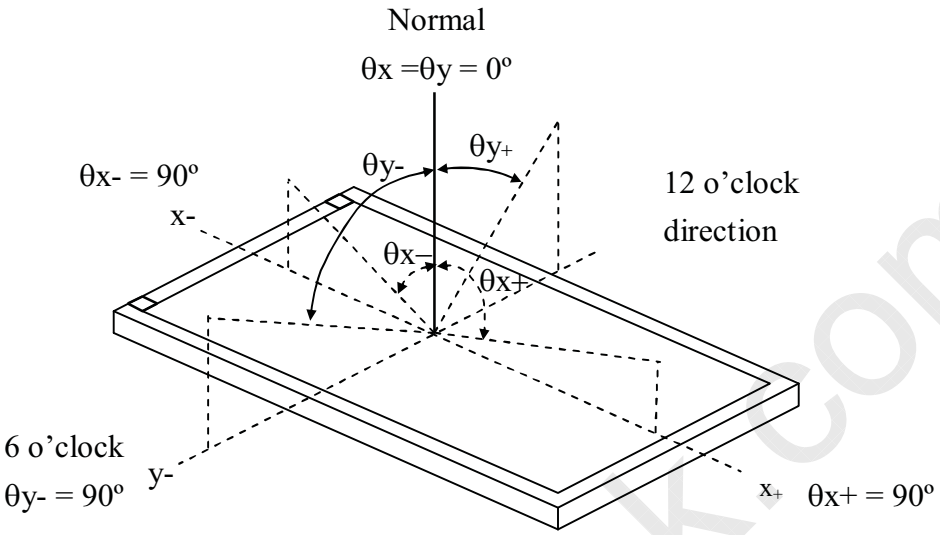
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		θx=0°, θy =0° Viewing angle at normal direction	3500	5000	-	-	(2)
Response Time (VA)		Gray to gray			-	6	12	ms	(3)
Center Luminance of White		L_C	2D		320	400	-	cd/m^2	(4)
			3D		-	60	-	cd/m^2	(8)
White Variation		δW			-	-	1.3	-	(6)
Cross Talk		CT	2D		-	-	4	%	(5)
			3D-W		-	4	-	%	(8)
			3D-D		-	11	-	%	(8)
Color Chromaticity	Red	Rx			Typ. -0.03	0.636	Typ. +0.03	-	-
		Ry				0.334		-	
	Green	Gx				0.296		-	
		Gy				0.601		-	
	Blue	Bx				0.152		-	
		By				0.054		-	
	White	Wx				0.280		-	
		Wy				0.290		-	
	Correlated color temperature				-	10000	-	K	-
	Color Gamut	C.G.			-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+		CR≥20	80	88	-	Deg.	(1)
		θx-			80	88	-		
	Vertical	θy+			80	88	-		
		θy-			80	88	-		
Transmission direction of the up polarizer		$Φ_{up}$		-	-	90	-	Deg.	(7)

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

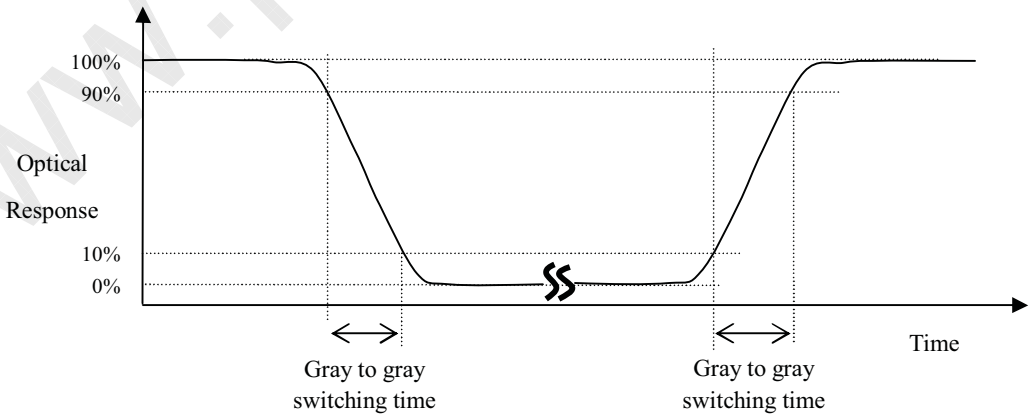
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (4) Definition of Luminance of White (LC):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

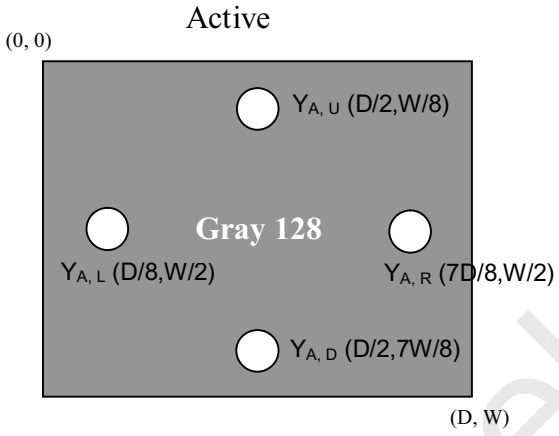
Note (5) Definition of Cross Talk (CT):

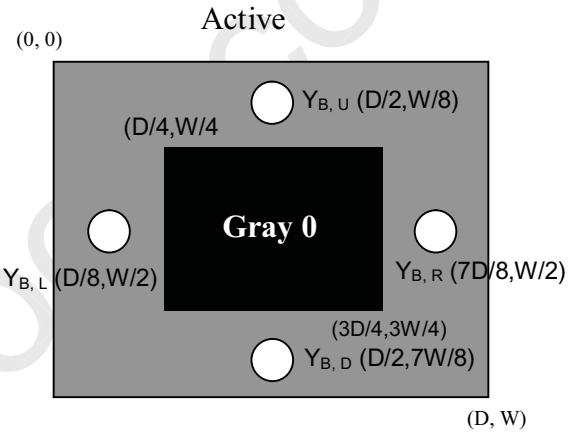
CT = $| Y_B - Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

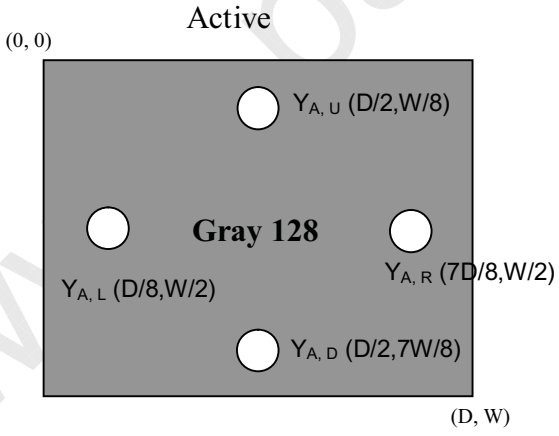
Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)

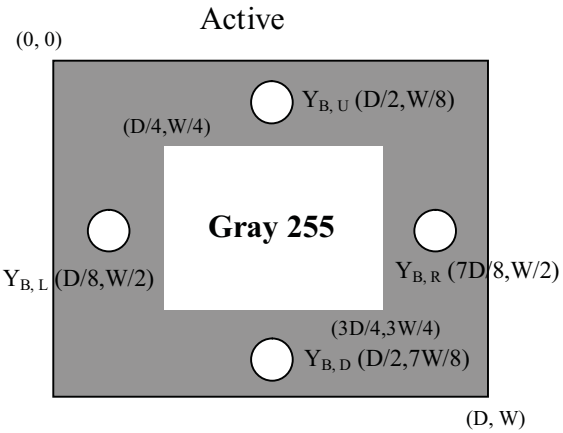




Y_A = Luminance of measured location without gray level 255 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m2)

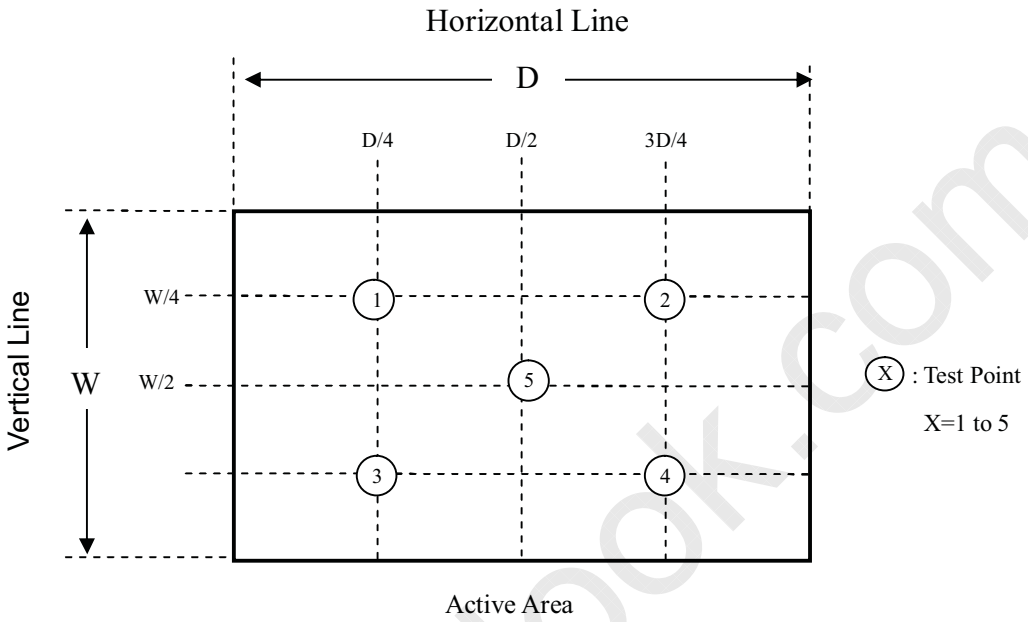




Note (6) Definition of White Variation (δW):

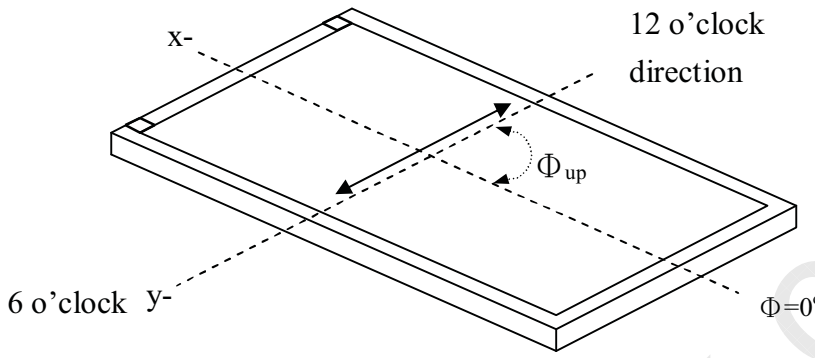
Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

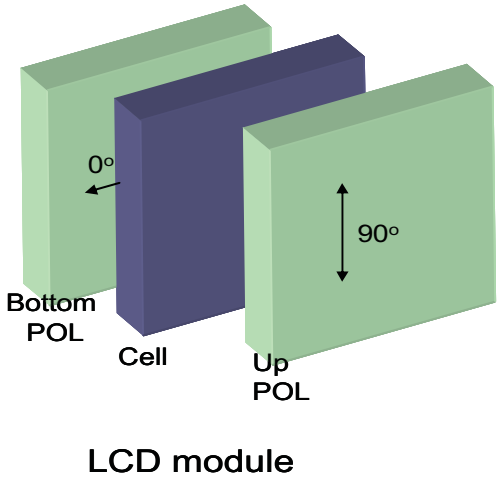


Note (7) This is a reference for designing the shutter glasses of 3D application. (VA)

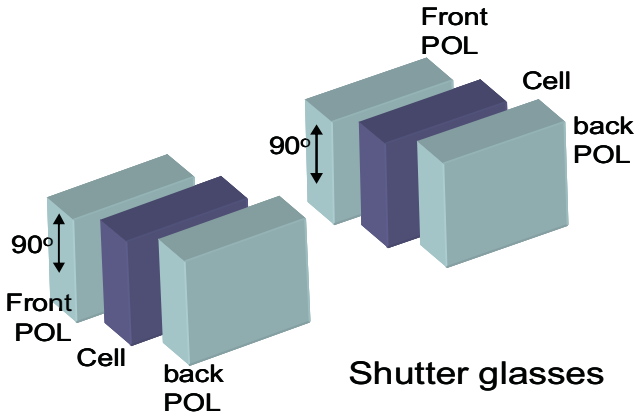
Definition of the transmission direction of the up polarizer:



The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



LCD module

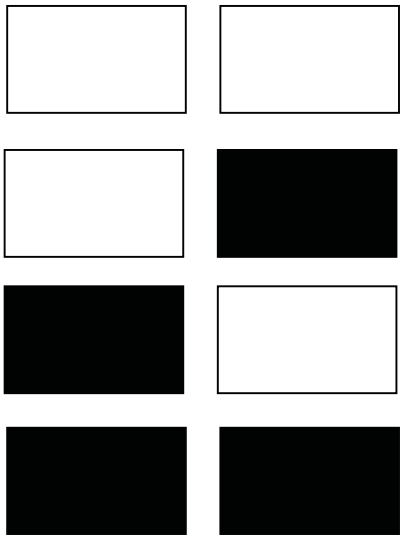


Shutter glasses

Note (8) Definition of the 3D mode performance (measured under 3D mode, use CMI's shutter glass):

a. Test pattern

Left eye image and right eye image are displayed alternated



WW

Left eye image: W255; Right eye image: W255

WB

Left eye image: W255; Right eye image: W0

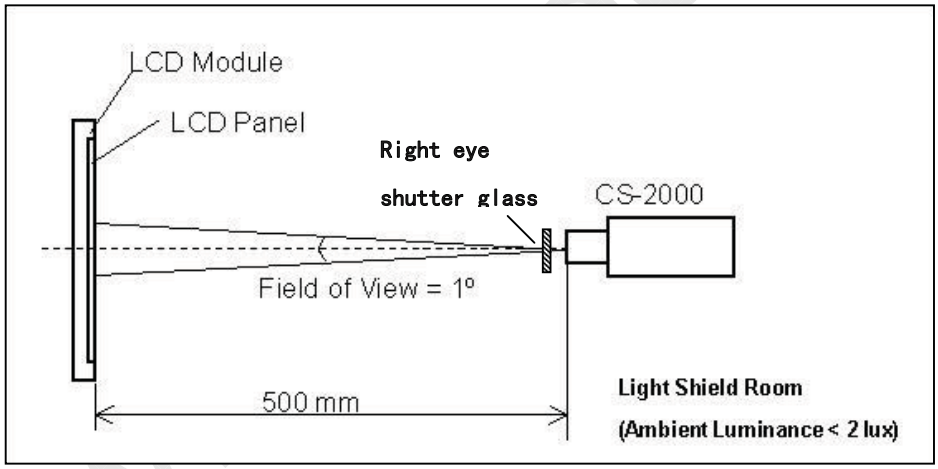
BW

Left eye image: W0; Right eye image: W255

BB

Left eye image: W0; Right eye image: W0

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation. The luminance of the test pattern "WW", denoted L(WW); the luminance of the test pattern "WB", denoted L(WB); the luminance of the test pattern "BW", denoted L(BW); the luminance of the test pattern "BB", denoted "L(BB)

c. Definition of the Center Luminance of White, Lc (3D) : L(WW)

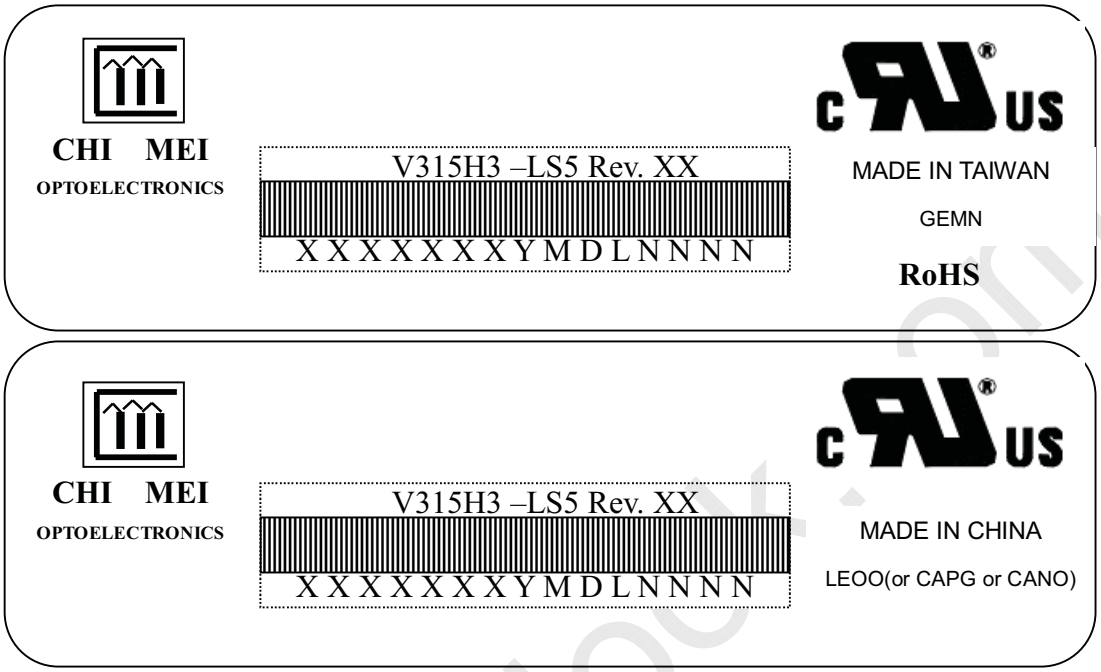
d. Definition of the 3D mode white crosstalk, CT (3D-W) : $CT(3D-W) \equiv \left| \frac{L(WB)-L(BB)}{L(WW)-L(BB)} \right|$

e. Definition of the 3D mode dark crosstalk, CT (3D-D) : $CT(3D-D) \equiv \left| \frac{L(WW)-L(BW)}{L(WW)-L(BB)} \right|$

8. DEFINITION OF LABELS

8.1 CMI MODULE LABEL

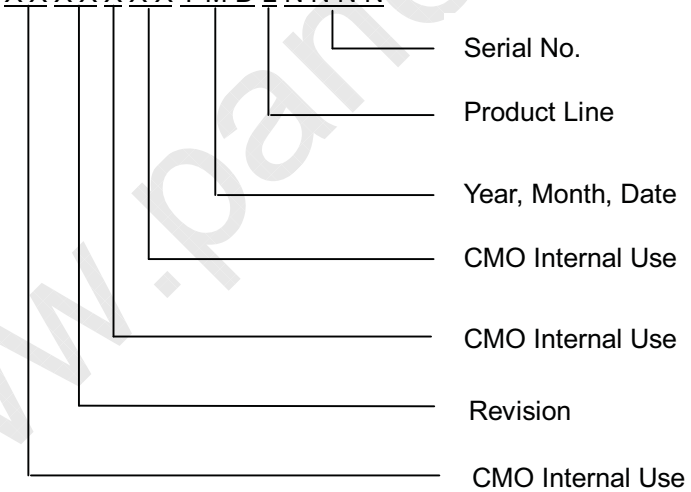
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V315H3-LS5

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 2001=1, 2002=2, 2003=3, 2004=4….2010=0, 2011=1, 2012=2....

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 6 LCD TV modules / 1 Box

(2) Box dimensions : 826(L)x376(W)x540(H)mm

(3) Weight : Approx. 30 Kg(6 modules per carton)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

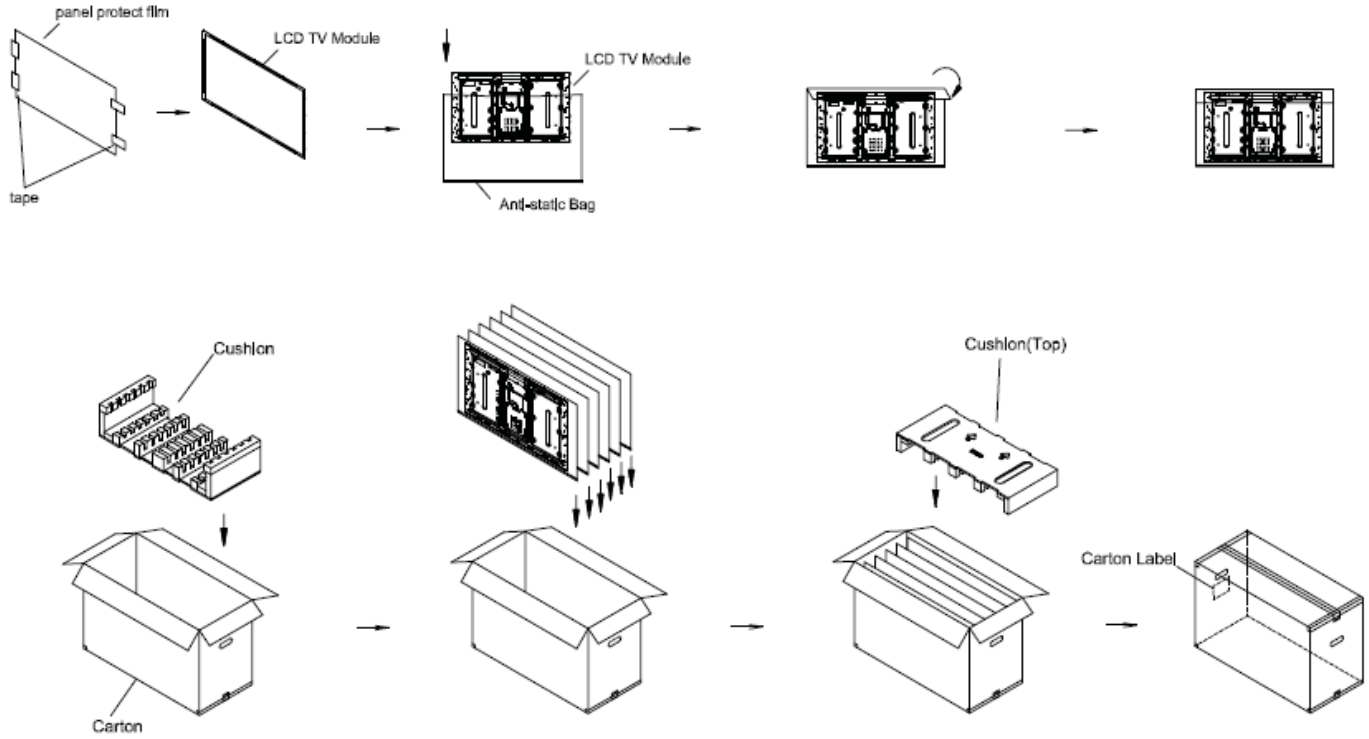


Figure.9-1 packing method

Sea / Land Transportation
(40ft Container)

Air Transportation

Sea / Land Transportation
(40ft HQ Container)

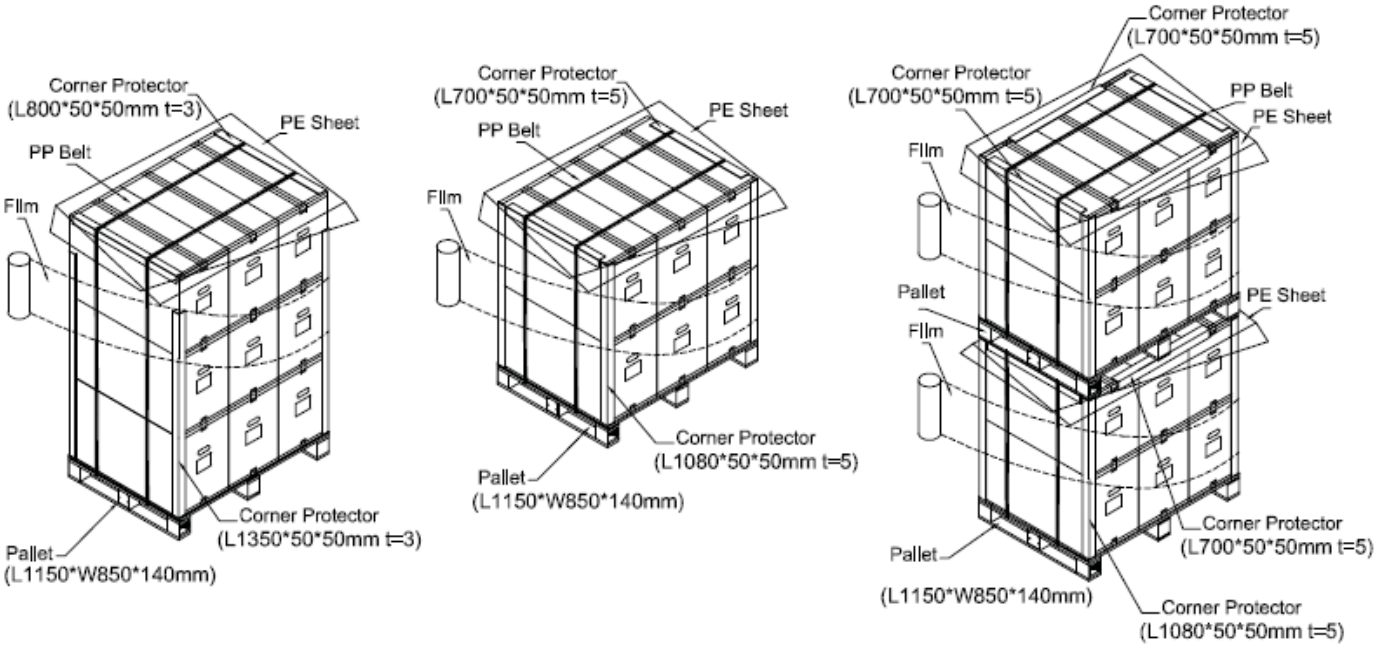


Figure.9-2 packing method

10. International Standard

10.1 Safety

(1) UL 60950-1, UL 60065: Standard for Safety of Information Technology Equipment Including electrical Business Equipment.

(2) IEC 60950-1:2005, IEC 60065:2001+ A1:2005 ; Standard for Safety of International Electrotechnical Commission.

(3) EN 60950-1:2006+ A11:2009, EN60065:2002 + A1:2006 + A11:2008; European Committee for Electrotechnical Standardization (CENELEC), EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

10.2 EMC

(1) ANSI C63.4 Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHZ. " American National standards Institute(ANSI)

(2) C.I.S.P.R "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment. " International Special committee on Radio Interference.

(3) EN 55022 "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment. "European Committee for Electortechnical Standardization.(CENELEC)

11. PRECAUTIONS

11.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED light bar will be higher than that of room temperature.

11.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the converter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

12. MECHANICAL CHARACTERISTICS