☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: V315H3
SUFFIX: PE6

Customer:

APPROVED BY **SIGNATURE**

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Vincent Chou	Wayne Lin

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Oct. 15, 2010	All	All	The approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315H3-PE6 is a 31.5" TFT Liquid Crystal Display product with driver ICs and 2ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit). The backlight unit is not built in.

1.2 FEATURES

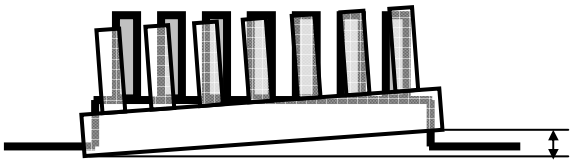
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	31.5
Pixels [lines]	1920 × 1080
Active Area [mm]	698.4(H) × 392.85(V)
Sub-Pixel Pitch [mm]	0.12125(H) × 0.36375(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 1150g
Physical Size [mm]	712.89(W) × 434.3(H) × 1.79(D) Typ.
Display Mode	Transmissive mode / Normallly black
Contrast Ratio	5000:1 Typ. (Typical value measure at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H), +88/-88(V) Typ. (CR≧20) (Typical value measure at CMI's module)
Color Chromaticity	R = (0.652, 0.325) G = (0.258, 0.586) B = (0.134, 0.106) W= (0.292, 0.337) * Please refer to "color chromaticity" on p.24
Cell Transparency [%]	4.4%
Polarizer Surface Treatment	Anti-Glare coating (Haze 11%), Hard coating (3H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	1100	1150	1200	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)

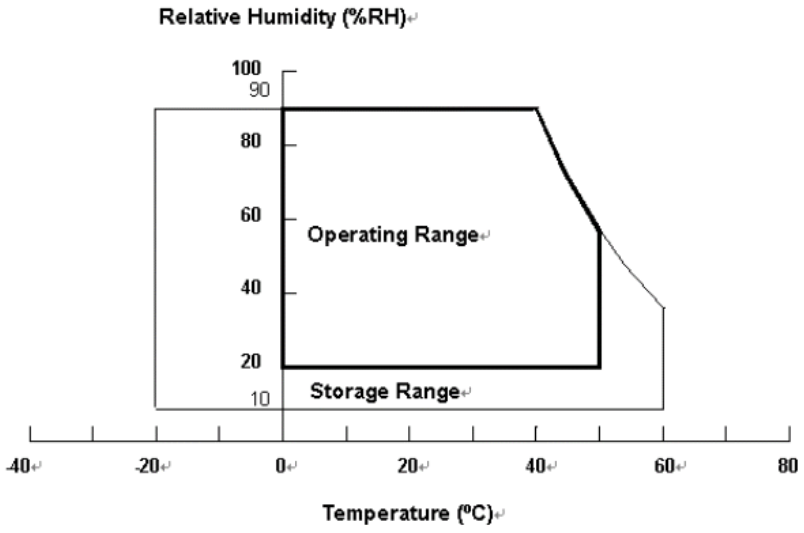
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Recommended Storage Condition: With shipping package.

Recommended Storage temperature range: 25±5 _

Recommended Storage humidity range: 50±10%RH

Recommended Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT OPEN CELL

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Voltage for gate driver	VGH	-0.3	40	V	
Voltage for gate driver	VGL	-20	0.3	V	
Voltage range for gate driver	VGH - VGL	-0.3	43	V	
Voltage for data diver	VAA	12	18	V	
Logic Input Voltage	VIN	-0.3	5	V	

3. ELECTRICAL CHARACTERISTICS

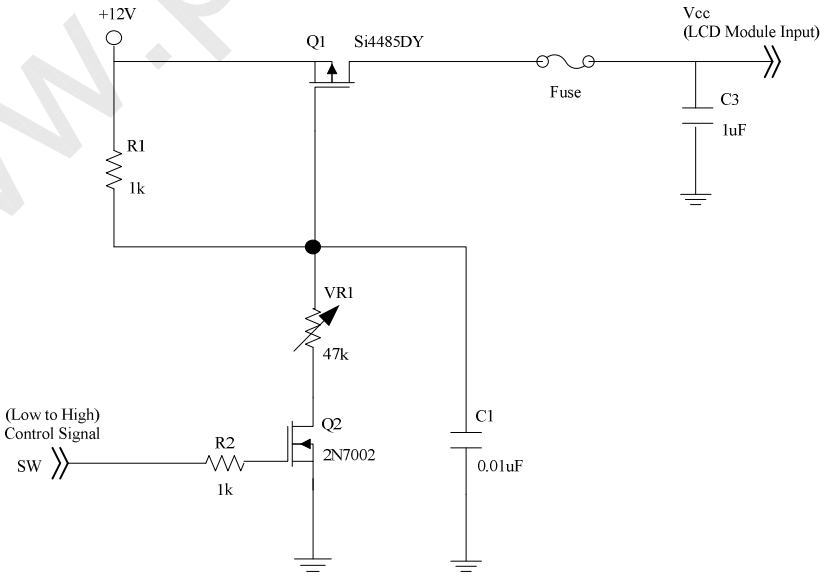
3.1 TFT LCD Module

(Ta = 25 ± 2 ºC)

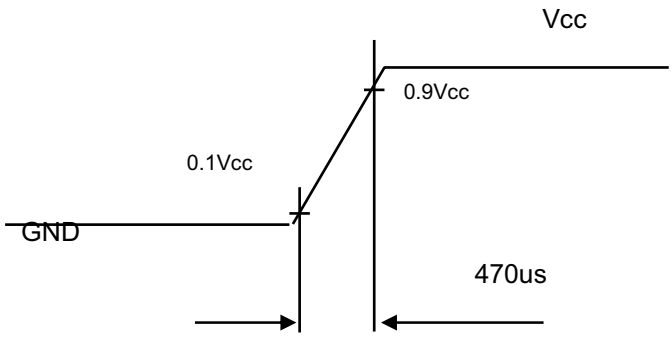
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	–	–	2.8	A	(2)
Power Supply Current	White Pattern	–	–	0.38	–	A	(3)
	Black Pattern	–	–	0.3	0.39	A	
	Horizontal Stripe	–	–	0.58	0.62	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	–	–	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	–	–	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	–	600	mV	
	Terminating Resistor	R_T	–	100	–	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	–	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	–	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

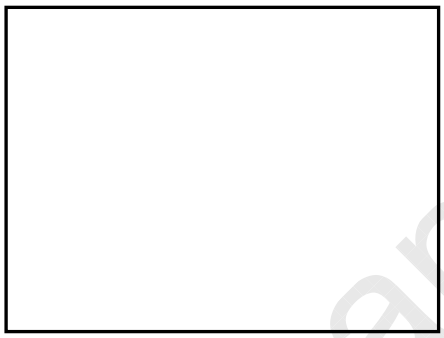


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

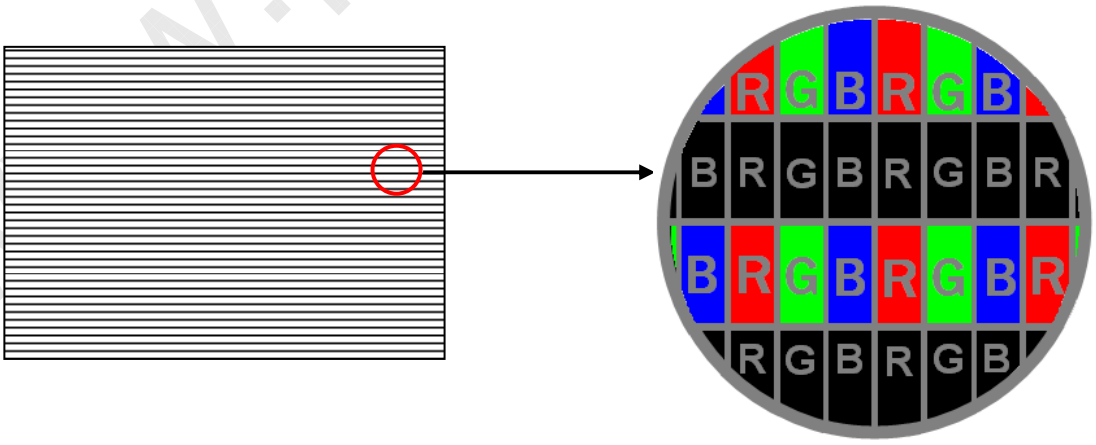


Active Area

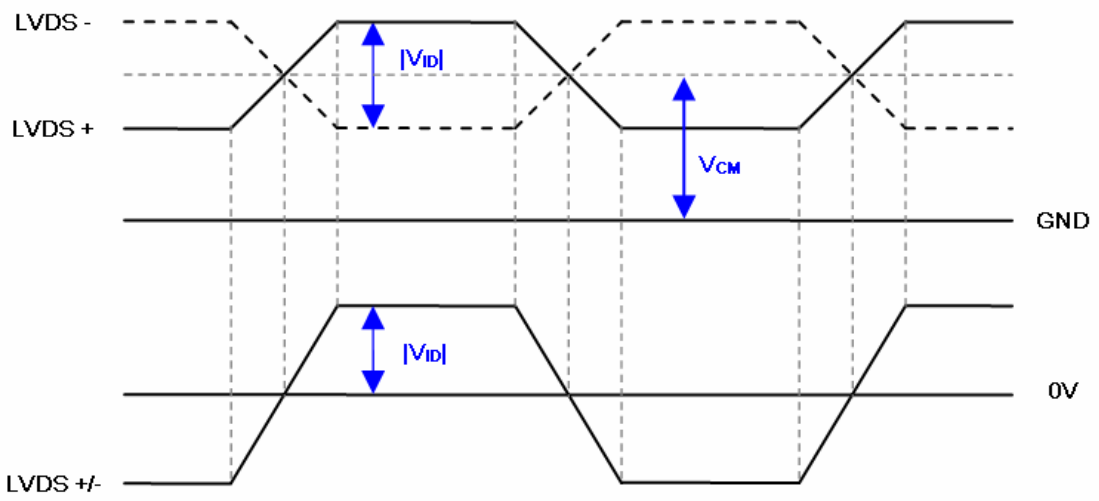
b. Black Pattern

Active Area

c. Horizontal Pattern

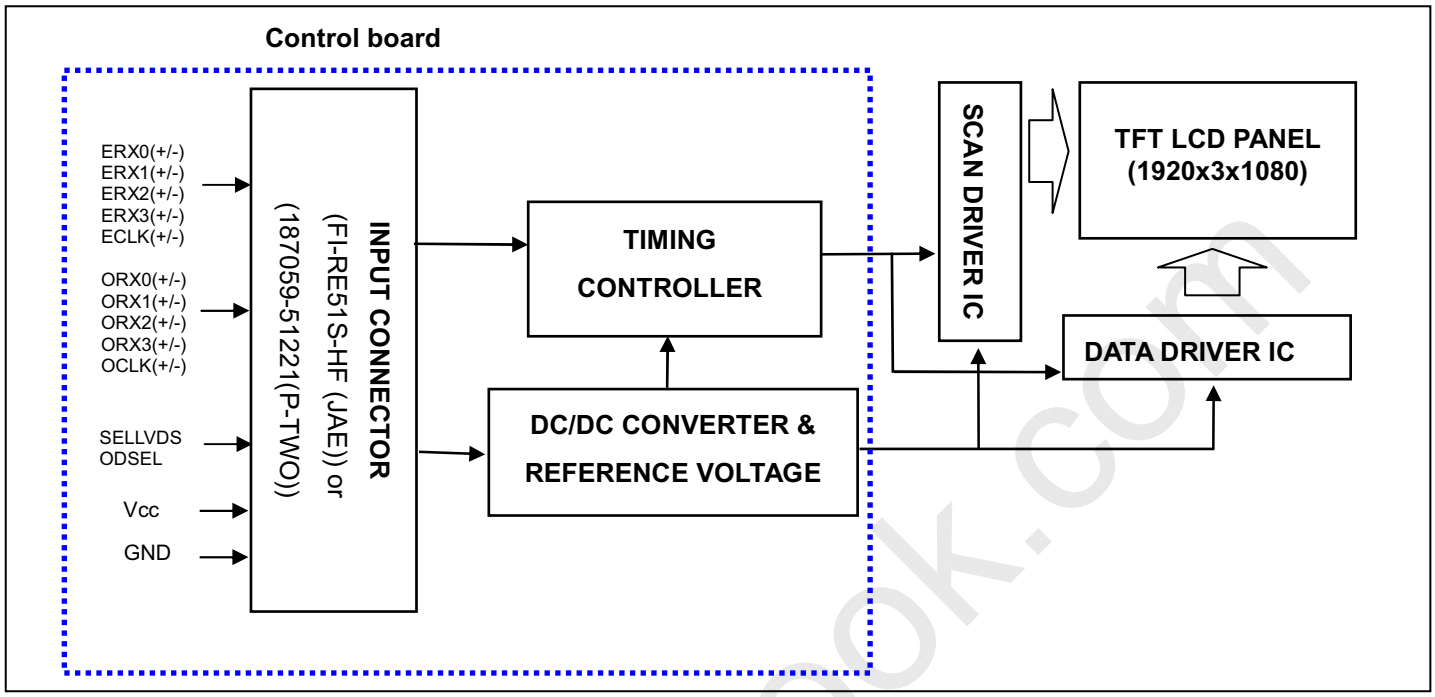


Note (4) The LVDS input characteristics are as follows :



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD OPEN CELL



5. INPUT TERMINAL PIN ASSIGNMENT

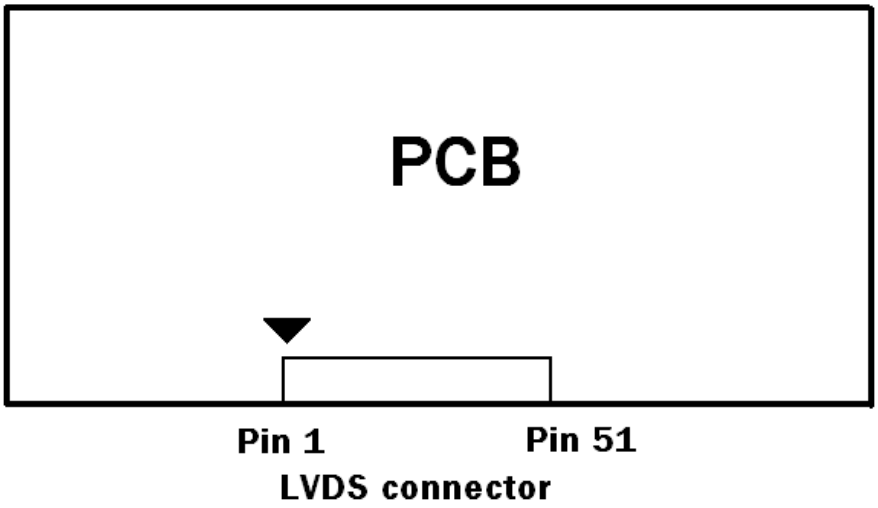
5.1 TFT LCD OPEN CELL INPUT

CNF1 Connector Pin Assignment

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	N.C.	No Connection	(2)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	(7)
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input	(7)
18	OCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(7)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(2)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	(7)
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input.	(7)
33	ECLK+	Even pixel Positive LVDS differential clock input.	
34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(7)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(2)
38	N.C.	No Connection	
39	GND	Ground	
40	SCL	EEPROM Serial Clock (for auto Vcom)	
41	SDA	EEPROM Serial Data (for auto Vcom)	
42	N.C.	No Connection	(2)
43	WP	EEPROM Write Protection (for auto Vcom) (0V~0.7V/Open→Disable, 2.7V~3.3V→Enable)	
44	N.C.	No Connection	(2)
45	SELLVDS	LVDS data format selection (2.7V~3.3V/Open→VESA, 0V~0.7V→JEIDA).	(3)(5)
46	OD_SEL	Overdriving lookup table selection	(4)(6)

47	N.C.	No Connection	(2)
48	TST_AGE	Do not need external clock when AGEN mode enabled. Test aging (0V~0.7V/Open→Disable, 2.7V~3.3V→Enable)	
49	N.C.	No Connection	
50	TCON_RDY	T-CON ready output signal	
51	N.C.	No Connection	(2)

Note (1) LVDS connector pin order defined as follows



Note (2) Reserved for internal use. Please leave it open.

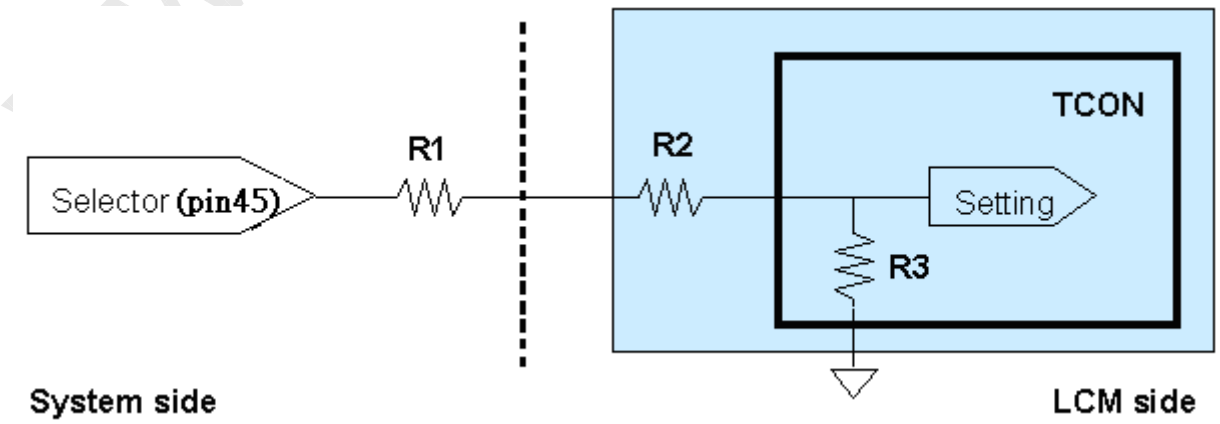
Note (3) Low = Open or connect to GND: JEIDA Format, High = Connect to +3.3V: VESA Format.

Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

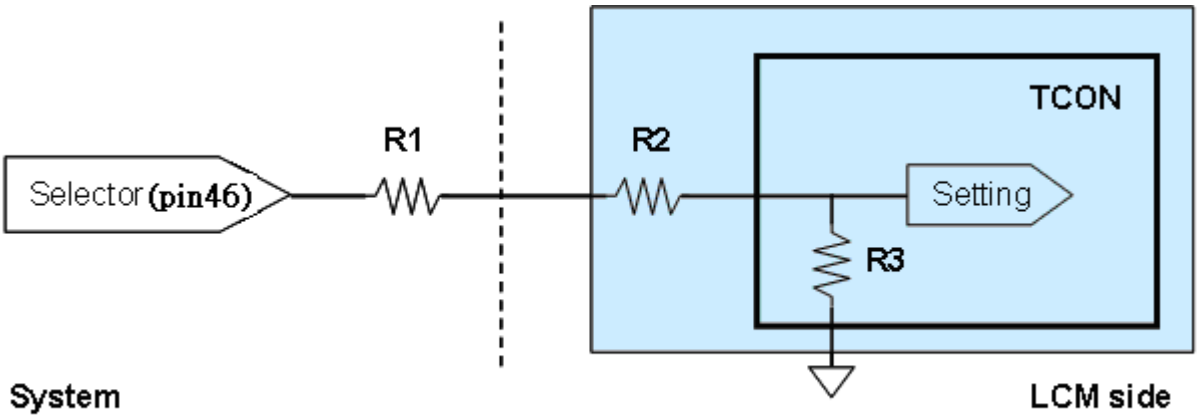
Low = Open or connect to GND, High = Connect to +3.3V

ODSEL	Note
L or open	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (5) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)

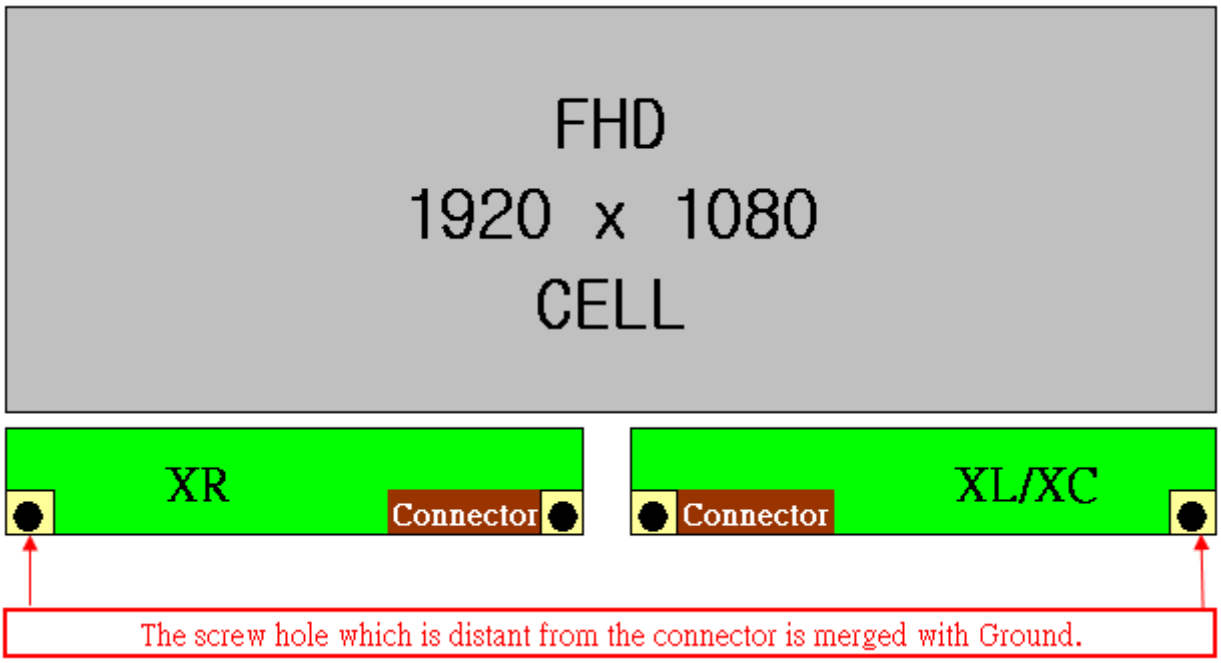


Note (6) ODSEL signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)

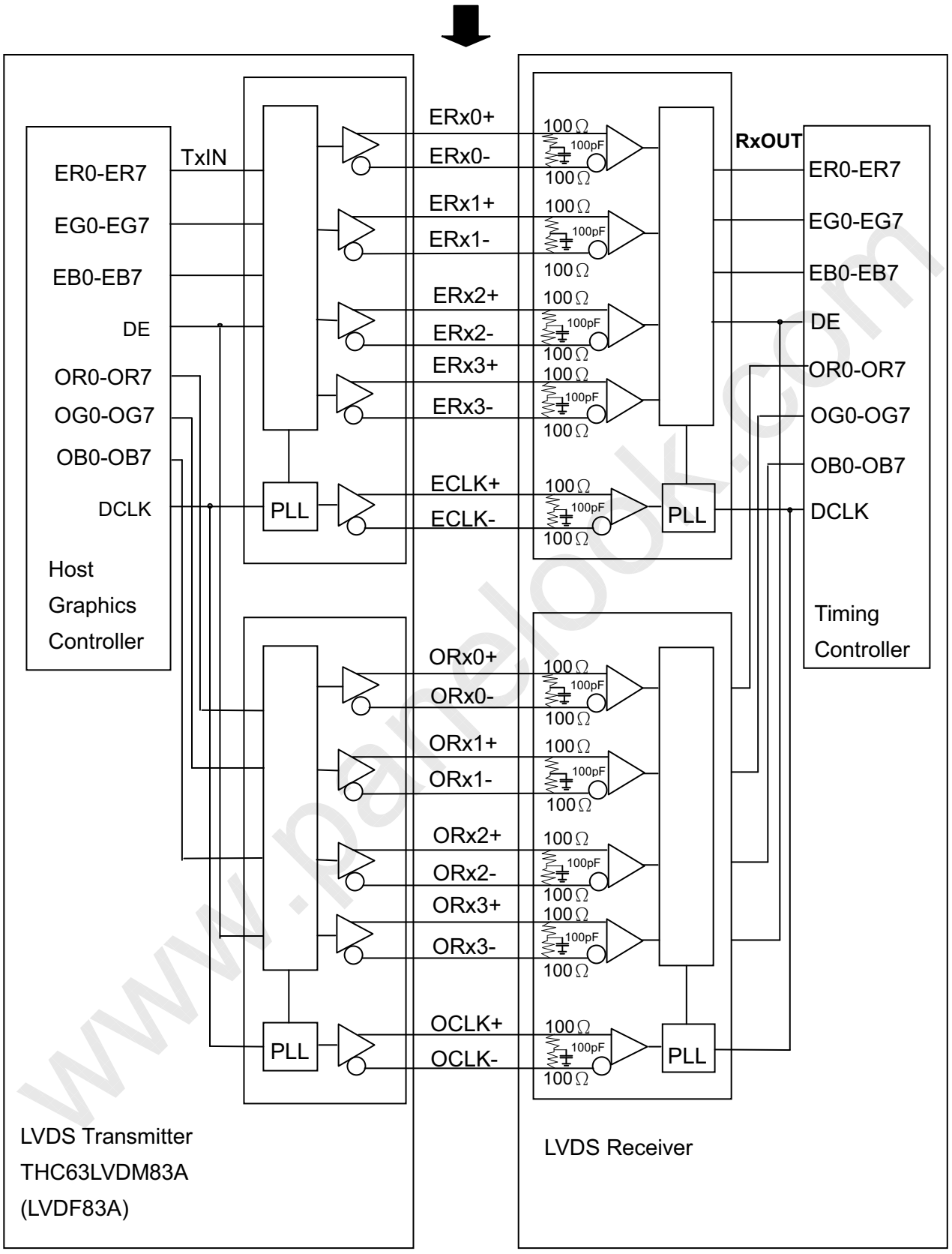


Note (7) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

Note (8) The screw hole which is distant from the connector is merged with Ground



5.2 BLOCK DIAGRAM OF INTERFACE



ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

DE: Data enable signal

DCLK: Data clock signal

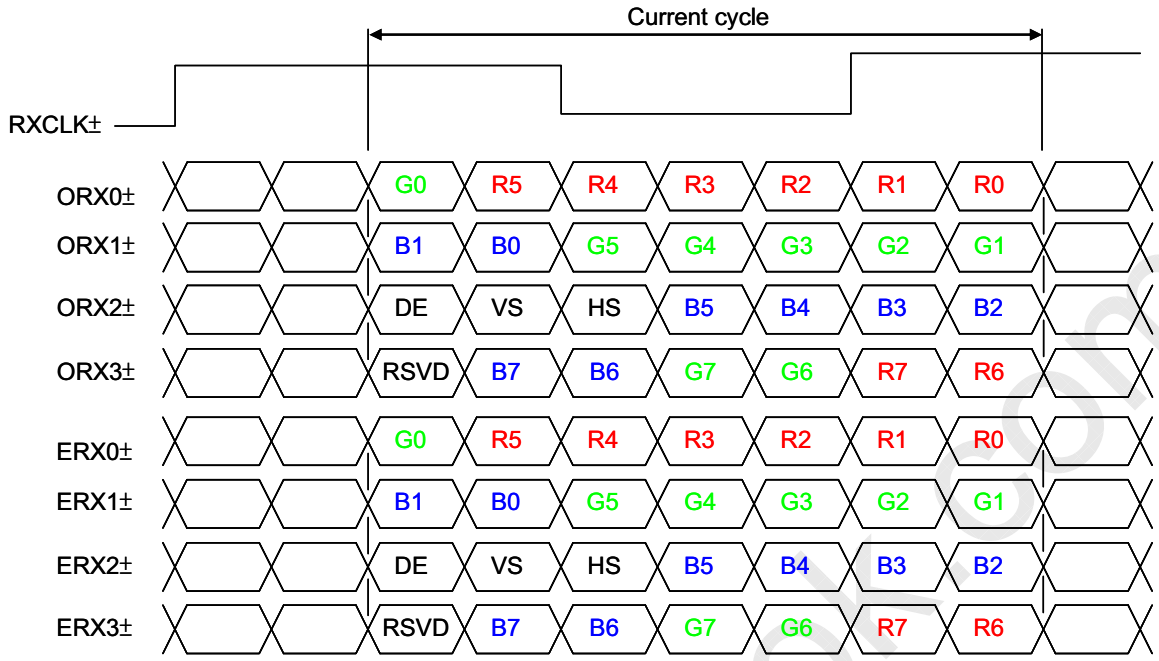
Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

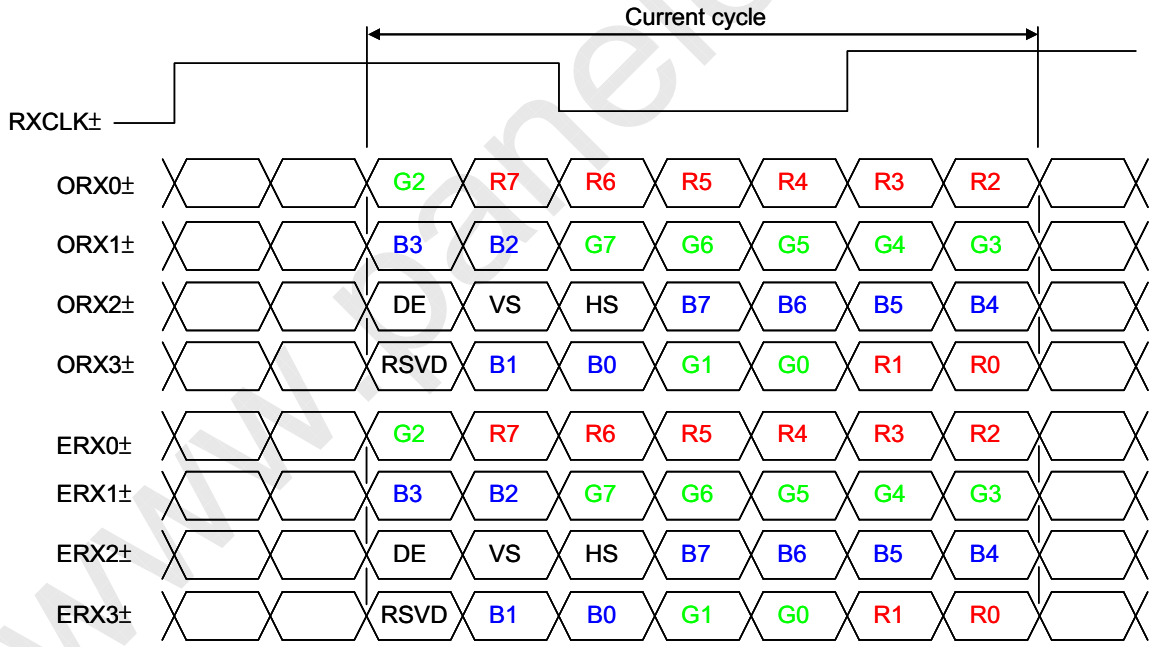
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.3 LVDS INTERFACE

VESA LVDS format：(SELLVDS pin=H or open)



JEDIA LVDS format：(SELLVDS pin=L)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

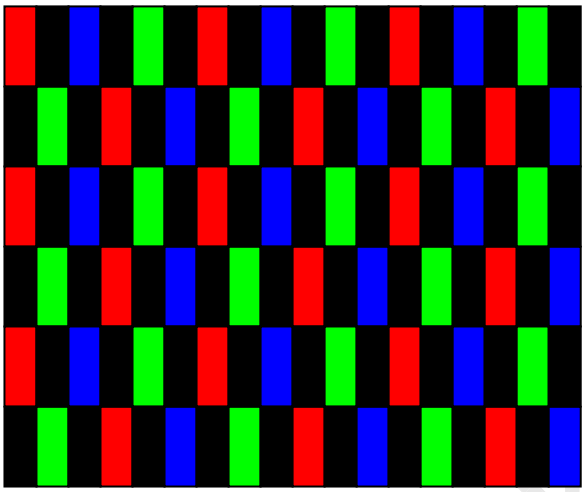
Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern:

Sub-pixel on-off pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com.The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

a. USB Sensor Board.

b. Programmable software.

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

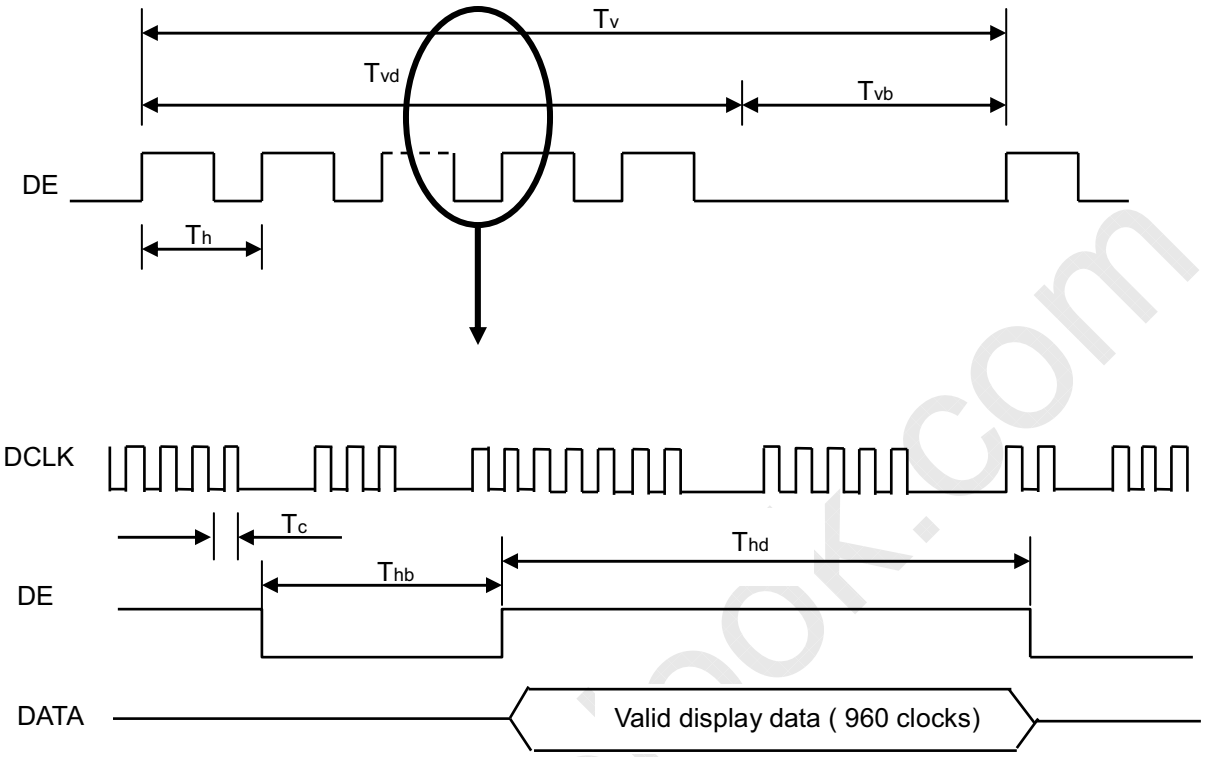
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	–	–	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	–	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	–	–	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	–	–	ps	(5)
	Hold Time	Tlvhd	600	–	–	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(6)
		F_{r6}	57	60	63	Hz	
	Total	Tv	1090	1125	1480	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	–
	Blank	Tvb	10	45	400	Th	–
Horizontal Active Display Term	Total	Th	1030	1100	1325	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	–
	Blank	Thb	70	140	365	Tc	–

Note (1) Please make sure the range of pixel clock has follow the below equation：

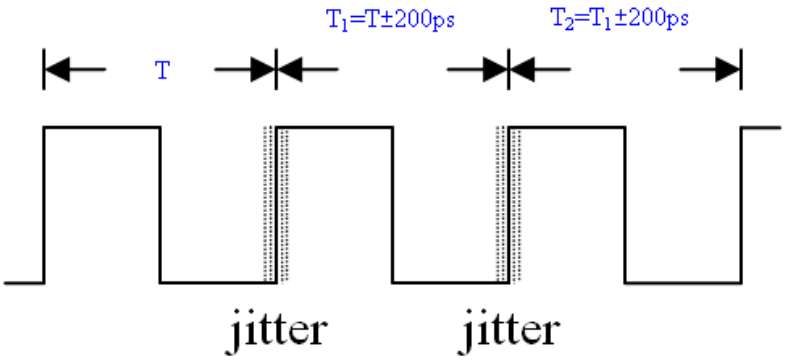
$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

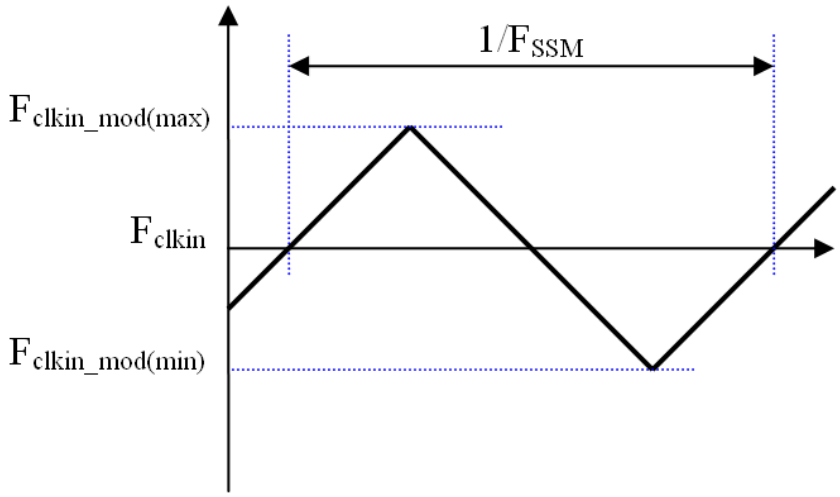
Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below：



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

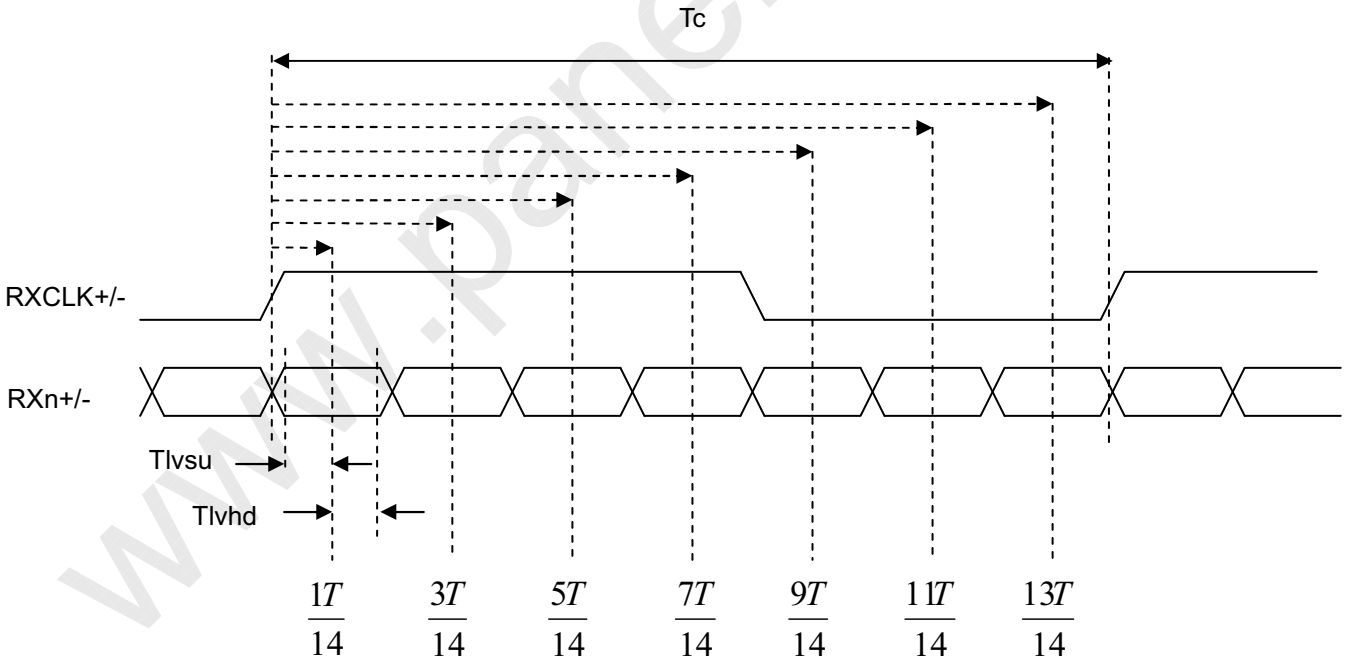


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

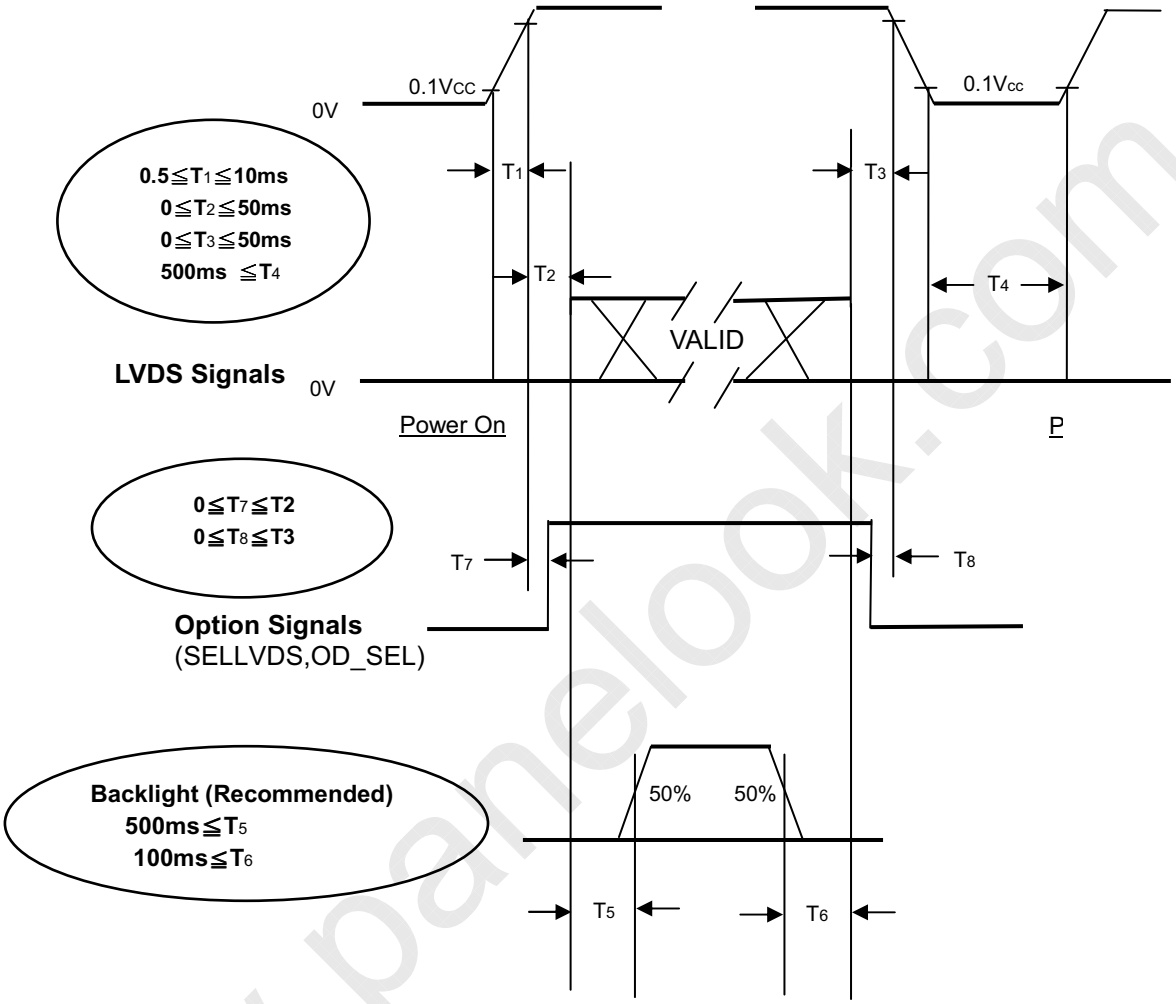


Note (6) : (ODSEL) = H/L or open for 50/60Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

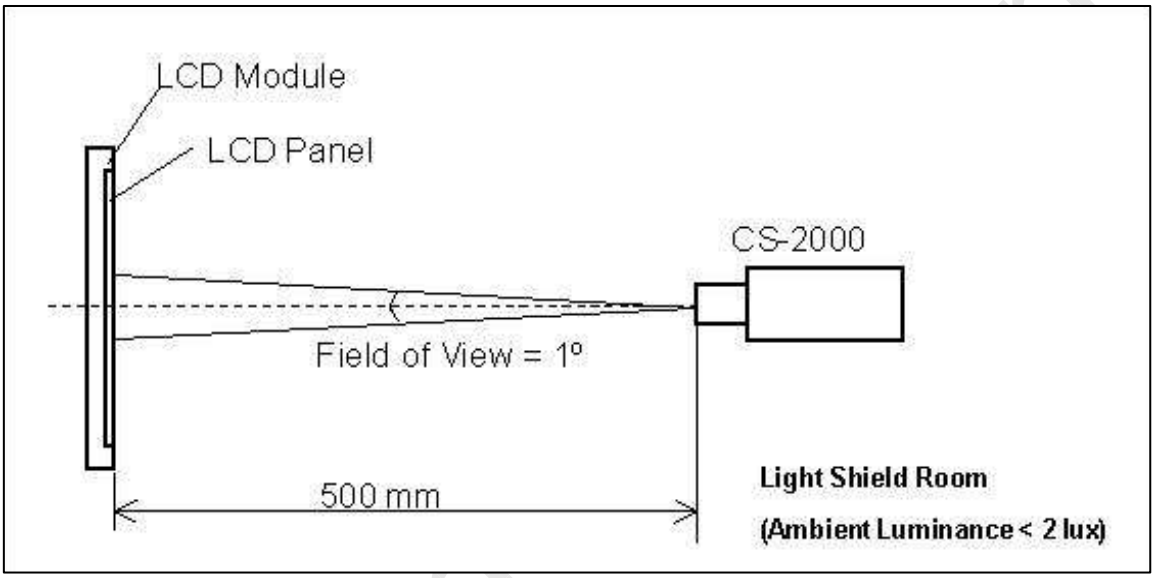
Note (5) Interface signal shall not be kept at high impedance when the power is on.

OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Vertical Frame Rate	Fr	60	Hz

Note (1) The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



Note (2) The LCD module should be measured with CMI T-CON code and follow the T-CON spec.

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction Standard light source "C"	Typ.-0.03	0.652	Typ+0.03	-	(0)
		Rcy			0.325		-	
	Green	Gcx			0.258		-	
		Gcy			0.586		-	
	Blue	Bcx			0.134		-	
		Bcy			0.106		-	
	White	Wcx			0.292		-	
		Wcy			0.337		-	
Center Transmittance		T%	θ_x=0°, θ_Y =0° with CMI module	-	4.4		%	(1),(8)
Contrast Ratio		CR		3500	5000		-	(1),(3)
Response Time (VA)		Gray to gray	θ_x=0°, θ_Y =0° with CMI Module@60Hz	-	8.5	17		(1),(4)
White Variation		δW	θ_x=0°, θ_Y =0° with CMI module	-	-	1.3	-	(1),(6)
Viewing Angle	Horizontal	θ_x+	CR≥20 (VA) with CMI module	80	88		Deg.	(1),(2)
		θ_x-		80	88			
	Vertical	θ_Y+		80	88			
		θ_Y-		80	88			

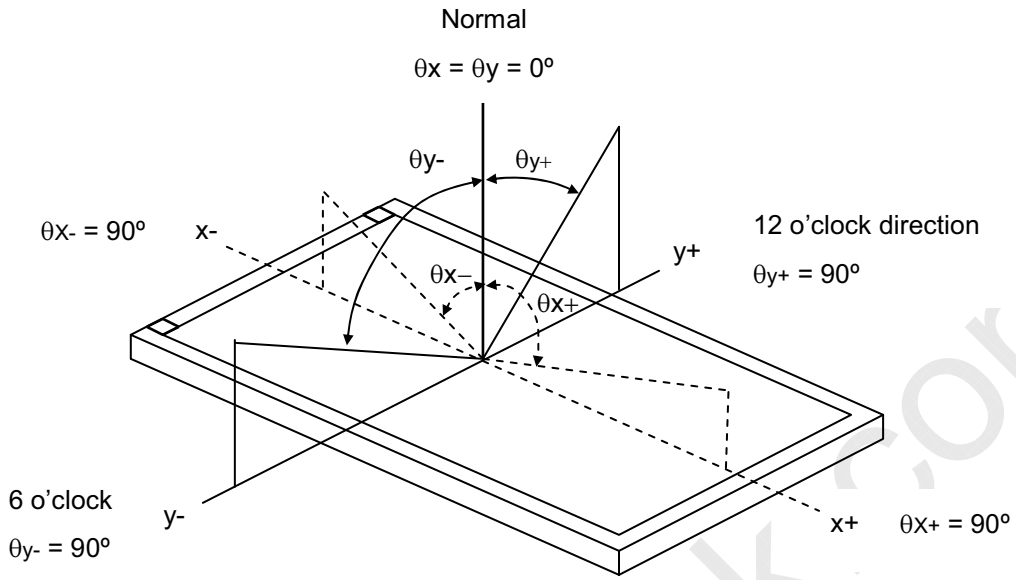
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's W,R,G,B spectrum and BLU's spectrum. Which BLU (for V315H1-L01) is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

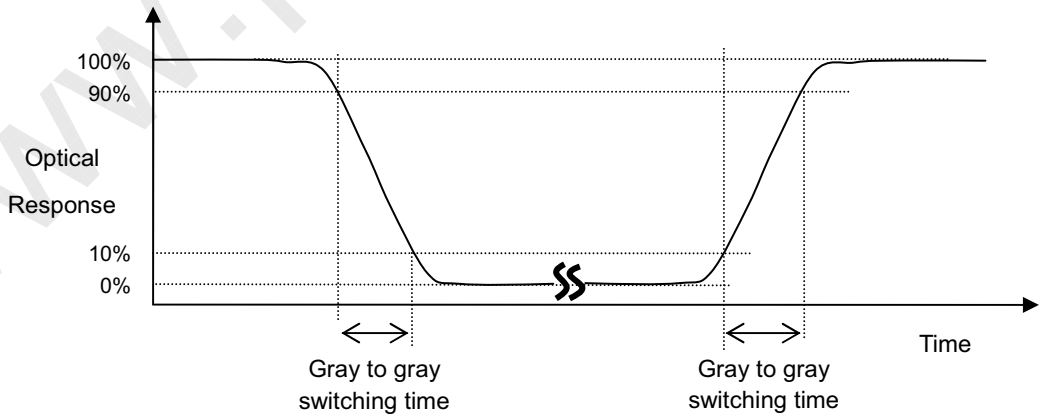
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

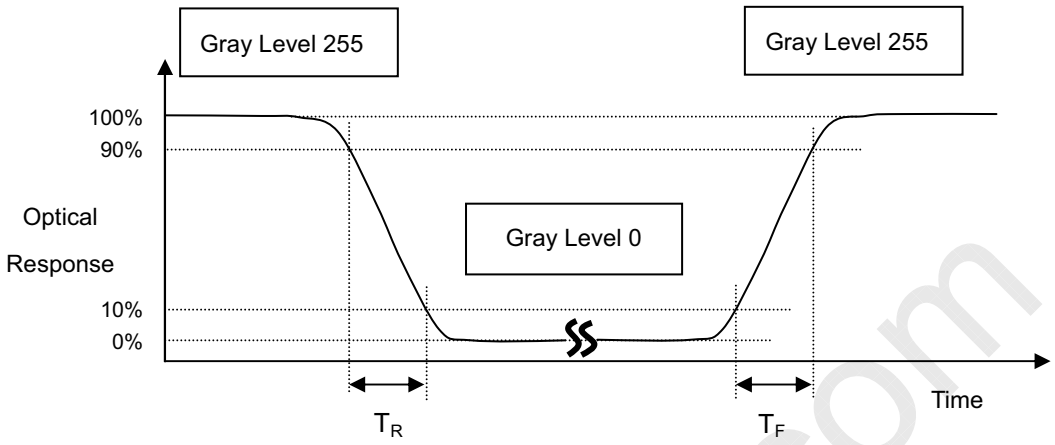
Note (4) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of Gray 0, 31, 63, 95, 127, 159, 191, 223, 255.

Gray to gray average time means the average switching time of Gray 0, 31, 63, 95, 127, 159, 191, 223, 255. to each other.

Note (5) Definition of Response Time (T_R, T_F):



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

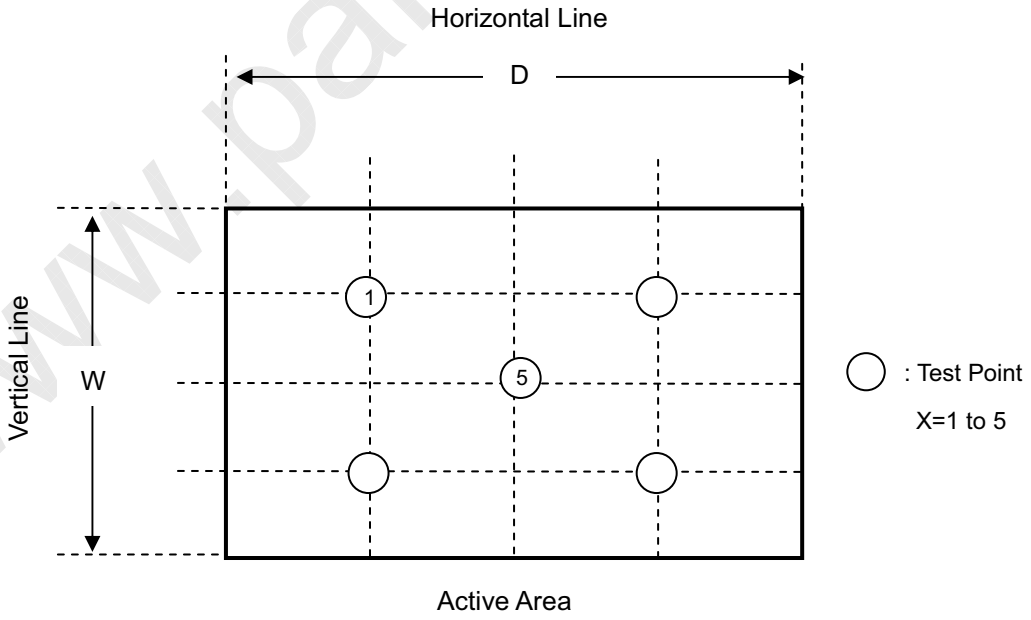
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

[Dino Hint: SEC and AUO are 9 points and the test point distance is W/6]



Note (8) Definition of Transmittance (T%) :

Measure the luminance of gray level 255 at center point of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\%$$ PRECAUTIONS

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] The distance between COF edge and rib of BLU must bigger than 5mm. This can prevent the damage of COF when assemble the module.

[6] Do not design sharp-pointed structure / parting line / tooling gate on the COF position of plastic parts, because the burr will scrape the COF.

[7] If COF would bended to assemble in the module. Do not put the IC location on the bending corner of COF.

[8] The gap between COF IC and any structure of BLU must bigger than 2mm. This can prevent the damage of COF IC

[9] Bezel opening must have no burr. Burr will scrape the panel surface.

[10] Bezel of module and bezel of set can not press or touch the panel surface. It will make light leakage or scrape.

[11] When module used FFC / FPC, but no FFC / FPC to be attached in the open cell. Customer can refer the FFC / FPC drawing and buy it by self.

[12] The gap between Panel and any structure of Bezel must bigger than 2mm. This can prevent the damage of Panel.

[13] Do not plug in or pull out the I/F connector while the module is in operation.

[14] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[15] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[16] When storing modules as spares for a long time, the following precaution is necessary.

[16.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35_at normal humidity without condensation.

[16.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[17] When ambient temperature is lower than 10ºC, the display quality might be reduced.

[18] The peeling strength of COF is 200gf/cm.

[19] During module assembly process, the static electricity around the environment should be less than 300V.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

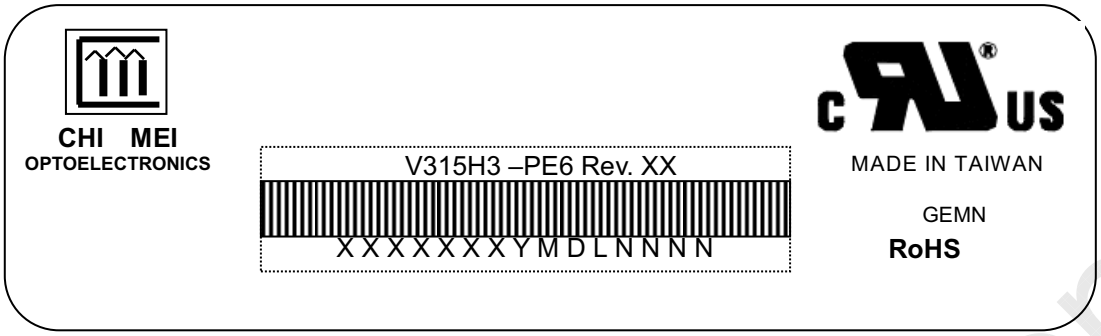
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

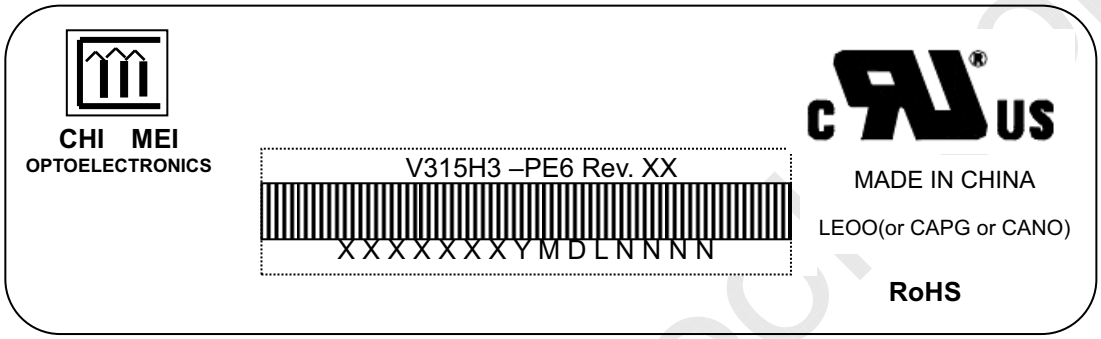
[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

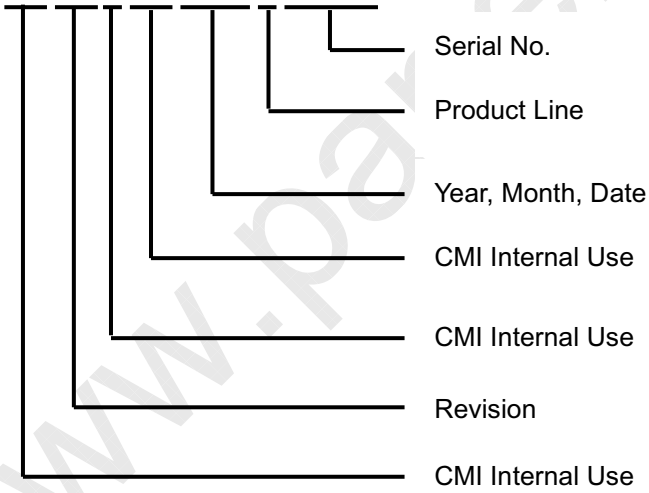




Model Name: V315H3-PE6

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 18 LCD TV Panels / 1 Box

(2) Box dimensions : 970 (L) X 640 (W) X 319 (H)

(3) Weight : approximately 36Kg (18 panels per box)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

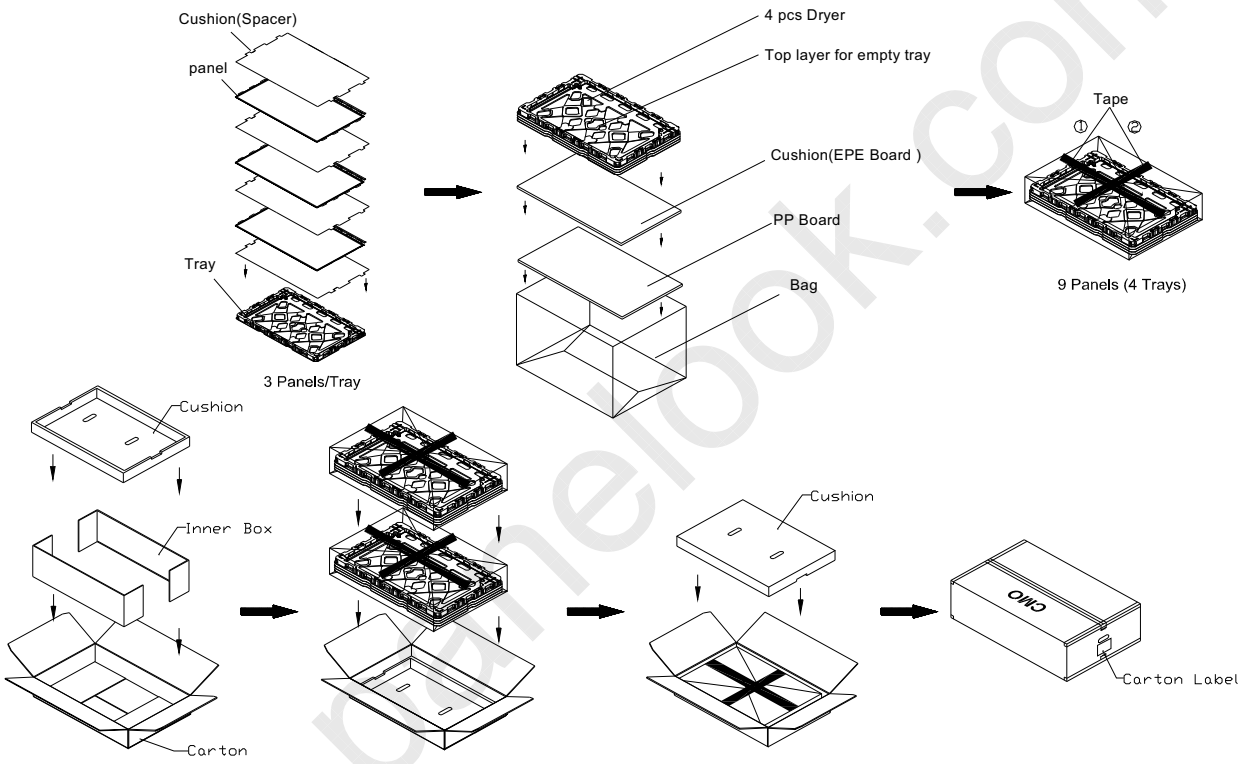
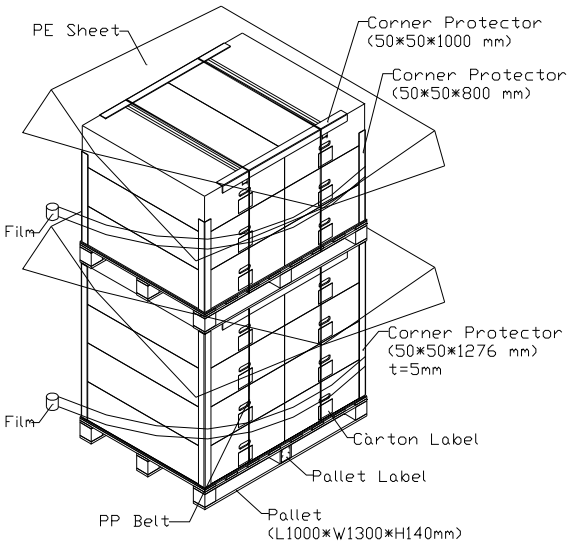
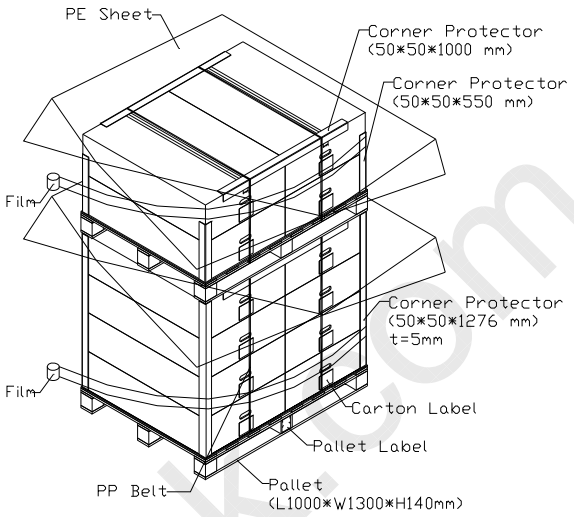


Figure.10-1 packing method

Sea / Land Transportation
(40ft HQ Container)



Sea / Land Transportation
(40ft Container)



Air Transportation

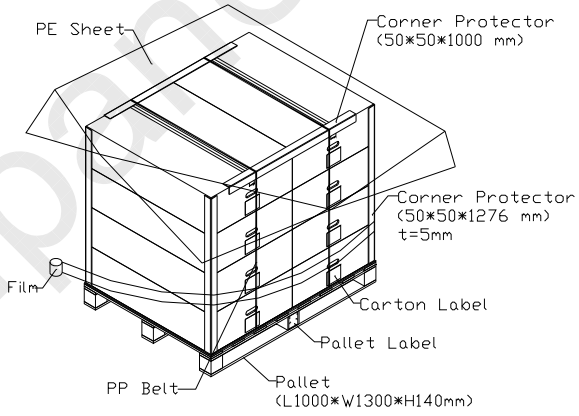


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTIC