☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

# MODEL NO.: V320BJ3
# SUFFIX: L01

**Customer:**

**APPROVED BY** **SIGNATURE**

Name / Title _____ _____

**Note**

Please return 1 copy for your confirmation with your signature and comments.

| Approved By | Checked By | Prepared By |
|---|---|---|
| Chao-Chun Chung | Vincent Chou | Kevin Tsai |

## CONTENTS

1. GENERAL DESCRIPTION ..... 5
1.1 OVERVIEW ..... 5
1.2 FEATURES ..... 5
1.3 APPLICATION ..... 5
1.4 GENERAL SPECIFICATIONS ..... 5
1.5 MECHANICAL SPECIFICATIONS ..... 6

2. ABSOLUTE MAXIMUM RATINGS ..... 7
2.1 ABSOLUTE RATINGS OF ENVIRONMENT ..... 7
2.2 PACKAGE STORAGE ..... 8
2.3 ELECTRICAL ABSOLUTE RATINGS ..... 8
2.3.1 TFT LCD MODULE ..... 8
2.3.2 BACKLIGHT INVERTER UNIT ..... 8

3. ELECTRICAL CHARACTERISTICS ..... 9
3.1 TFT LCD MODULE ..... 9
3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION ..... 12
3.2.1 LAMP SPECIFICATION (Ta = 25 ± 2 ºC) ..... 12
3.2.2 ELECTRICAL SPECIFICATION ..... 12
4.1 TFT LCD MODULE ..... 16

5. INPUT TERMINAL PIN ASSIGNMENT ..... 16
5.1 TFT LCD Module Input ..... 17
5.2 BACKLIGHT UNIT ..... 19
5.3 BLOCK DIAGRAM OF INTERFACE ..... 21
5.4 LVDS INTERFACE ..... 22
5.5 COLOR DATA INPUT ASSIGNMENT ..... 23

6. INTERFACE TIMING ..... 24
6.1 INPUT SIGNAL TIMING SPECIFICATIONS ..... 24
6.2 POWER ON/OFF SEQUENCE ..... 27

7. OPTICAL CHARACTERISTICS ..... 28
7.1 TEST CONDITIONS ..... 28
7.2 OPTICAL SPECIFICATIONS ..... 29

PRECAUTIONS ..... 33
8.1 ASSEMBLY AND HANDLING PRECAUTIONS ..... 33
8.2 SAFETY PRECAUTIONS ..... 33

9. DEFINITION OF LABELS ..... 34
9.1 CMI MODULE LABEL ..... 34

10. PACKAGING ..... 35
10.1 PACKAGING SPECIFICATIONS ..... 35
10.2 PACKAGING METHOD ..... 35

11. MECHANICAL CHARACTERISTIC ..... 37

## REVISION HISTORY

| Version | Date | Page(New) | Section | Description |
|---|---|---|---|---|
| Ver. 2.0 | Mar. 7, 2012 | All | All | The Approval specification was first issued. |

# 1. GENERAL DESCRIPTION

## 1.1 OVERVIEW

V320BJ3-L01 is a TFT Liquid Crystal Display module with 4U type CCFL Backlight unit and 1ch-LVDS interface. This module supports 1366 x 768 HDTV format and can display 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

## 1.2 FEATURES

- High brightness (400 nits)
- High contrast ratio (3000:1)
- Fast response time (Gray to gray average 8.5 ms)
- Response time (8.5ms)
- High color saturation (NTSC 72%)
- HDTV (1366 x 768 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- Viewing Angle : 176(H)/176(V) (CR>10) VA Technology

## 1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

## 1.4 GENERAL SPECIFICATIONS

| Item | Specification | Unit | Note |
|---|---|---|---|
| Active Area | 697.6845 (H) x 392.256 (V) | mm | (1) |
| Bezel Opening Area | 703.8 (H) x 398.4 (V) | mm | |
| Driver Element | a-si TFT active matrix | - | - |
| Pixel Number | 1366 x R.G.B. x768 | pixel | - |
| Pixel Pitch(Sub Pixel) | 0.17025(H) x 0.51075 (V) | mm | - |
| Pixel Arrangement | RGB vertical stripe | - | - |
| Power consumption | 71.40W (LVDS input Power 6.40W + Backlight Power 65 W) | Watt | (2) |
| Display Colors | 16.7M | color | - |
| Display Operation Mode | Transmissive mode / Normally Black | - | - |
| Surface Treatment | Anti-Glare coating (Haze 3.5%),Hard coating (3H) | - | (3) |

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) Please refer sec 3.1 and 3.2 for more information of Power consumption

Note (3) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

### 1.5 MECHANICAL SPECIFICATIONS

| Item | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Horizontal (H)<br>Vertical (V)<br>Depth (D)<br>Depth (D) | Horizontal (H) | 759 | 760 | 761 | mm | (1) |
| | Vertical (V) | 449 | 450 | 451 | mm | (1) |
| | Depth (D) | 31.5 | 32.5 | 33.5 | mm | (2) |
| | Depth (D) | 46.9 | 47.9 | 48.9 | mm | (3) |
| Weight | | - | 4860 | - | | - |

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to rear.

Note (3) Module Depth is between bezel to Inverter cover.

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Storage Temperature | TST | -20 | +60 | ºC | (1) |
| Operating Ambient Temperature | TOP | 0 | 50 | ºC | (1), (2) |
| Shock (Non-Operating) | SNOP | - | 50 | G | (3), (5) |
| Vibration (Non-Operating) | VNOP | - | 1.0 | G | (4), (5) |

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

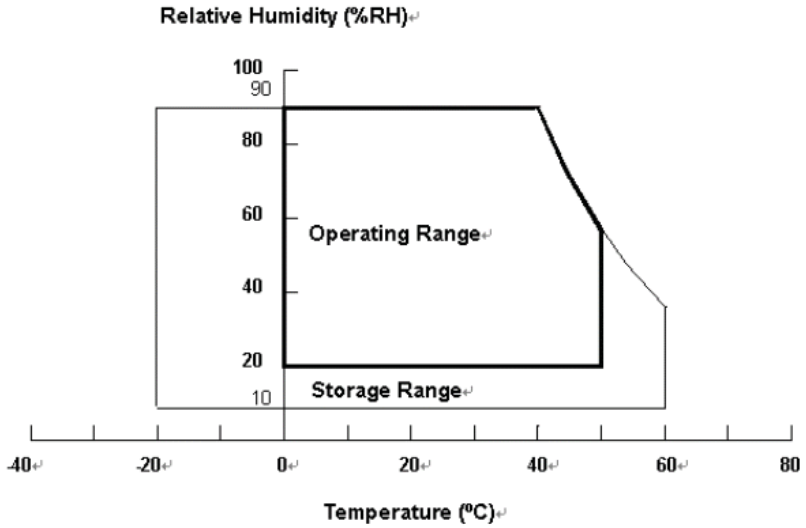
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



## 2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

## 2.3 ELECTRICAL ABSOLUTE RATINGS

### 2.3.1 TFT LCD MODULE

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power Supply Voltage | VCC | -0.3 | 13.5 | V | (1) |
| Logic Input Voltage | VIN | -0.3 | 3.6 | V | |

### 2.3.2 BACKLIGHT INVERTER UNIT

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Lamp Voltage | VW | – | 3000 | VRMS | |
| Power Supply Voltage | VBL | 0 | 30 | V | (1) |
| Control Signal Level | – | -0.3 | 7 | V | (1), (3) |

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.

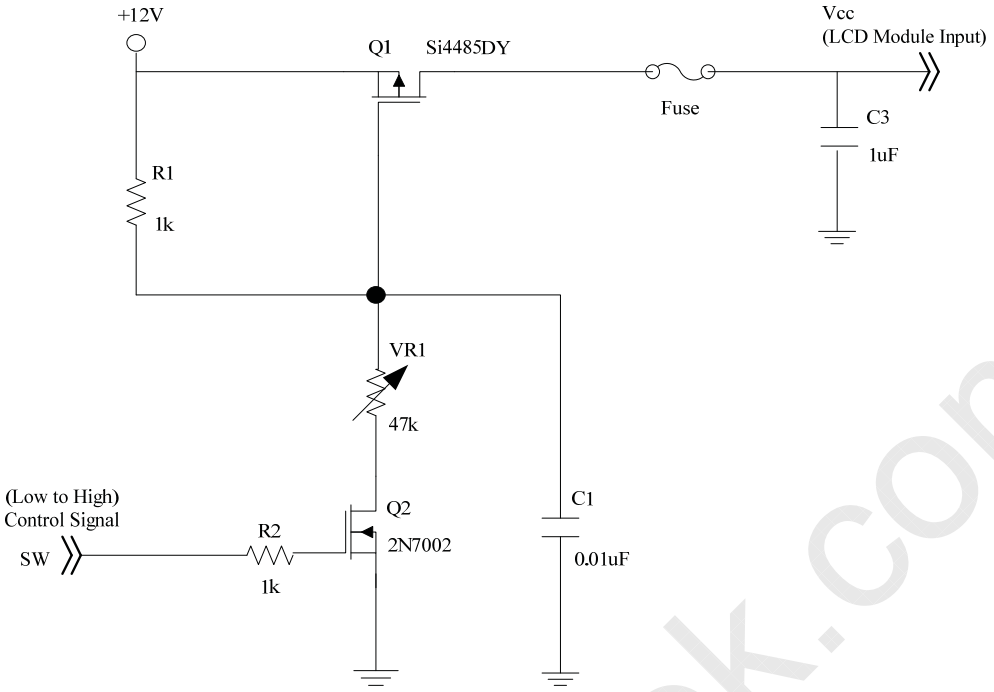
## 3. ELECTRICAL CHARACTERISTICS

### 3.1 TFT LCD MODULE

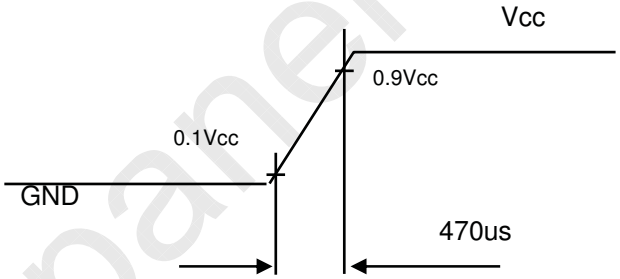
(Ta = 25 ± 2 ºC)

| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power Supply Voltage | | $V_{CC}$ | 10.8 | 12 | 13.2 | V | (1) |
| Rush Current | | $I_{RUSH}$ | — | — | 2.25 | A | (2) |
| Power consumption | White Pattern | $P_T$ | — | 3.76 | 4.53 | W | (3) |
| | Horizontal Stripe | | — | 5.47 | 6.40 | W | |
| | Black Pattern | | — | 3.6 | 4.21 | W | |
| Power Supply Current | White Pattern | Icc | — | 0.31 | 0.38 | A | (4) |
| | Horizontal Stripe | Icc | — | 0.456 | 0.53 | A | |
| | Black Pattern | Icc | — | 0.3 | 0.35 | A | |
| LVDS interface | Differential Input High Threshold Voltage | $V_{LVTH}$ | +100 | — | +500 | mV | (5) |
| | Differential Input Low Threshold Voltage | $V_{LVTL}$ | -500 | — | -100 | mV | |
| | Common Input Voltage | $V_{CM}$ | 1.0 | 1.2 | 1.4 | V | |
| | Differential input voltage (single-end) | $\lvert V_{ID} \rvert$ | 200 | — | 600 | mV | |
| | Terminating Resistor | $R_T$ | — | 100 | — | ohm | |
| CMIS interface | Input High Threshold Voltage | $V_{IH}$ | 2.7 | — | 3.3 | V | |
| | Input Low Threshold Voltage | $V_{IL}$ | 0 | — | 0.7 | V | |

Note (1) The module should be always operated within the above ranges.



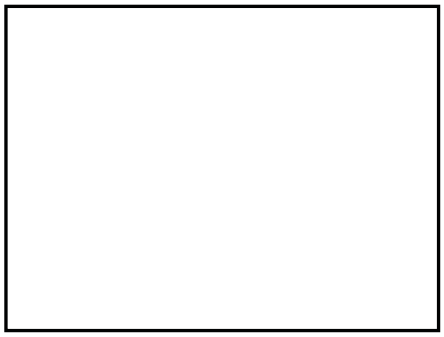

**Vcc rising time is 470us**




Note (3) The Specified Power consumption is under a,b,c pattern.

Note (4) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, $f_v$ = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

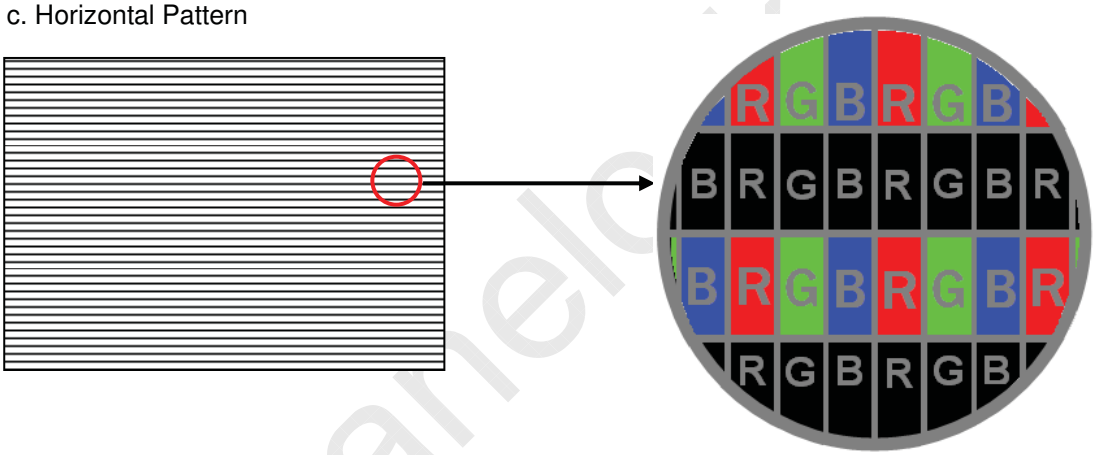


Active Area

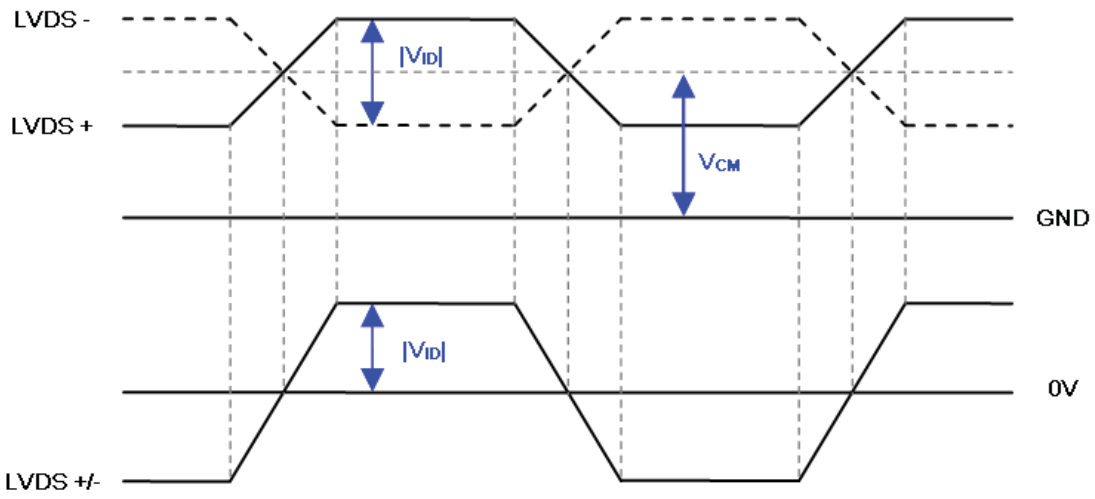
b. Black Pattern

Active Area

c. Horizontal Pattern




Note (4) The LVDS input characteristics are as follows :



### 3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

#### 3.2.1 LAMP SPECIFICATION (Ta = 25 ± 2 ºC)

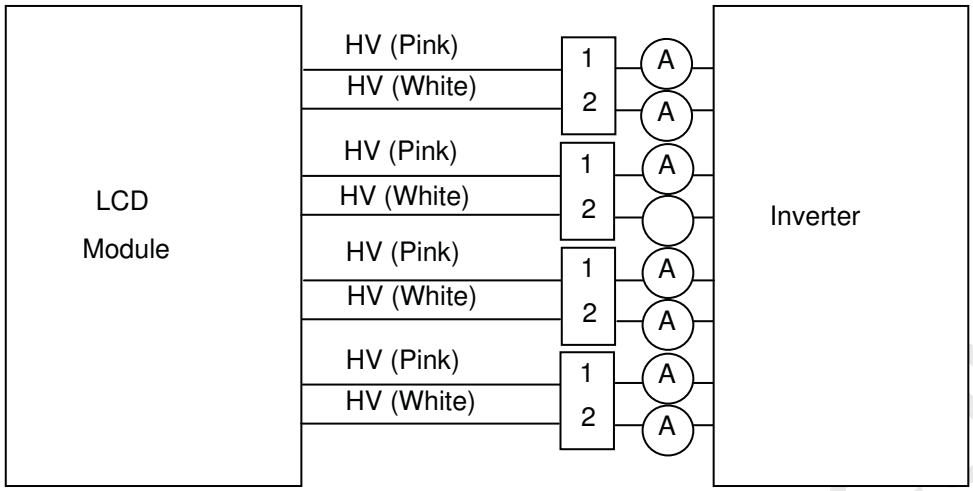
| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Lamp Input Voltage | VL | - | 1550 | - | $V_{RMS}$ | $I_L$=10.5mA |
| Lamp Current | $I_L$ | 10.0 | 10.5 | 11.0 | $mA_{RMS}$ | (1) |
| Lamp Turn On Voltage | VS | - | - | 2700 | $V_{RMS}$ | Ta = 0 ºC (2) |
| | | - | - | 2290 | $V_{RMS}$ | Ta = 25 ºC(3) |
| Operating Frequency | FL | 30 | - | 80 | KHz | |
| Lamp Life Time | LBL | 50,000 | - | - | Hrs | (4) |

#### 3.2.2 ELECTRICAL SPECIFICATION

(Ta = 25 ± 2 ºC)

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Total Power Consumption | $P_{255}$ | - | 65 | 69 | W | (5), (6), $I_L$ =10.5mA |
| Power Supply Voltage | $V_{BL}$ | 22.8 | 24.0 | 25.2 | VDC | |
| Power Supply Current | $I_{BL}$ | - | 2.71 | 2.88 | A | Non Dimming |
| Inrush current | $I_R$ | - | - | 4.22 | $A_{peak}$ | $V_{BL}$=24V,(IL=typ) (7) |
| Input Ripple Noise | - | - | - | 912 | mVP-P | VBL=22.8V |
| Oscillating Frequency | $F_W$ | 60 | 63 | 66 | kHz | (3) |
| Dimming Frequency | $F_B$ | 150 | 160 | 170 | Hz | |
| PWM Duty Ratio | $D_{MIN}$ | 10 | - | 100 | % | (8) |

**Note (1)** Lamp current is measured by utilizing **AC current probe Tektronix P6022** as shown below:




**Note (2)** The lamp starting voltage $V_S$ should be applied to the lamp for more than 1 second under starting up duration. Otherwise the lamp could not be lighted on completed.

**Note (3)** The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

**Note (4)** The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and $I_L$ = 10.0~11.0 $mA_{RMS}$.

**Note (5)** The power supply capacity should be higher than the total inverter power consumption $P_{BL}$. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

**Note (6)** The measurement condition of Max. value is based on 31.5" backlight unit under input voltage 24V, average lamp current 10.8 mA and lighting 30 minutes later.

**Note (7)** The duration of Input Inrush Current is about VBL Rising Time 30ms.

**Note (8)** 10% minimum duty ratio is only valid for electrical operation

### 3.2.3 INVERTER INTERFACE CHARACTERISTICS

| Parameter | | Symbol | Test Condition | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| On/Off Control Voltage | ON | $V_{BLON}$ | — | 2.0 | — | 5.0 | V | |
| | OFF | | — | 0 | — | 0.8 | V | |
| External PWM Control Voltage | HI | $V_{EPWM}$ | — | 2.0 | — | 5.0 | V | Duty on |
| | LO | | | 0 | — | 0.8 | V | Duty off |
| Error Signal | | ERR | — | Open Collector | | | | Abnormal |
| | | | | 0 | — | 0.8 | V | Normal |
| VBL Rising Time | | Tr1 | — | 30 | — | — | ms | 10%-90%$V_{BL}$ |
| VBL Falling Time | | Tf1 | — | 30 | — | — | ms | |
| Control Signal Rising Time | | Tr | — | — | — | 100 | ms | |
| Control Signal Falling Time | | Tf | — | — | — | 100 | ms | |
| PWM Signal Rising Time | | $T_{PWMR}$ | — | — | — | 100 | us | |
| PWM Signal Falling Time | | $T_{PWMF}$ | — | — | — | 100 | us | |
| Input impedance | | $R_{IN}$ | — | 1 | — | — | MΩ | |
| PWM Turn on Delay Time | | $T_{PWM}$ | — | 0 | — | — | ms | |
| BLON Turn on Delay Time | | $T_{on}$ | — | 300 | — | — | ms | |
| BLON Turn off Time | | $T_{off}$ | — | 300 | — | — | ms | |
| BLON Delay Time | | $T_{on1}$ | — | 300 | — | — | ms | |

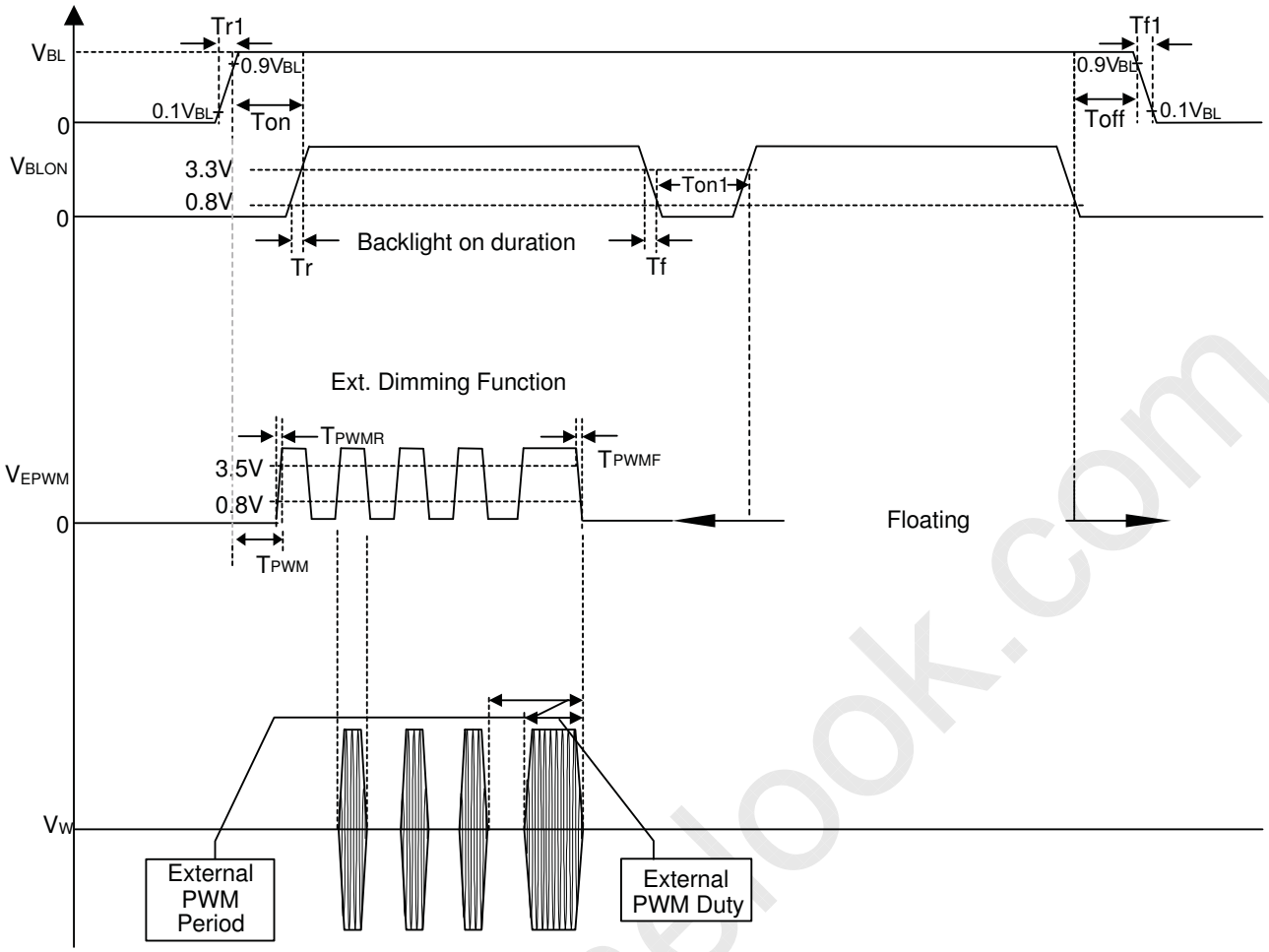
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

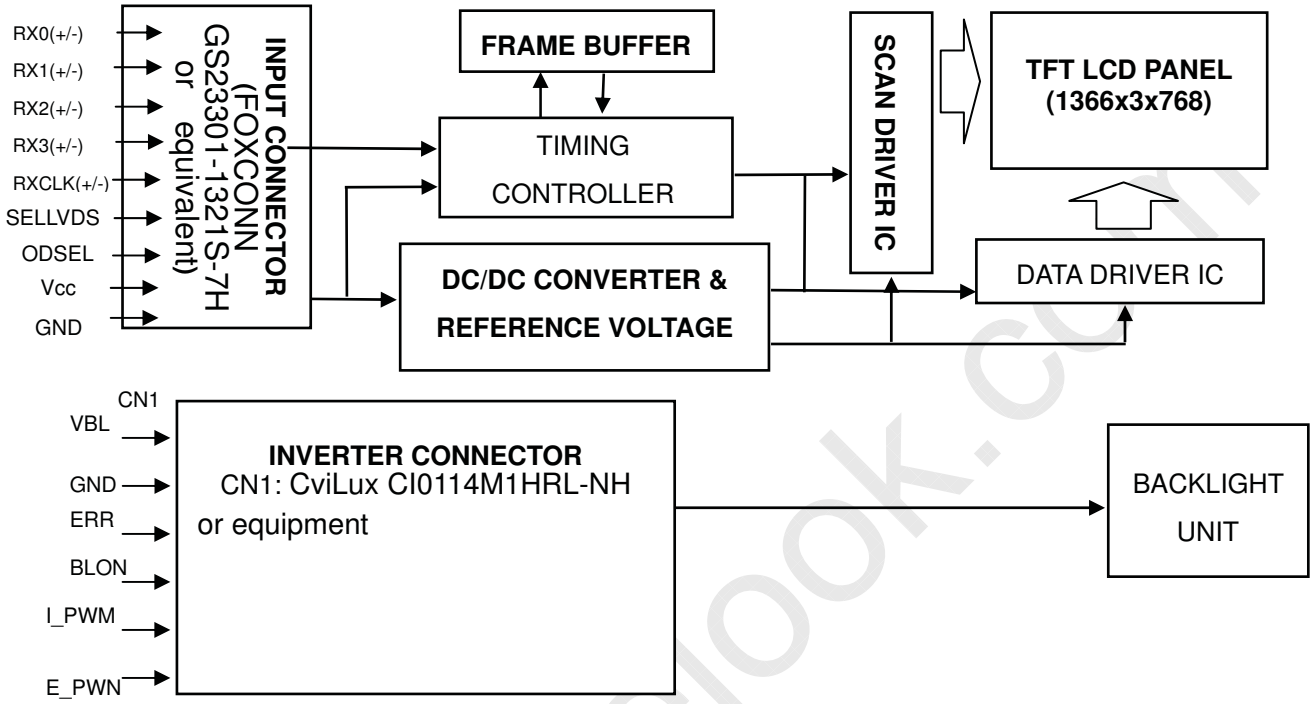
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



## 4. BLOCK DIAGRAM OF INTERFACE

### 4.1 TFT LCD MODULE



## 5. INPUT TERMINAL PIN ASSIGNMENT

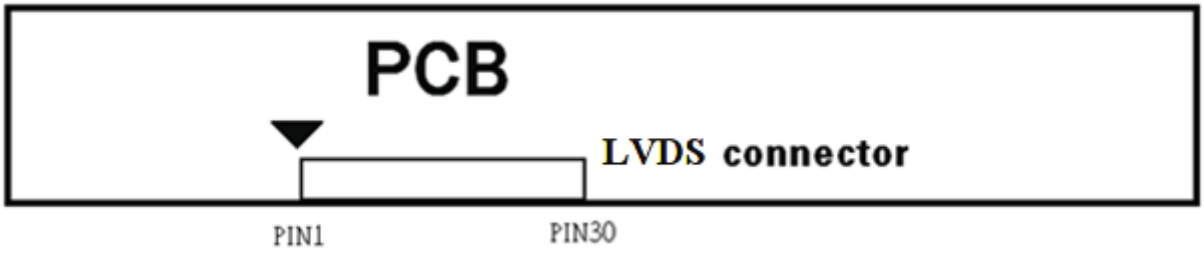
### 5.1 TFT LCD Module Input

**CNF1 Connector Pin Assignment**

| Pin No. | Symbol | Description | Note |
|---|---|---|---|
| 1 | VCC | Power supply: +12V | |
| 2 | VCC | Power supply: +12V | |
| 3 | VCC | Power supply: +12V | |
| 4 | VCC | Power supply: +12V | |
| 5 | GND | Ground | |
| 6 | GND | Ground | |
| 7 | GND | Ground | |
| 8 | GND | Ground | |
| 9 | SELLVDS | Select LVDS data format | (2)(4) |
| 10 | NC | No connection | (3) |
| 11 | GND | Ground | |
| 12 | RX0- | Negative transmission data of pixel 0 | |
| 13 | RX0+ | Positive transmission data of pixel 0 | |
| 14 | GND | Ground | |
| 15 | RX1- | Negative transmission data of pixel 1 | |
| 16 | RX1+ | Positive transmission data of pixel 1 | |
| 17 | GND | Ground | |
| 18 | RX2- | Negative transmission data of pixel 2 | |
| 19 | RX2+ | Positive transmission data of pixel 2 | |
| 20 | GND | Ground | |
| 21 | RXCLK- | Negative of clock | |
| 22 | RXCLK+ | Positive of clock | |
| 23 | GND | Ground | |
| 24 | RX3- | Negative transmission data of pixel 3 | |
| 25 | RX3+ | Positive transmission data of pixel 3 | |
| 26 | GND | Ground | |
| 27 | NC | No connection | (3) |
| 28 | NC | No connection | (3) |
| 29 | NC | No connection | (3) |
| 30 | GND | Ground | |

Note (1) Connector type: FOXCONN GS23301-1321S-7H or equivalent.

LVDS connector pin order defined as follows



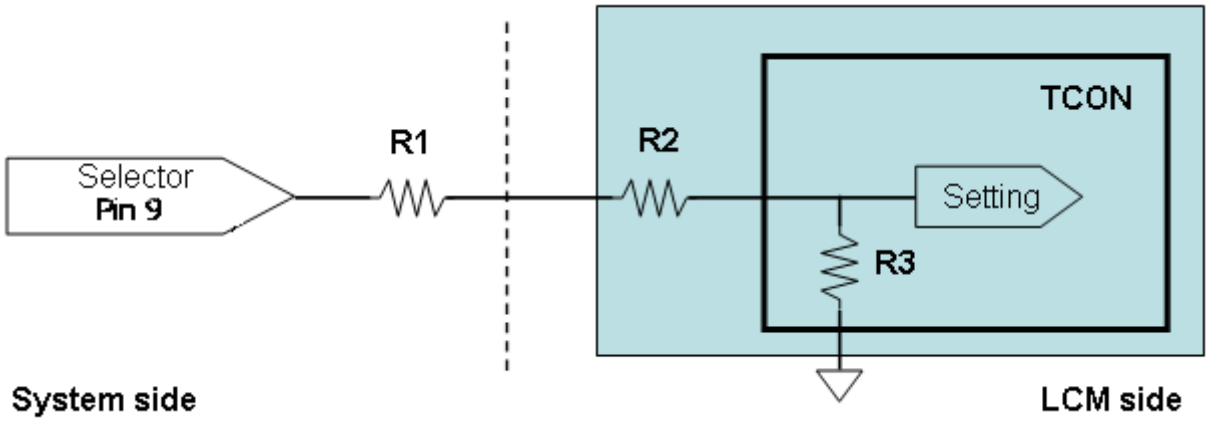

Note (2) Low = Open or connect to GND: VESA Format, High = Connect to +3.3V: JEIDA Format.

Please refer to 5.5 LVDS INTERFACE

Note (3) Reserved for internal use. Left it open.

Note (4) SELLVDS pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



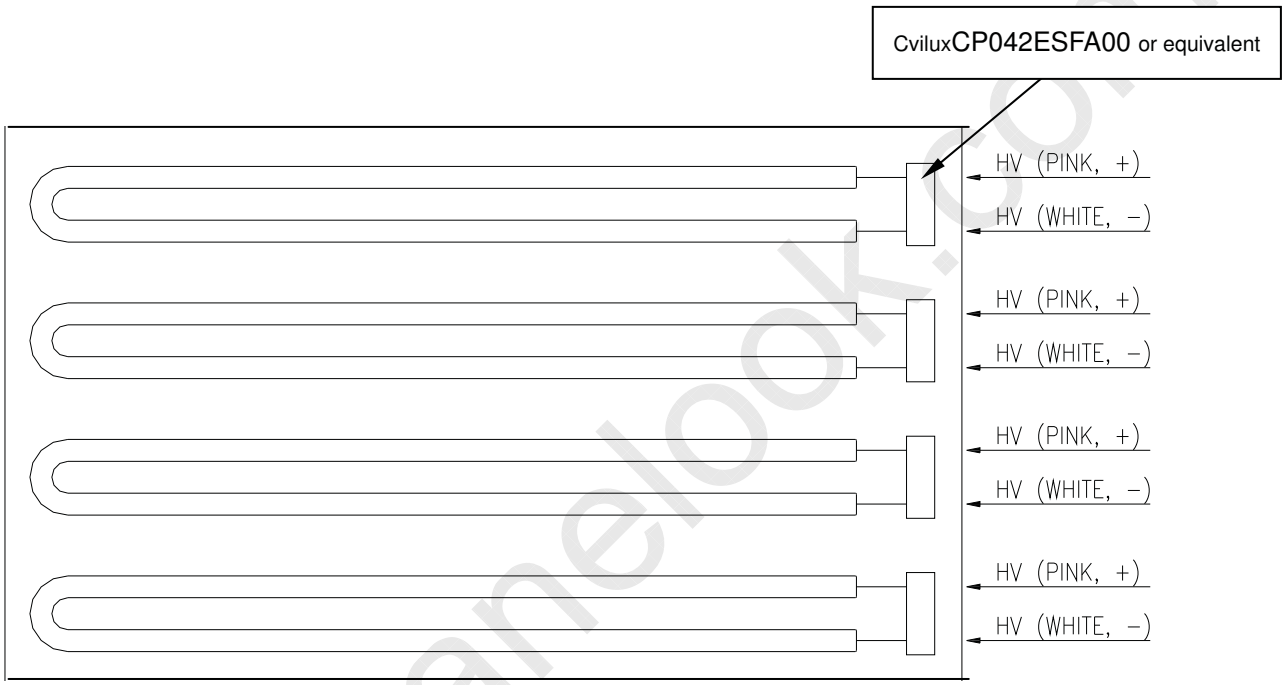
### 5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2-CN5 (Housing): Cvilux CP042ESFA00 or equivalent

| Pin No. | Symbol | Description | Wire Color |
|---|---|---|---|
| 1 | HV | High Voltage | PINK |
| 2 | HV | High Voltage | WHITE |

Note (1) The backlight interface housing for high voltage side is Cvilux CP042ESFA00 or equivalent. The mating header on inverter part number is Cvilux CP042EP1MFB-LF or equivalent



**INVERTER UNIT**

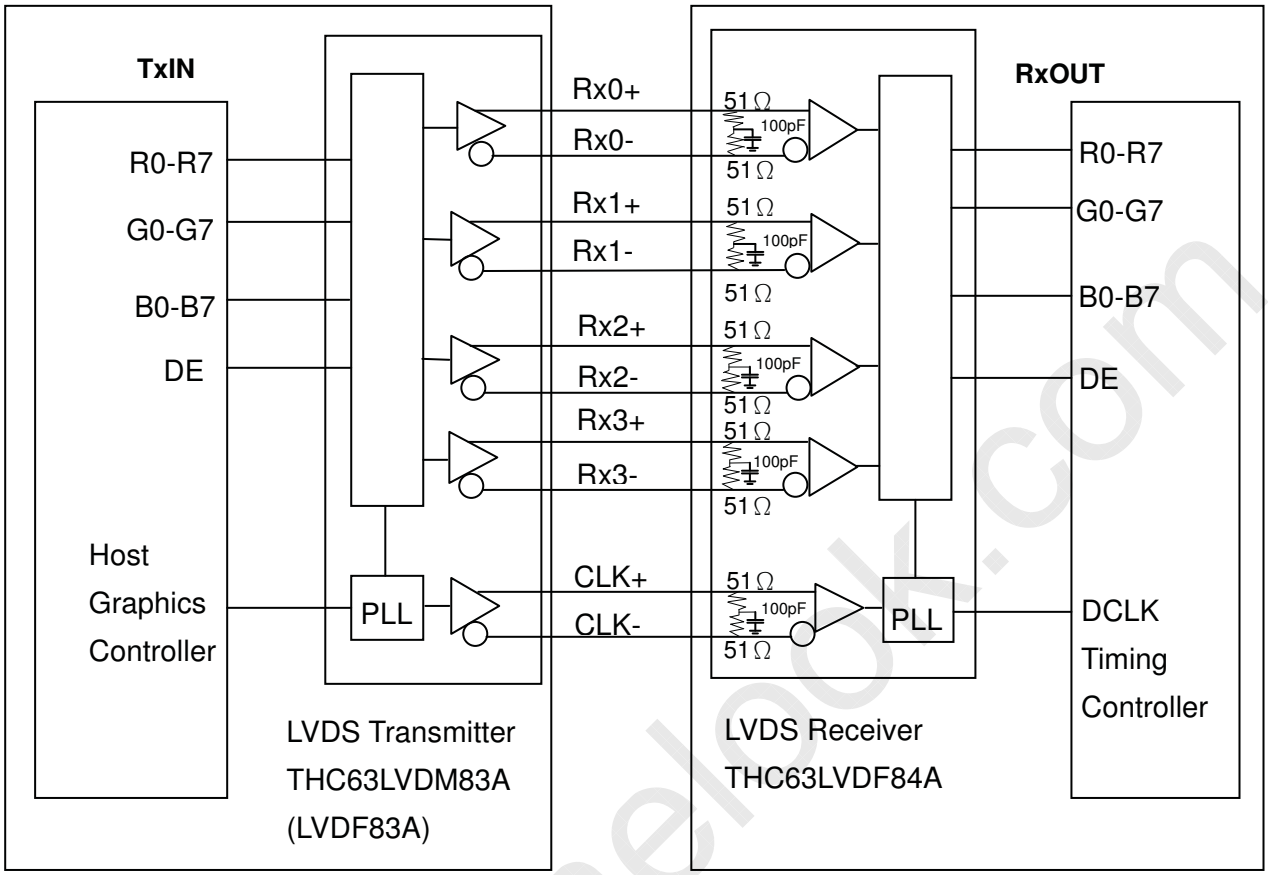
CN1(Header): CviLux CI0114M1HRL-NH or equipment

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VBL | +24V Power input |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | GND | Ground |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |
| 11 | ERR | Normal (GND)<br>Abnormal ( open collector) |
| 12 | BLON | Backlight on/off control |
| 13 | NC | NC |
| 14 | E_PWM | External PWM control signal |

CN2-CN5(Header): CviLux CP042EP1MFB-LF or equivalent

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | CCFL HOT | CCFL high voltage |
| 2 | CCFL HOT | CCFL high voltage |

### 5.3 BLOCK DIAGRAM OF INTERFACE

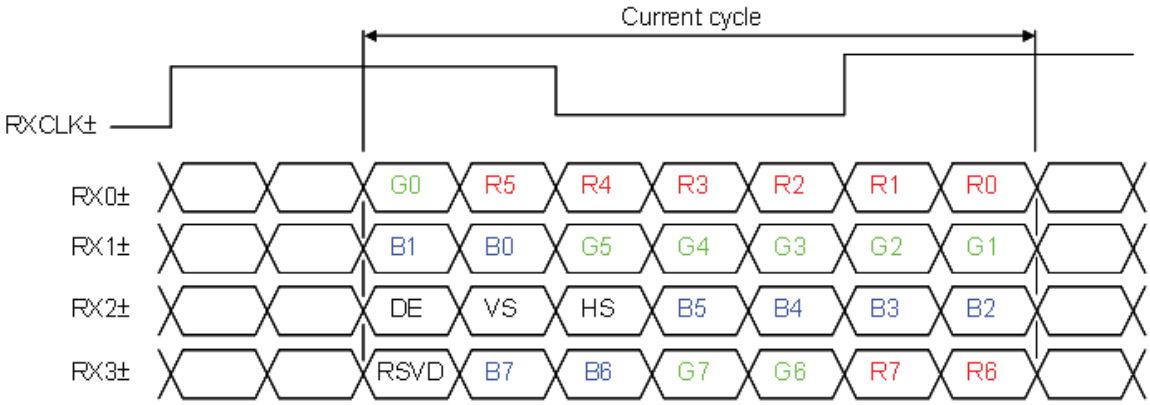



R0~R7 : Pixel R Data ,
G0~G7 : Pixel G Data ,
B0~B7 : Pixel B Data ,
DE : Data enable signal
DCLK : Data clock signal

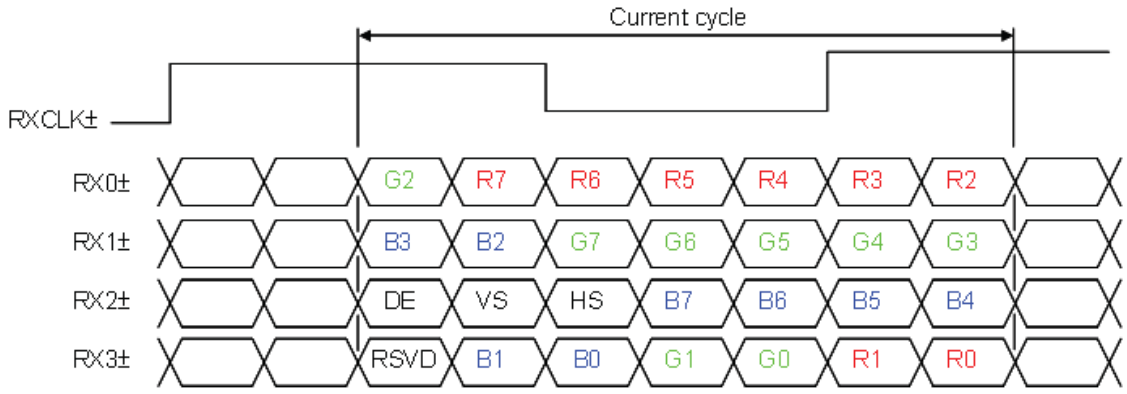
Note (1) The system must have the transmitter to drive the module.
Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

## 5.4 LVDS INTERFACE

**SELLVDS = L or Open (VESA)**




**SELLVDS = H (JEIDA)**




R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

Notes(1) RSVD(reserved)pins on the transmitter shall be “H” or( “L” or OPEN)

### 5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

| Color | | Data Signal | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Red | | | | | | | | Green | | | | | | | | Blue | | | | | | | |
| | | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Magenta | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Gray Scale Of Red | Red (0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (2) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Red (253) | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (254) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (255) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale Of Green | Green (0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Green (253) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (254) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (255) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale Of Blue | Blue (0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | Blue (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Blue (253) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| | Blue (254) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | Blue (255) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 6. INTERFACE TIMING

### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

| Signal | Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| LVDS Receiver Clock | Frequency | $F_{clkin}$ (=1/TC) | 60 | 76 | 82 | MHz | |
| | Input cycle to cycle jitter | $T_{rcl}$ | — | — | 350 | ps | (3) |
| | Spread spectrum modulation range | $F_{clkin\_mod}$ | $F_{clkin}$-2% | — | $F_{clkin}$+2% | MHz | (4) |
| | Spread spectrum modulation frequency | $F_{SSM}$ | — | — | 200 | KHz | |
| LVDS Receiver Data | Receiver Skew Margin | $T_{RSKM}$ | -400 | — | 400 | ps | (5) |
| Vertical Active Display Term | Frame Rate | $F_{r5}$ | 47 | 50 | 53 | Hz | |
| | | $F_{r6}$ | 57 | 60 | 63 | Hz | |
| | Total | Tv | 778 | 806 | 888 | Th | Tv=Tvd+Tvb |
| | Display | Tvd | 768 | 768 | 768 | Th | |
| | Blank | Tvb | 10 | 38 | 120 | Th | |
| Horizontal Active Display Term | Total | Th | 1442 | 1560 | 2006 | Tc | Th=Thd+Thb |
| | Display | Thd | 1366 | 1366 | 1366 | Tc | |
| | Blank | Thb | 76 | 194 | 640 | Tc | |

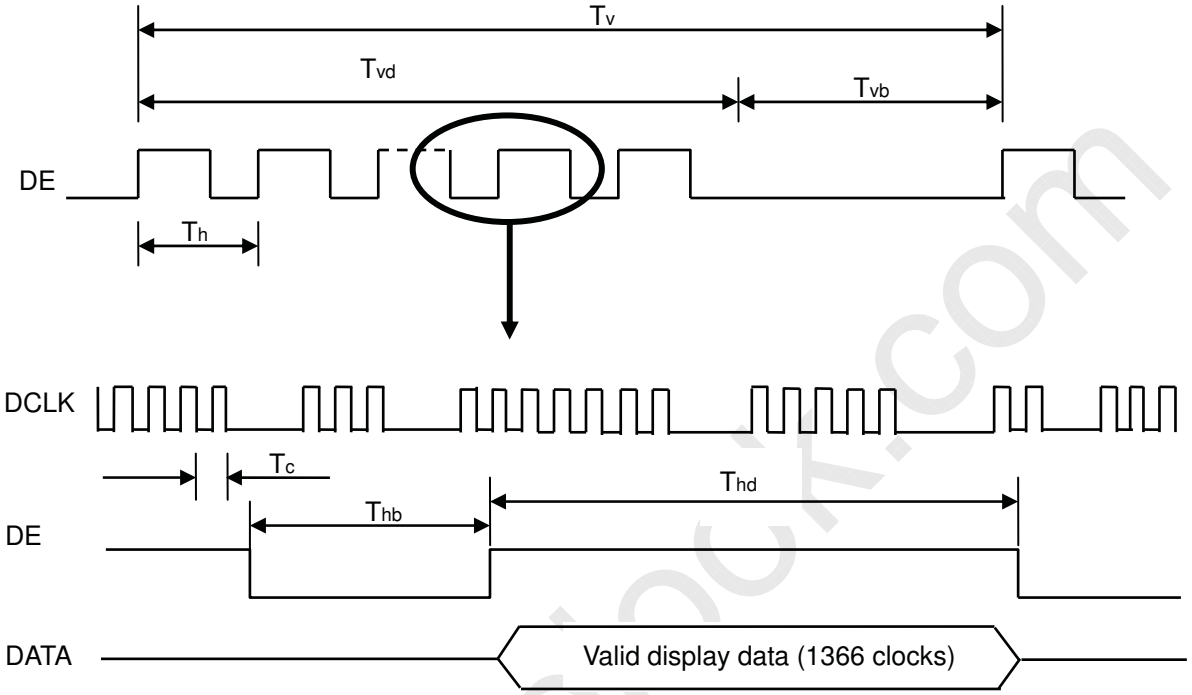
Note (1) Please make sure the range of frame rate has follow the below equation：

$Fclkin(max) \geqq Fr6 \times Tv \times Th$

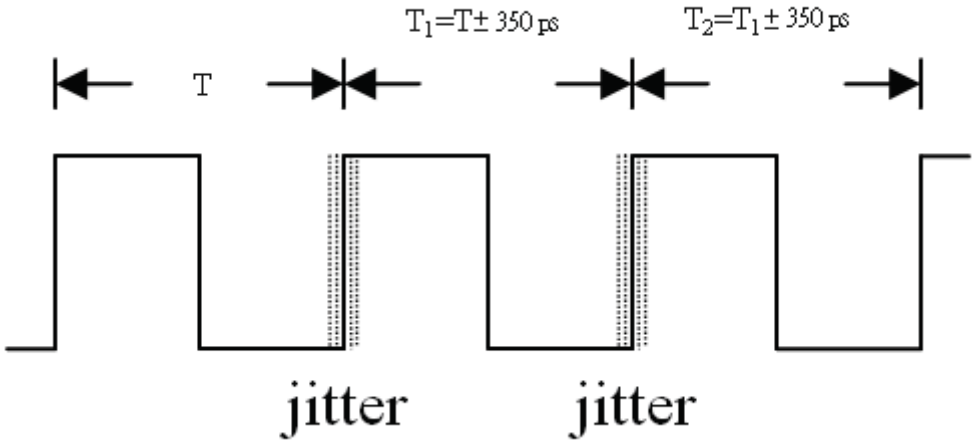
$Fr5 \times Tv \times Th \geqq Fclkin(min)$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below：

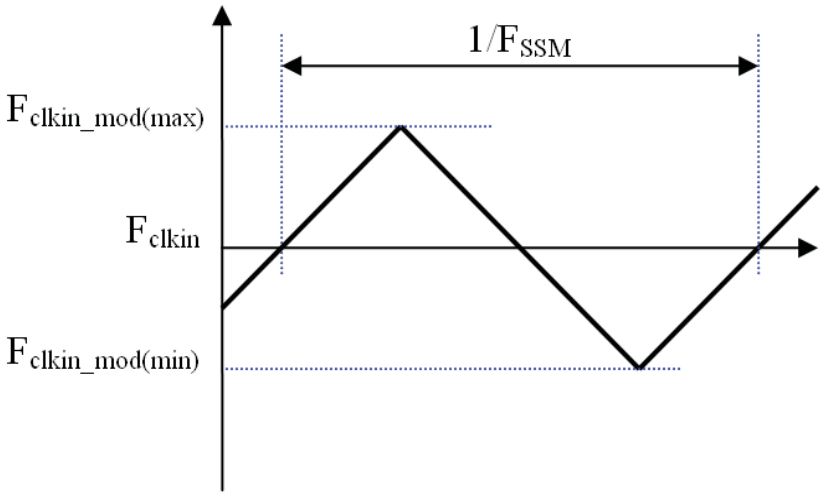
**INPUT SIGNAL TIMING DIAGRAM**




Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I $T_1$ – TI

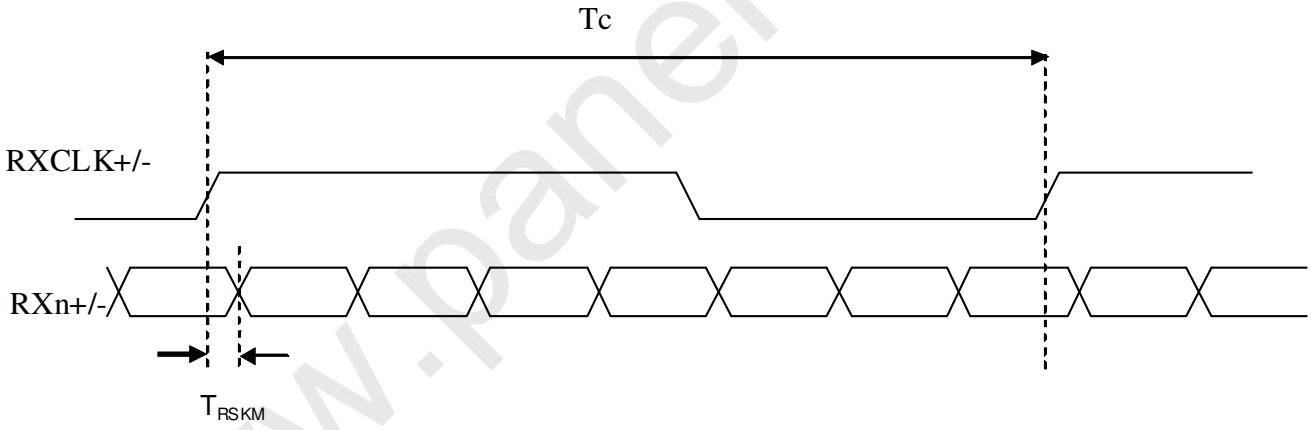


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.




Note (5) LVDS receiver skew margin is defined and showing as the following figures.

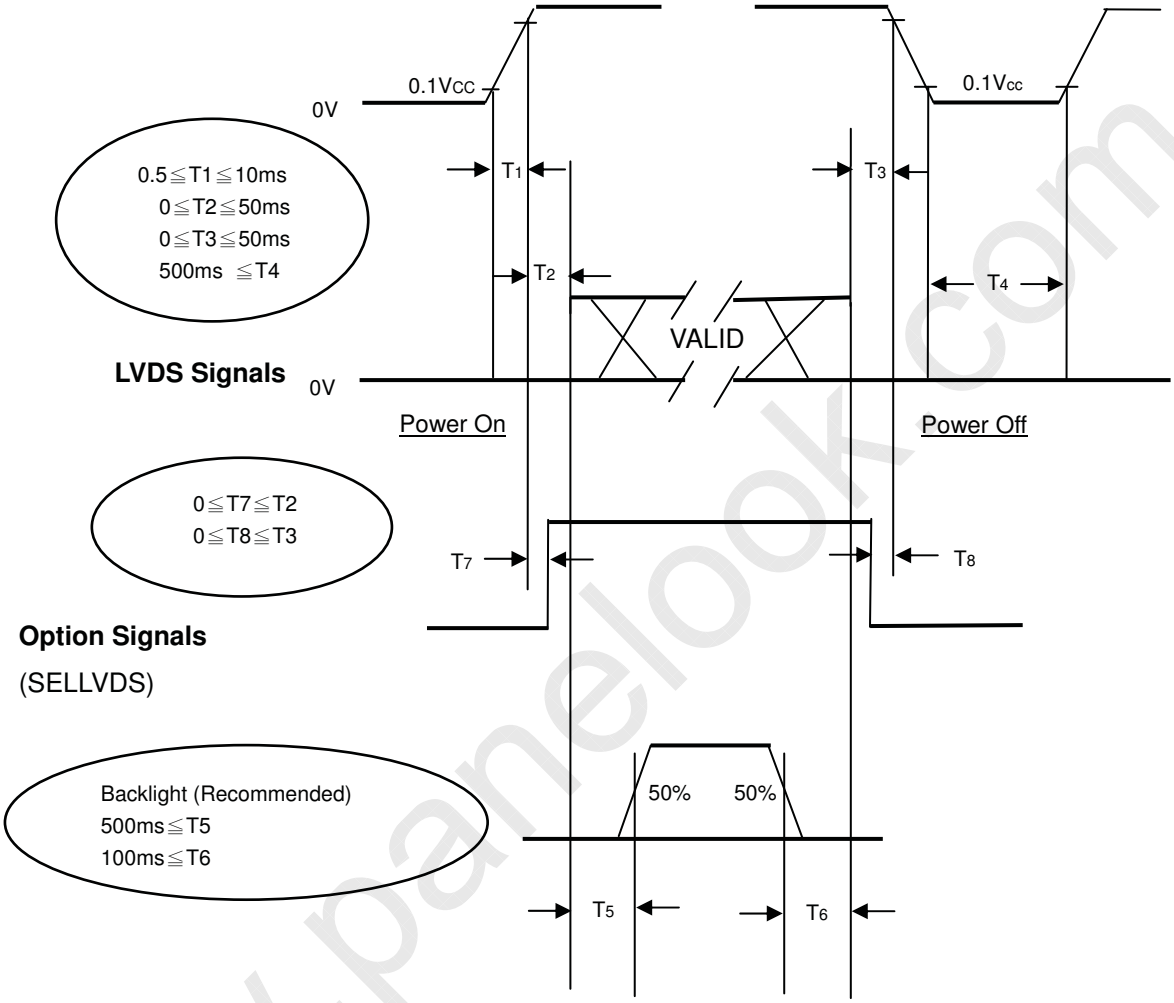
**LVDS RECEIVER INTERFACE TIMING DIAGRAM**



### 6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.




**Power ON/OFF Sequence**

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failures.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

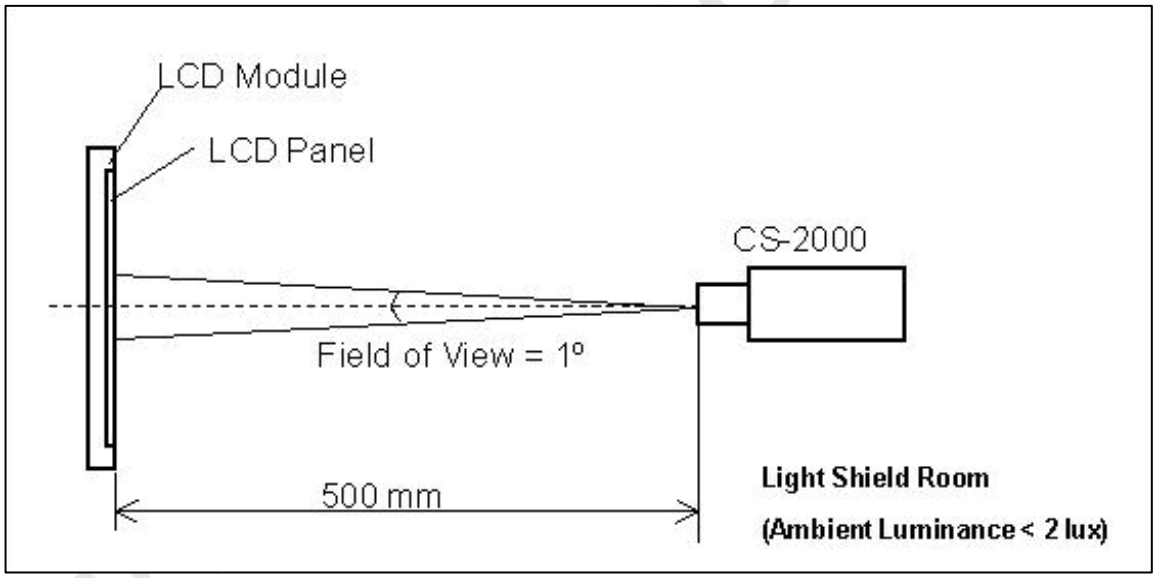
Note (5) Interface signal shall not be kept at high impedance when the power is on.

## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Ambient Temperature | Ta | 25±2 | °C |
| Ambient Humidity | Ha | 50±10 | %RH |
| Supply Voltage | VCC | 12 | V |
| Input Signal | According to typical value in "3. ELECTRICAL CHARACTERISTICS" | | |
| Lamp Current | IL | 10.5±0.5 | mA |
| Oscillating Frequency (Inverter) | FW | 63±3 | KHz |
| Vertical Frame Rate | Fr | 60 | Hz |

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



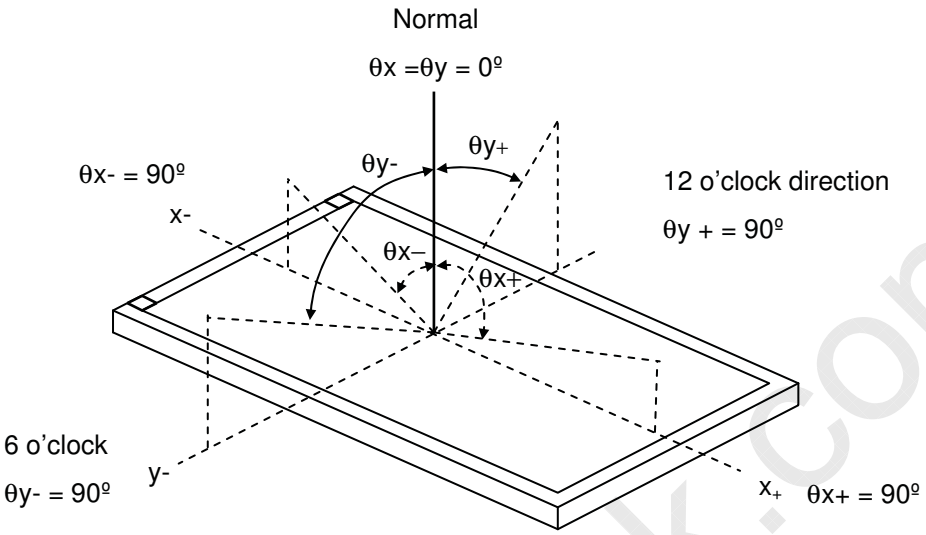
### 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | θx=0°, θy =0° Viewing angle at normal direction | 2250 | 3000 | - | - | (2) |
| Response Time (VA) | | Gray to gray | | - | 8.5 | - | ms | (3) |
| Center Luminance of White | | $L_C$ | | 350 | 400 | - | $cd/m^2$ | (4) |
| White Variation | | δW | | - | - | 1.3 | - | (6) |
| Cross Talk | | CT | | - | - | 4 | % | (5) |
| Color Chromaticity | Red | Rx | | Typ. -0.03 | 0.647 | Typ. +0.03 | - | - |
| | | Ry | | | 0.334 | | - | |
| | Green | Gx | | | 0.275 | | - | |
| | | Gy | | | 0.596 | | - | |
| | Blue | Bx | | | 0.143 | | - | |
| | | By | | | 0.068 | | - | |
| | White | Wx | | | 0.285 | | - | |
| | | Wy | | | 0.293 | | - | |
| | Color Gamut | C.G | | - | 72 | - | % | NTSC |
| Viewing Angle | Horizontal | θx+ | CR≥10 | 80 | 88 | - | Deg. | (1) |
| | | θx- | | 80 | 88 | - | | |
| | Vertical | θY+ | | 80 | 88 | - | | |
| | | θY- | | 80 | 88 | - | | |

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Conoscope Cono-80




Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

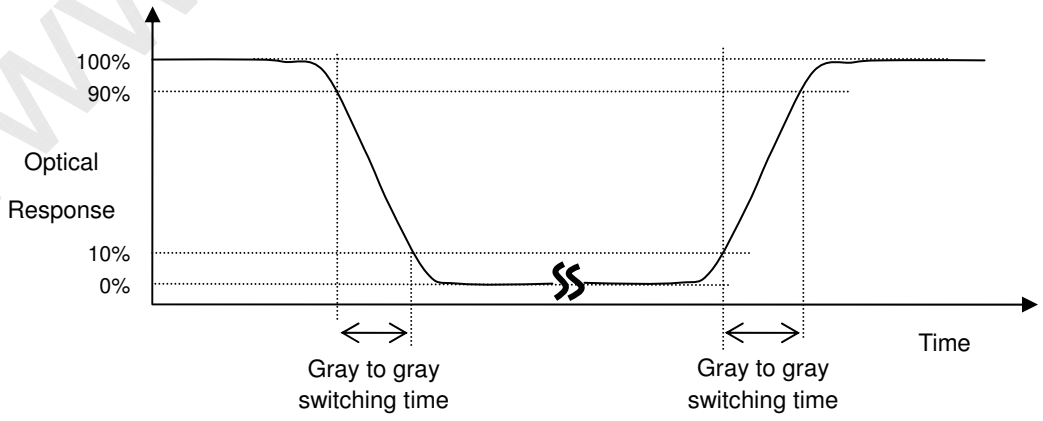
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:




The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (4) Definition of Luminance of White ($L_C$):

Measure the luminance of gray level 255 at center point and 5 points

$L_C$ = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

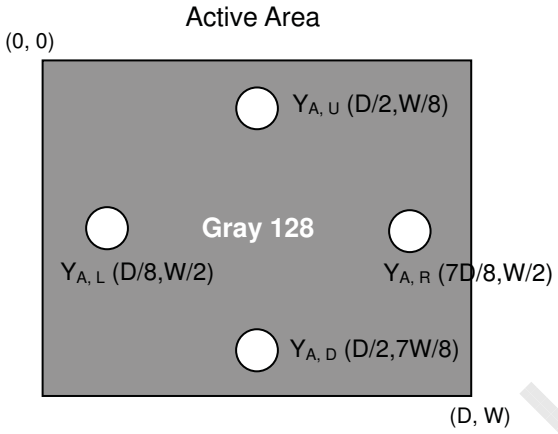
Note (5) Definition of Cross Talk (CT):

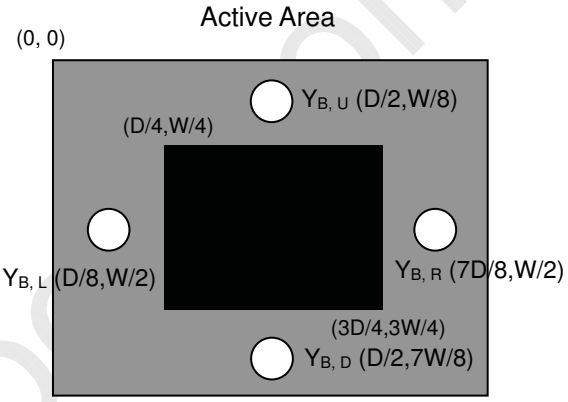
$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

$Y_A$ = Luminance of measured location without gray level 0 pattern (cd/m2)

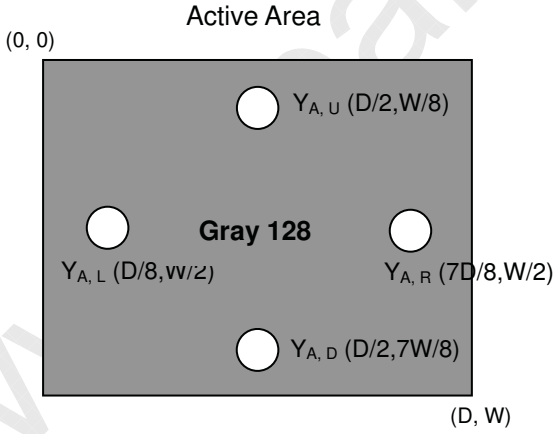
$Y_B$ = Luminance of measured location with gray level 0 pattern (cd/m2)

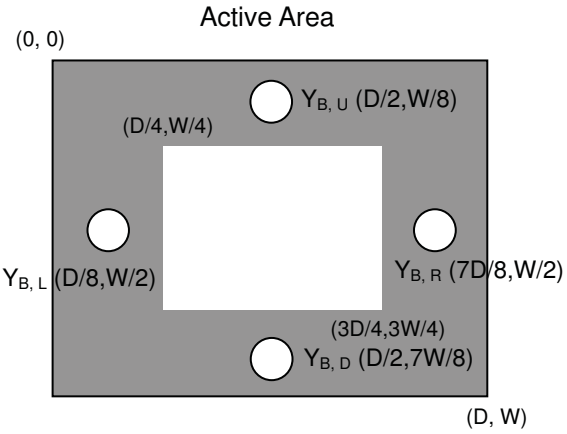



$Y_A$ = Luminance of measured location without gray level 255 pattern (cd/m2)

$Y_B$ = Luminance of measured location with gray level 255 pattern (cd/m2)

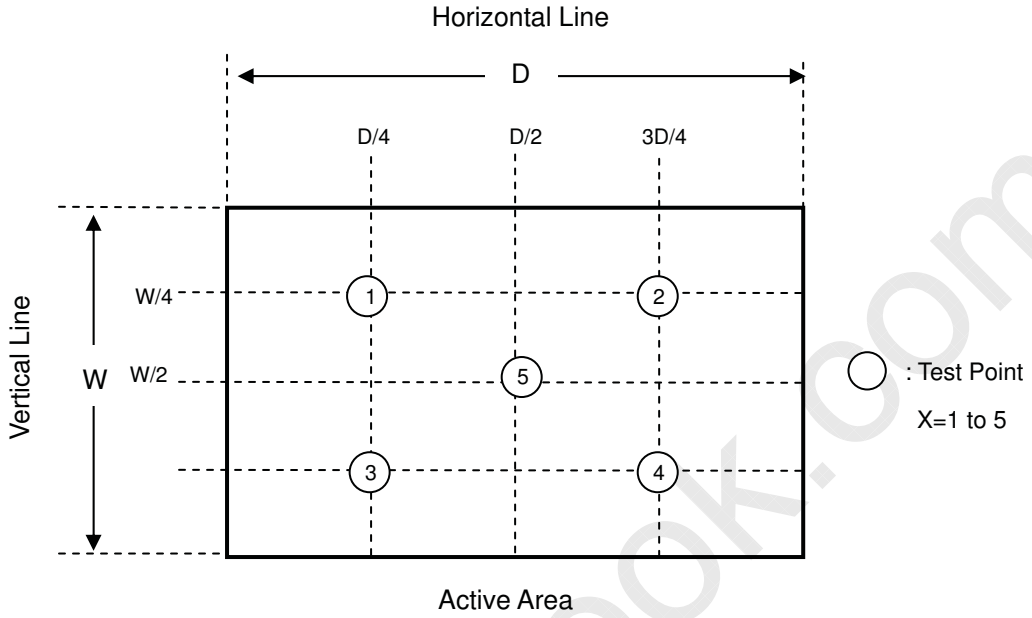


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



## PRECAUTIONS

### 8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[ 1 ] Do not apply rough force such as bending or twisting to the module during assembly.

[ 2 ] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[ 3 ] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[ 4 ] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMIS LSI chips.

[ 5 ] Do not plug in or pull out the I/F connector while the module is in operation.

[ 6 ] Do not disassemble the module.

[ 7 ] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[ 8 ] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[ 9 ] When storing modules as spares for a long time, the following precaution is necessary.

[ 9.1 ] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[ 9.2 ] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[ 10 ] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

### 8.2 SAFETY PRECAUTIONS

[ 1 ] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

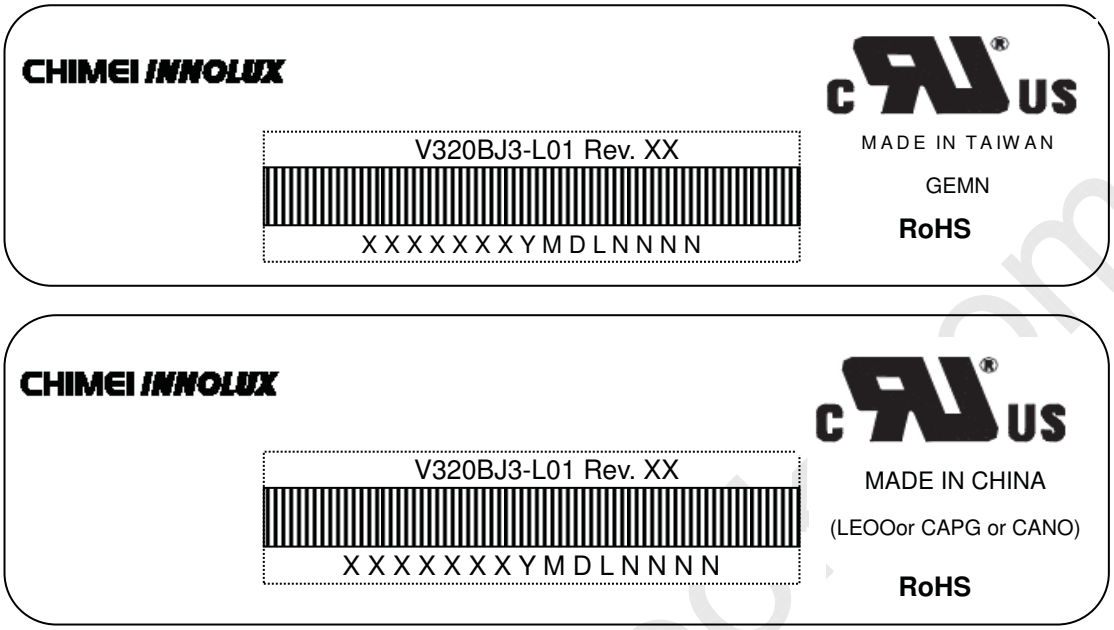
[ 2 ] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[ 3 ] After the module's end of life, it is not harmful in case of normal operation and storage.

## 9. DEFINITION OF LABELS

### 9.1 CMI MODULE LABEL

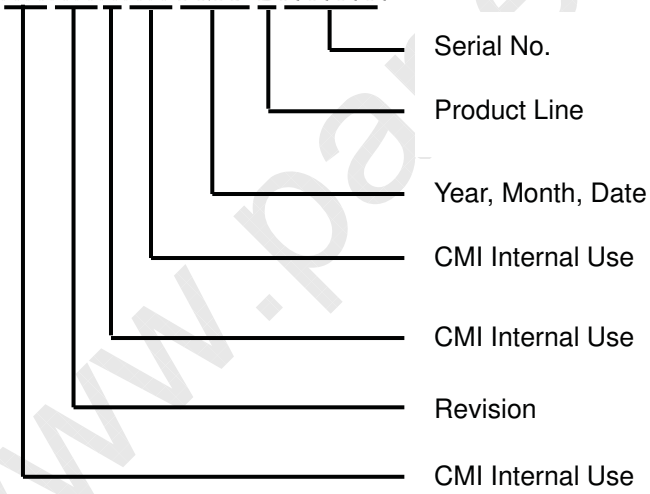
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.




Model Name: V320BJ3-L01

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N




Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, …etc.

## 10. PACKAGING

### 10.1 PACKAGING SPECIFICATIONS

(1) 5 LCD TV MODULES / 1 BOX

(2) BOX DIMENSIONS : 826(L)X376(W)X540(H)MM

(3) WEIGHT : APPROXIMATELY 28 KG (5 MODULES PER BOX)

### 10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

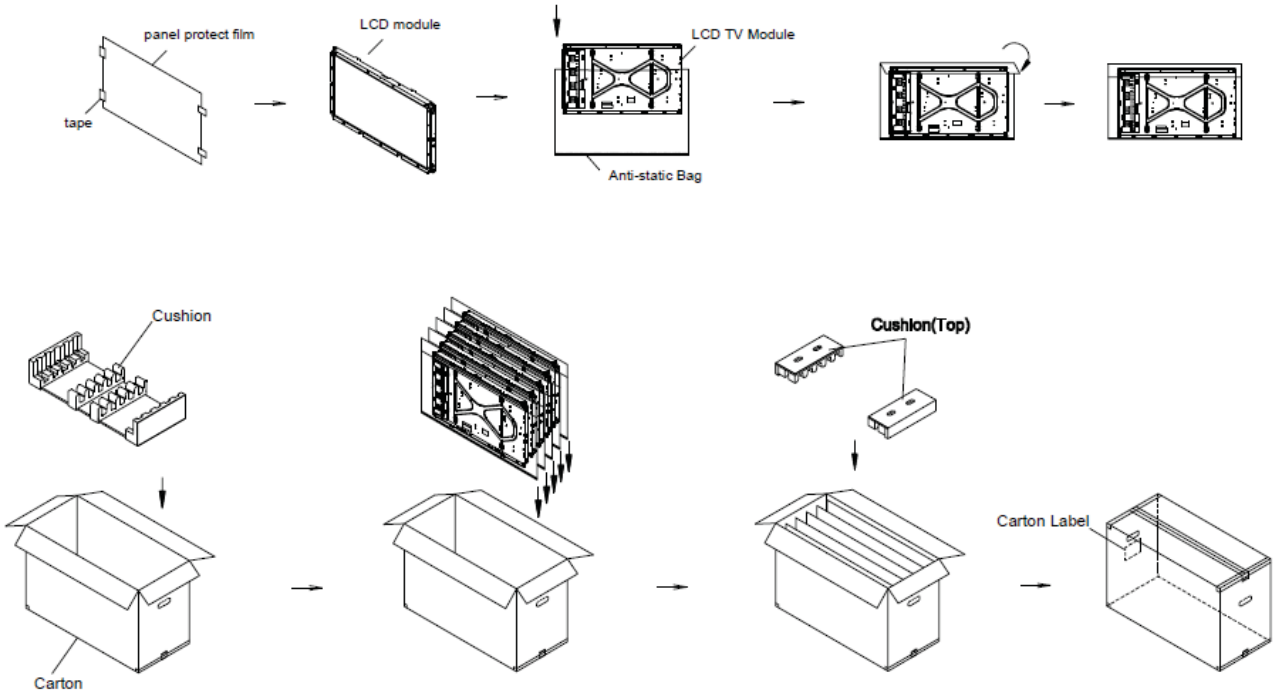



Figure. 10-1 Packing method

Sea / Land Transportation (40ft Container)

Air Transportation

Sea / Land Transportation (40ft HQ Container)

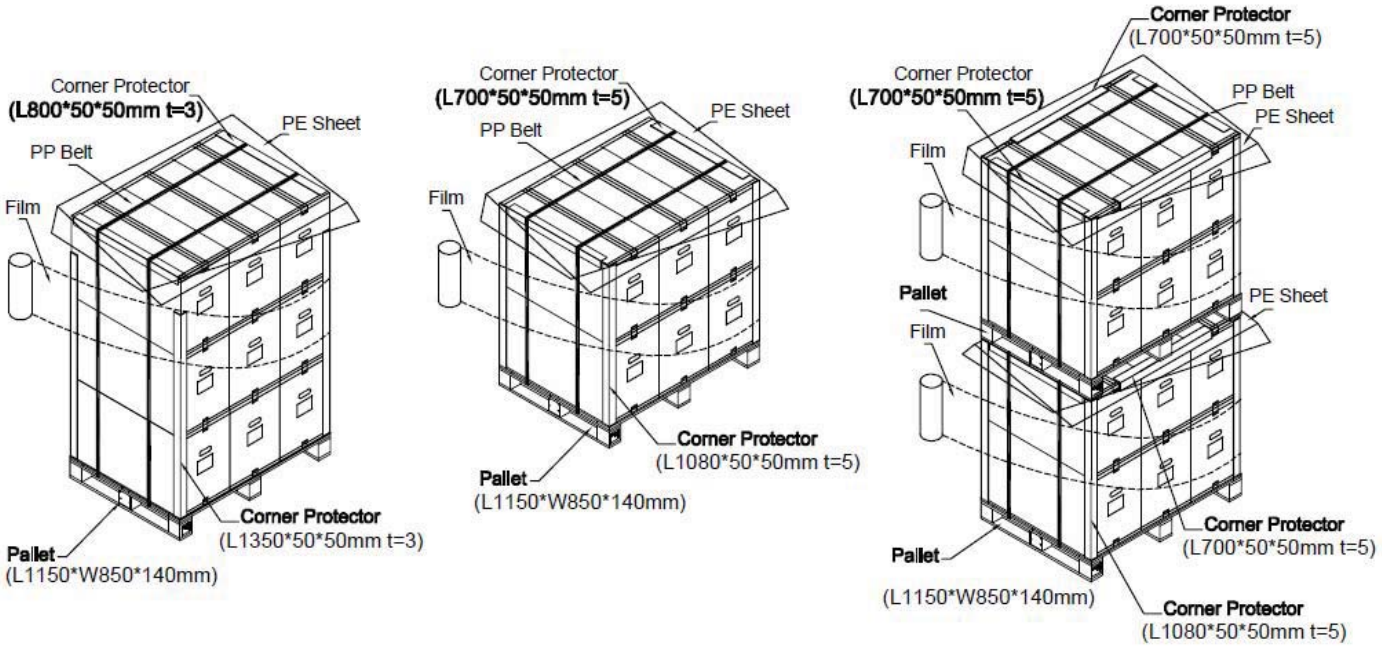



Figure. 10-2 Packing method

## 11. MECHANICAL CHARACTERISTIC