TFT LCD Approval Specification

MODEL NO.: V400H1 - P02

Customer: _____

Approved by: _____

Note:

Approved By	TVHD
	CC Chung

Reviewed By	QA Dept.	Product Development Div.
	Hsin-nan Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	Josh Chi	Karen Liao

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Nov. 19,'09	All	All	Approval Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V400H1-P02 is a 40" TFT Liquid Crystal Display cell with driver ICs and 2ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit colors). The backlight unit is not built-in.

1.2 CHARACTERISTICS

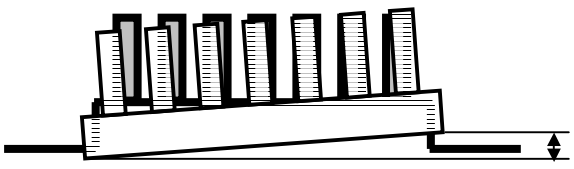
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	40
Pixels [lines]	1920 x 1080
Active Area [mm]	885.6(H) x 498.15 (V) (40" diagonal)
Sub -Pixel Pitch [mm]	0.15375 (H) x 0.46125 (V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 1908
Physical Size [mm]	Reference 2D Drawing
Display Mode	Transmissive mode / Normally black
Contrast Ratio	6500:1 Typ. (Typical value measured at CMO's module)
Glass thickness (Array/CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H),+88/-88(V) Typ. (Typical value measured at CMO's module)
Color Chromaticity	R=(0.635, 0.323) G=(0.285, 0.602) B=(0.148, 0.056) W=(0.280, 0.290) (Typical value measured at CMO's module)
Cell Transparency [%]	4.6% Typ. (Typical value measured at CMO's module)
Polarizer (CF side)	Super Wide View Glare coating, 1030.18 (H) x 586.37(w).. Hardness: 3H
Polarizer (TFT side)	Super Wide View, 1030.18(H) x 586.37(w).

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	2260	2560	2860	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ±0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position



+/- 0.5mm

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT (BASE ON CMO MODULE V400H1-L08)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	30	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

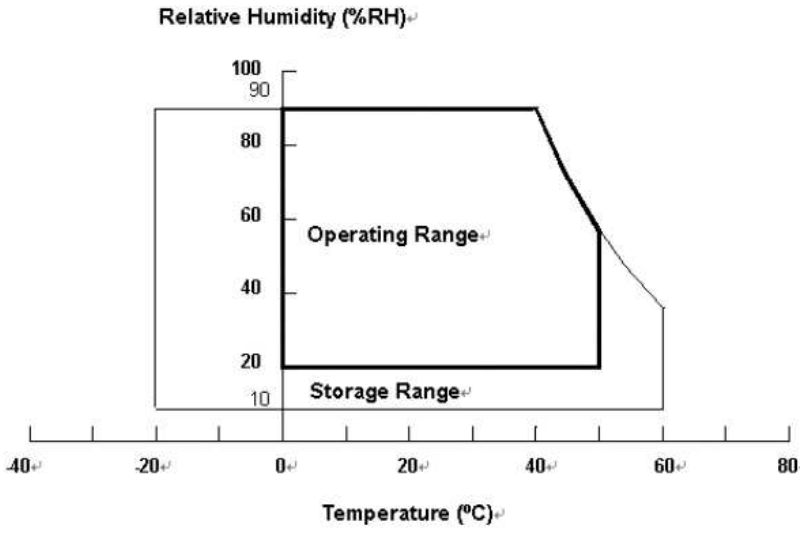
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

Storage condition: With shipping package.

Storage temperature rang: 25±5℃

Storage humidity range: 50±10%RH

Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

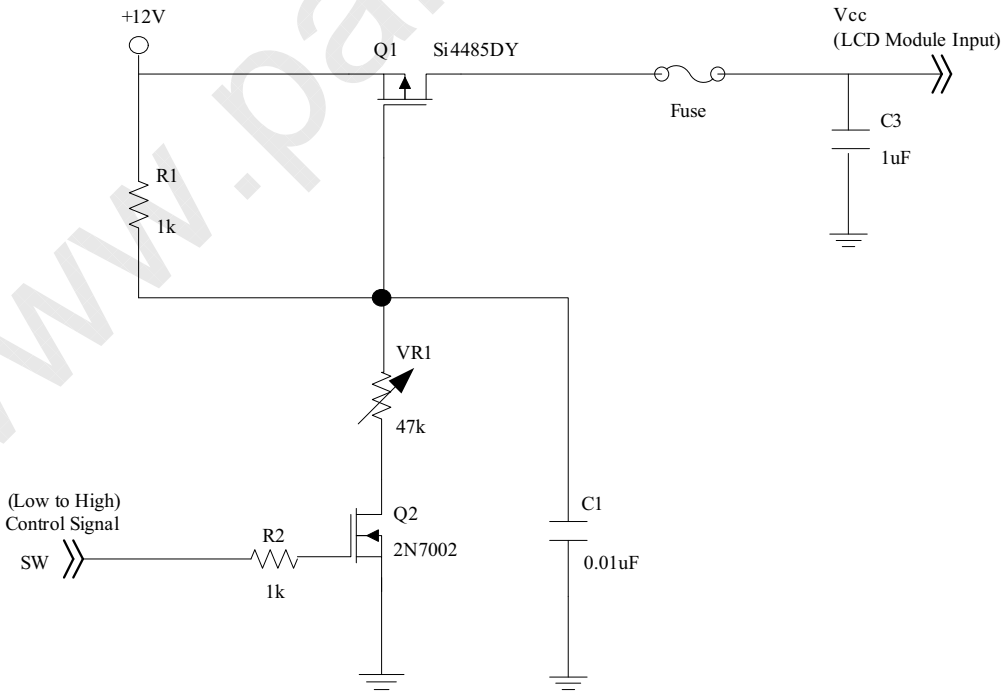
3.1 TFT LCD OPEN CELL

(Ta = 25 ± 2 ºC)

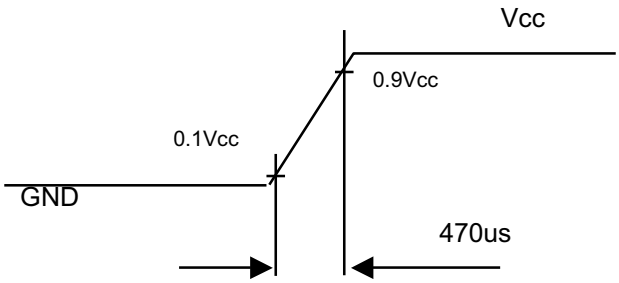
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	2.4	A	(2)
Power Supply Current	White Pattern	-	-	0.8	-	A	(3)
	Black Pattern	-	-	0.4	-	A	
	Horizontal Stripe	-	-	1.0	1.3	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, fv = 60 Hz, whereas a power dissipation check pattern below is displayed.

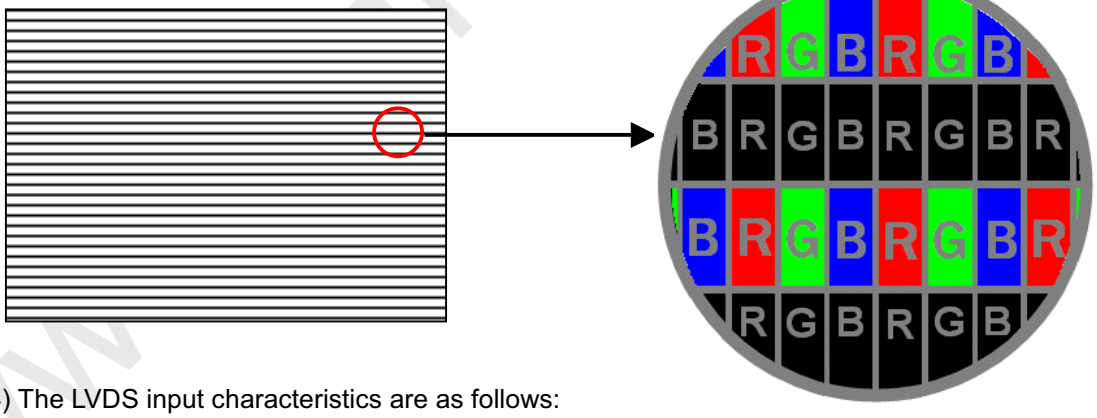
a. White Pattern

Active Area

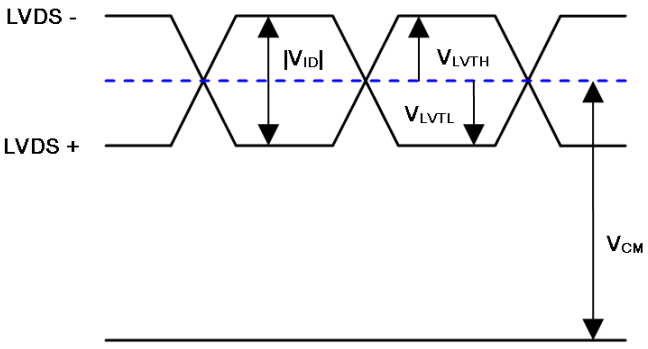
b. Black Pattern

Active Area

c. Horizontal Pattern

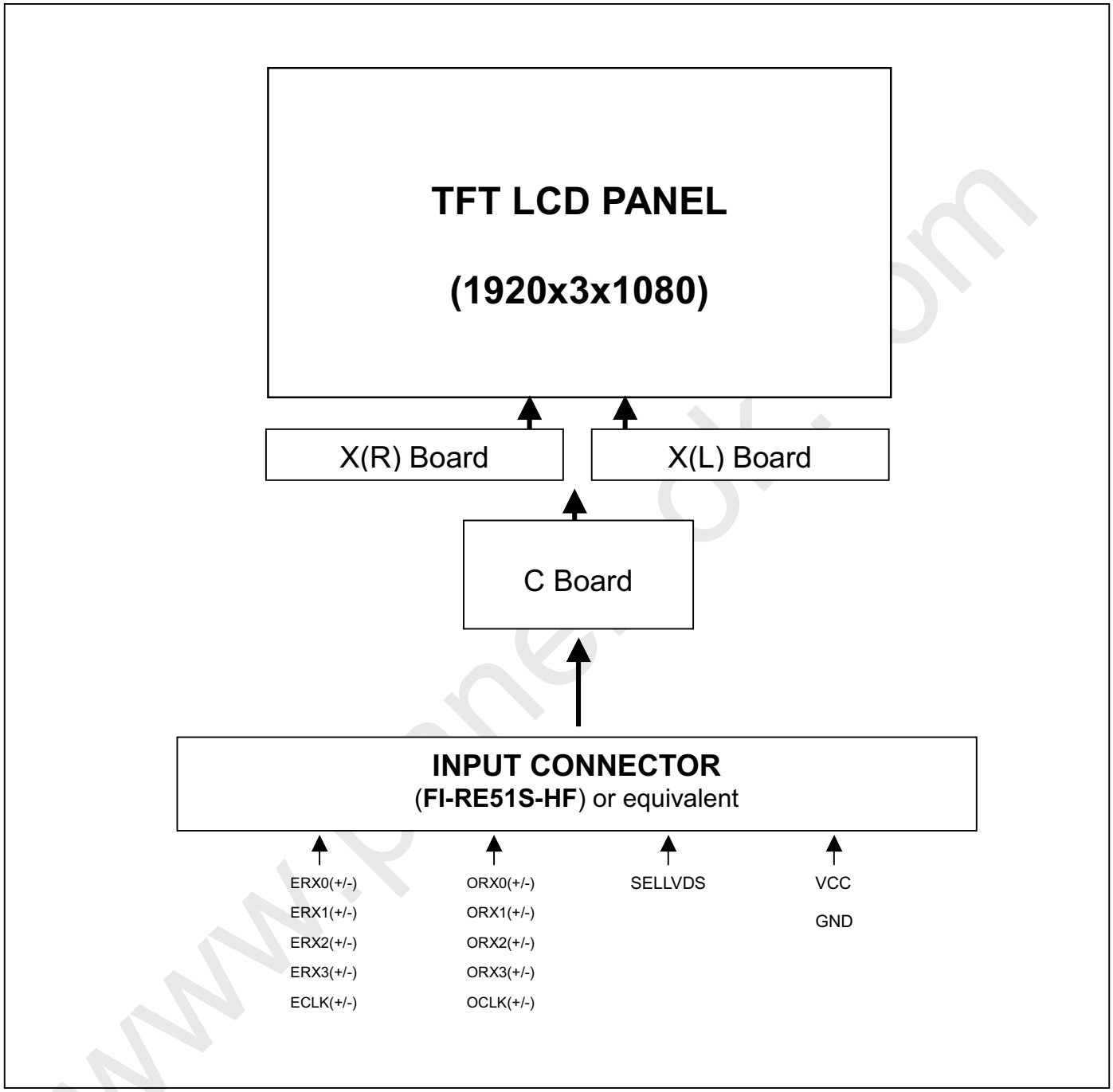


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM

4.1 TFT LCD OPEN CELL



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module

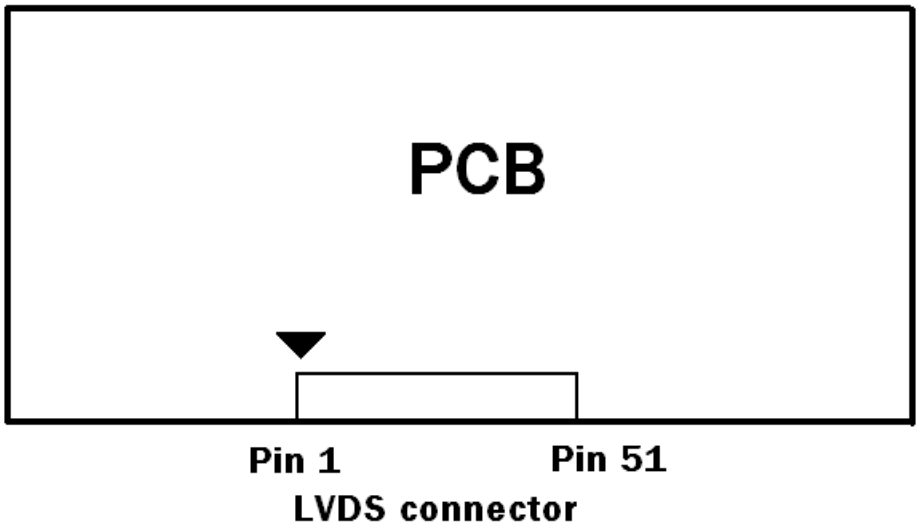
CNF1 Connector Pin Assignment

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(1)
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input	(1)
18	OCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(1)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(3)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(1)
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input.	(1)
33	ECLK+	Even pixel Positive LVDS differential clock input.	

34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(1)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(3)
38	N.C.	No Connection	
39	GND	Ground	
40	SCL	EEPROM Serial Clock	
41	N.C.	No Connection	(3)
42	N.C.	No Connection	
43	WP	EEPROM Write Protection	
44	SDA	EEPROM Serial Data	
45	LVDS_SEL	High(3.3V) or open for VESA, Low (GND) for JEIDA	(4)
46	N.C.	No Connection	(3)
47	N.C.	No Connection	
48	N.C.	No Connection	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

Note (2) LVDS connector pin order defined as follows

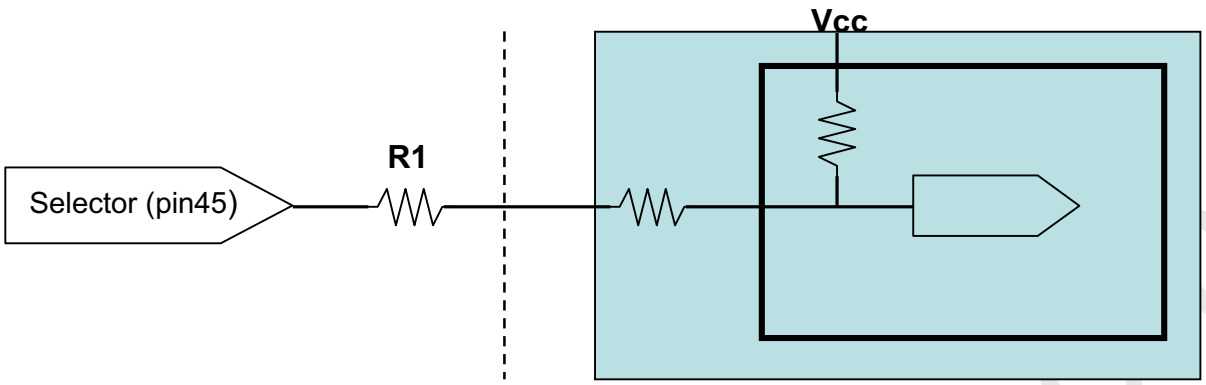


Note (3) Reserved for internal use. Please leave it open.

Note (4) Low: JEIDA LVDS Format (Connect to GND), High or open: VESA Format. (Connect to +3.3V)

Note (5) LVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)

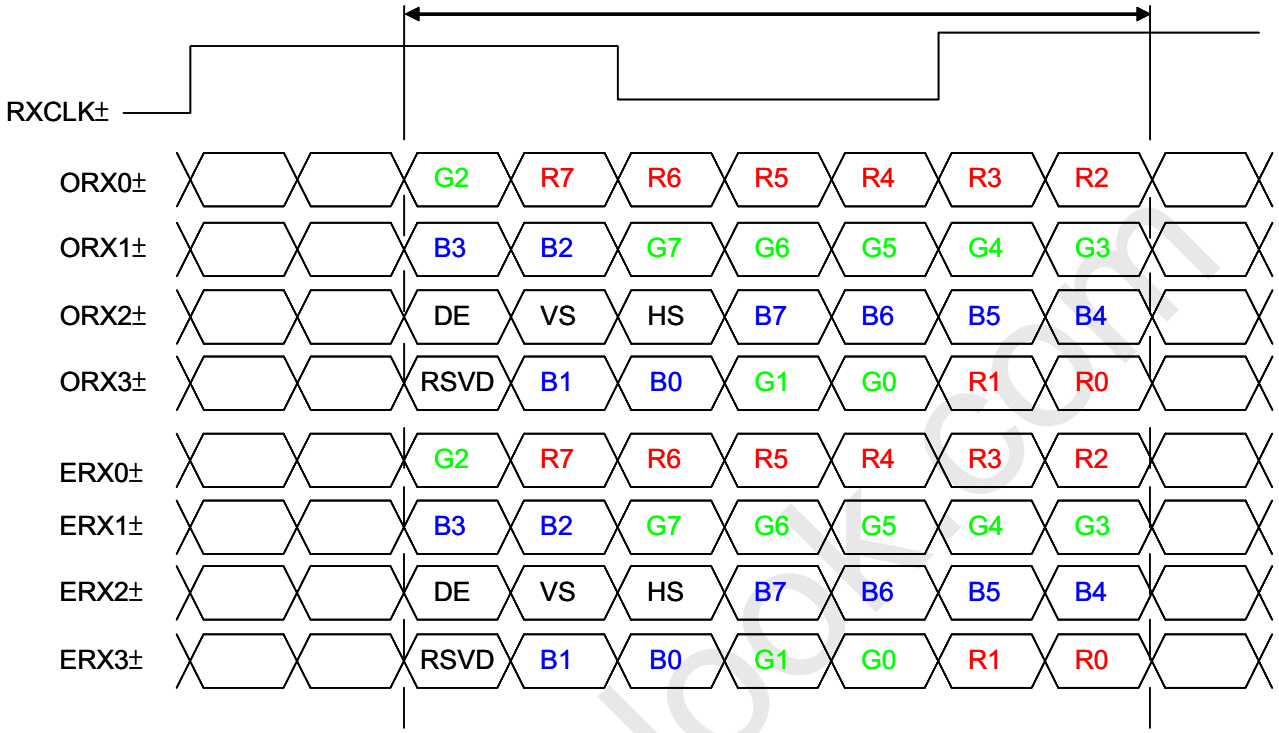


System side

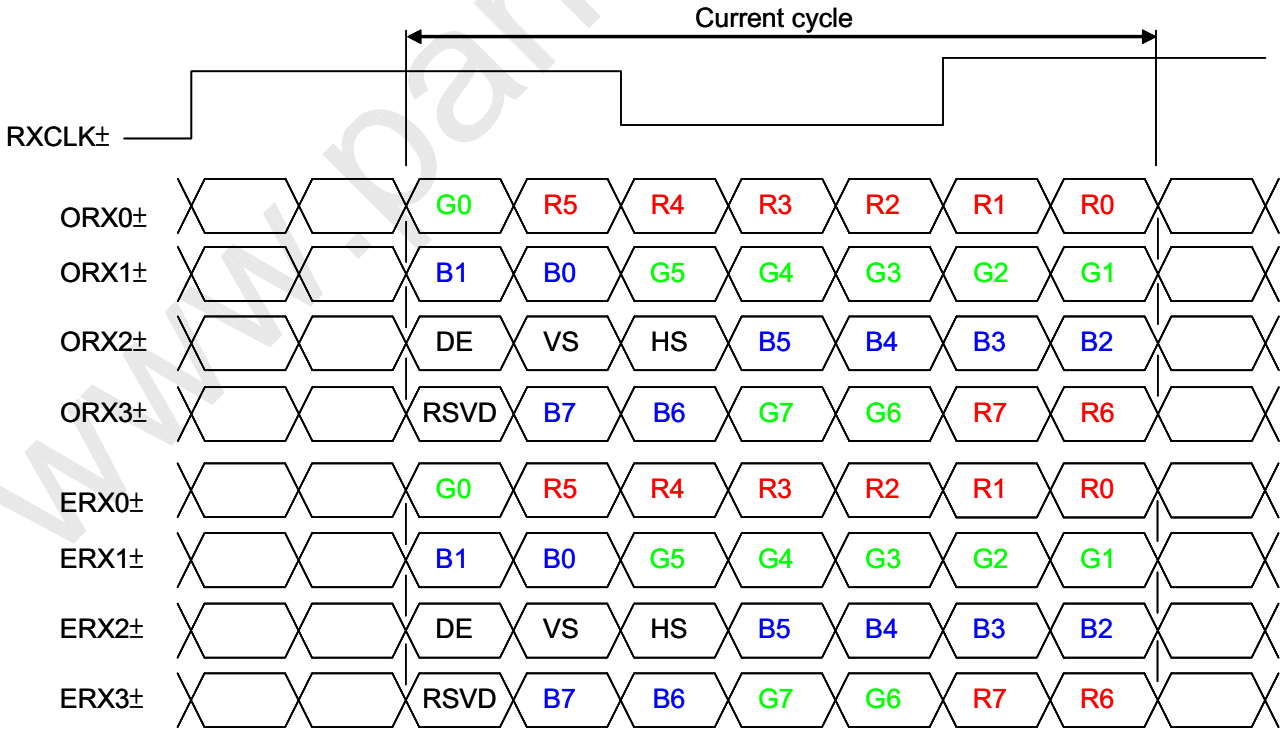
R1 < 1K

5.2 LVDS INTERFACE

JEDIA Format：SELLVDS=L



VESA Format：SELLVDS=H or Open



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

DCLK: Data clock signal

Notes (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	57	60	63	Hz	(6)
		F_{r6}	47	50	53	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	—
	Blank	Thb	90	140	190	Tc	—

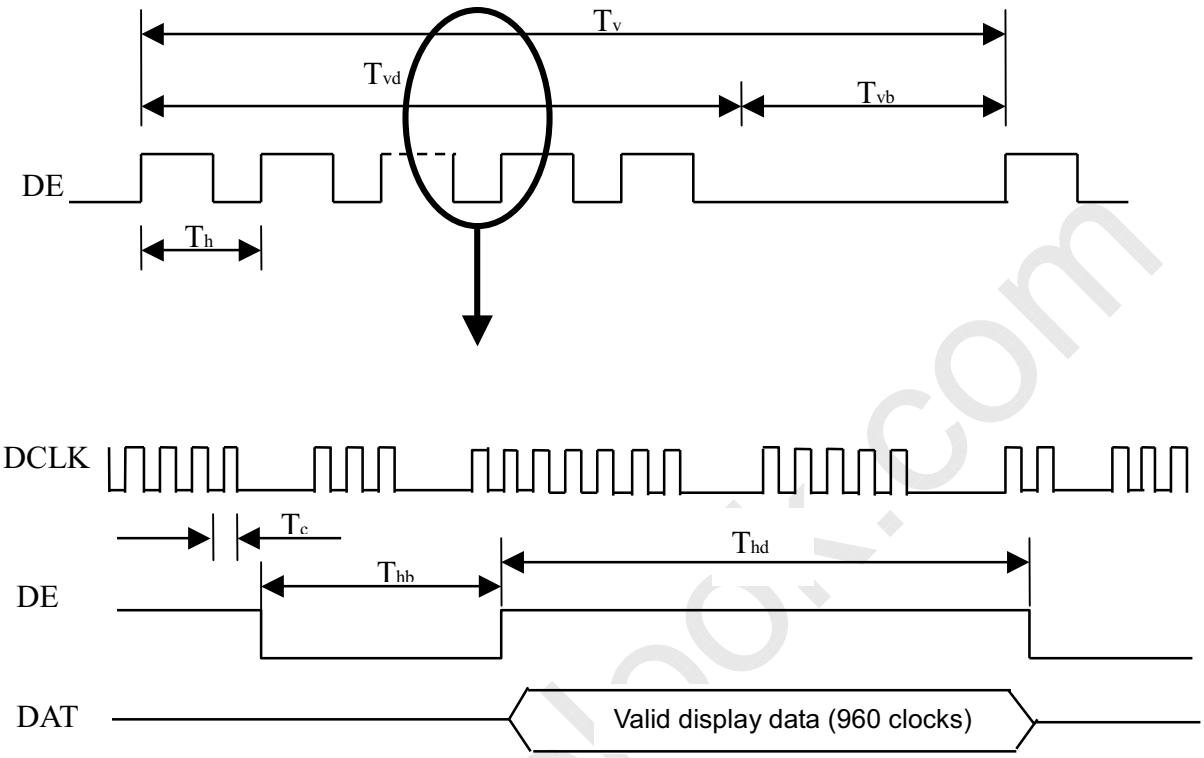
Note (1) Please make sure the range of pixel clock has follow the below equation：

$$Fclkin(max) \geqq Fr6 \times Tv \times Th$$

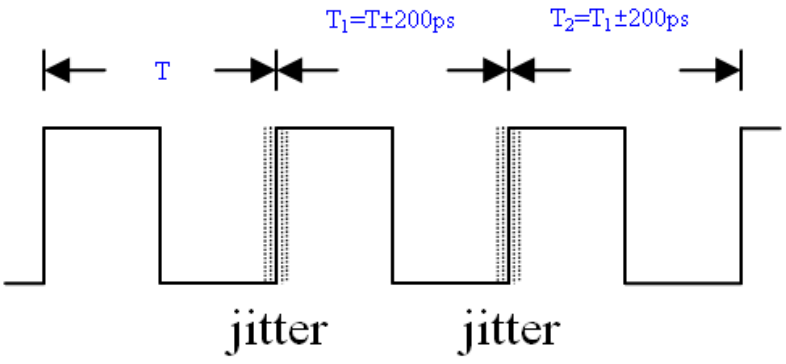
$$Fr5 \times Tv \times Th \geqq Fclkin(min)$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below：

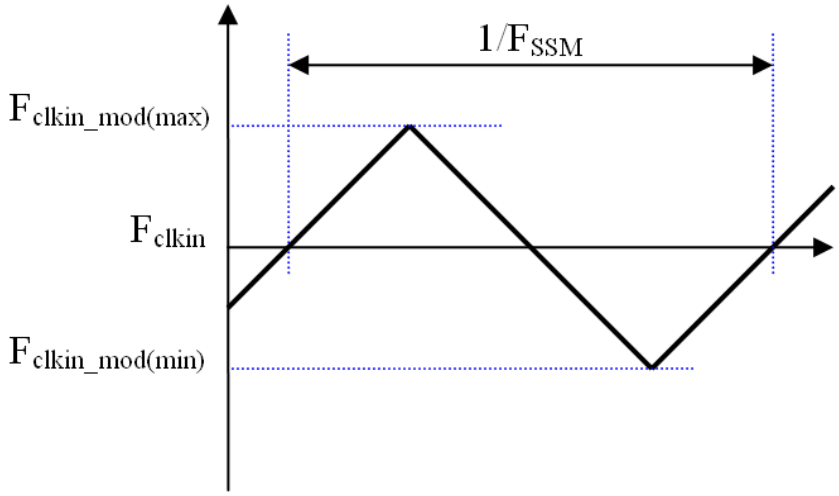
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T1 – TI

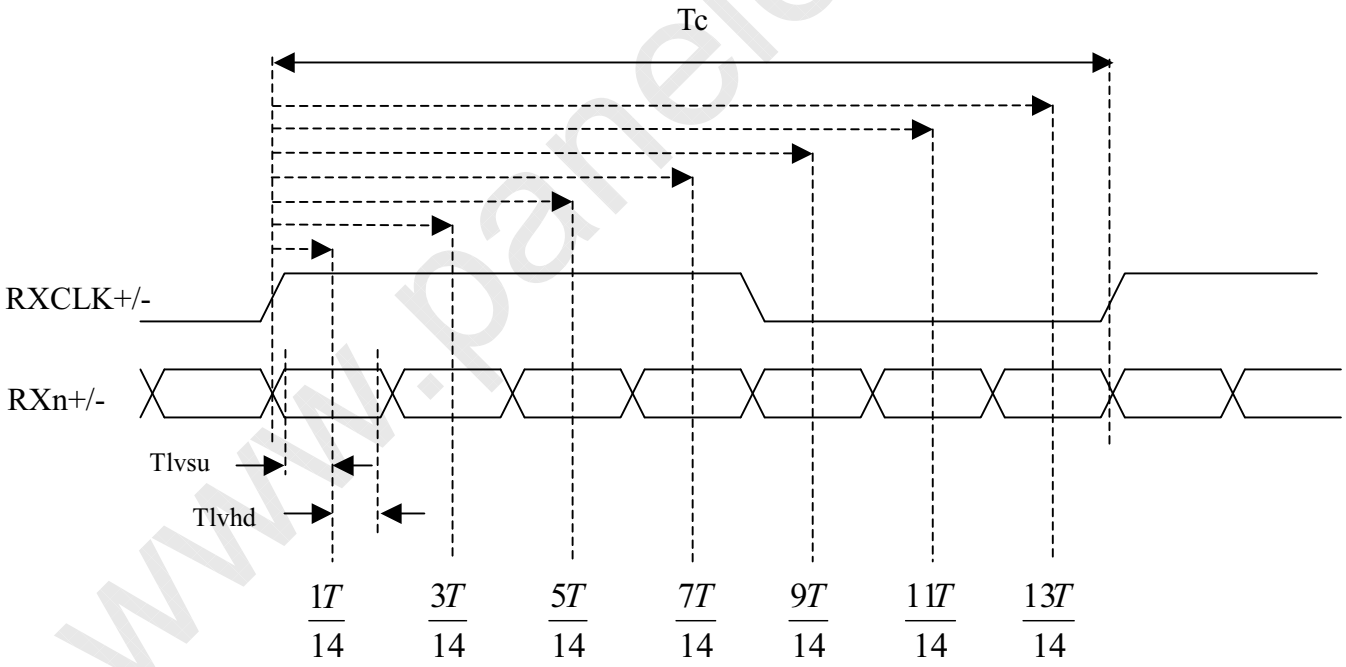


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

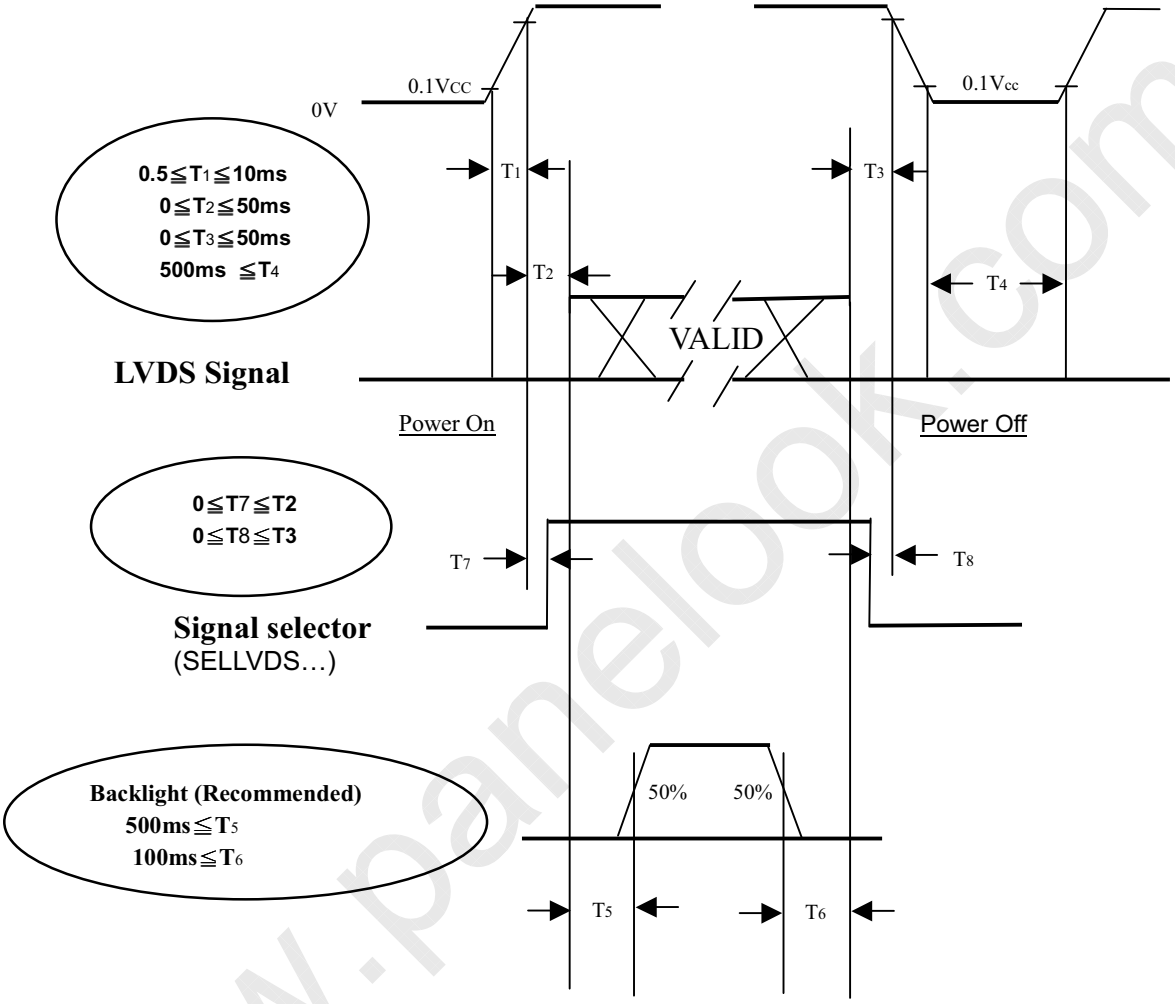


Note (6) (ODSEL) = H/L or open for 50/60Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note：

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Vertical Frame Rate	Fr	60	Hz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (7).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		4600	6500	-	-	(2), (4)
Response Time		Gray to gray	θ_x=0°, θ_Y =0° With CMO Module	-	6.5	12	ms	(5)
Center Transmittance		T%		-	4.6	-	%	(2)
White Variation		δW		-	-	1.3	-	(2), (7)
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° CS-1000T Standard light source "C"	Typ - 0.03	0.647	Typ + 0.03	-	(1), (6)
		Rcy			0.327		-	
	Green	Gcx			0.296		-	
		Gcy			0.600		-	
	Blue	Bcx			0.144		-	
		Bcy			0.083		-	
	White	Wcx			0.335		-	
		Wcy			0.379		-	
Viewing Angle	Horizontal	θ_x+	CR≥20 With CMO Module	80	88	-	Deg.	(2), (3)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

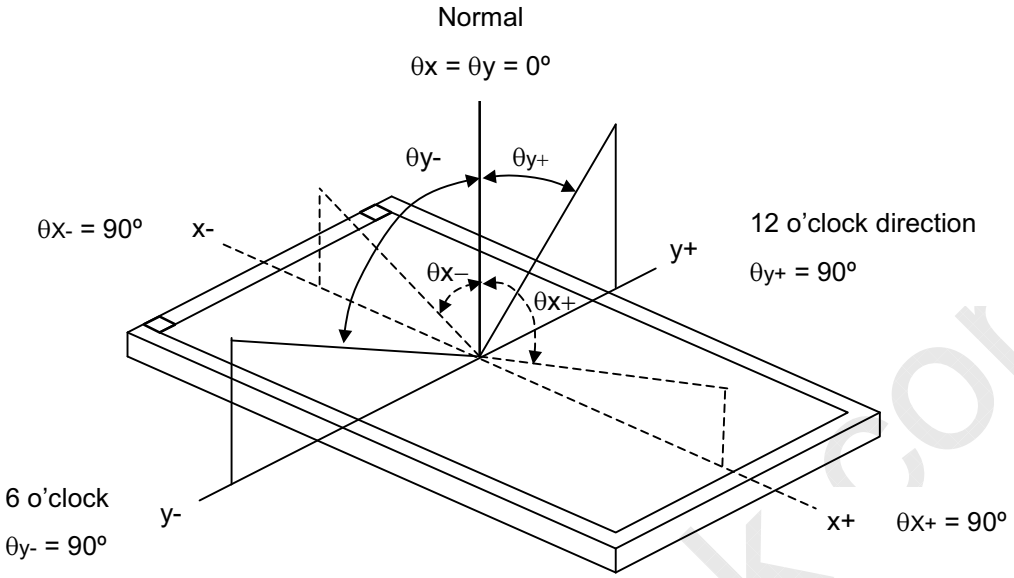
Note (1) Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following：

1. Measure Module's and BLU's spectrums. W, R, G, B are with signal input. BLU (for V400H1-L08) is supplied by CMO.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C"

Note (2) Light source is the BLU which is supplied by CMO and driving voltages are based on suitable gamma voltages.

Note (3) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

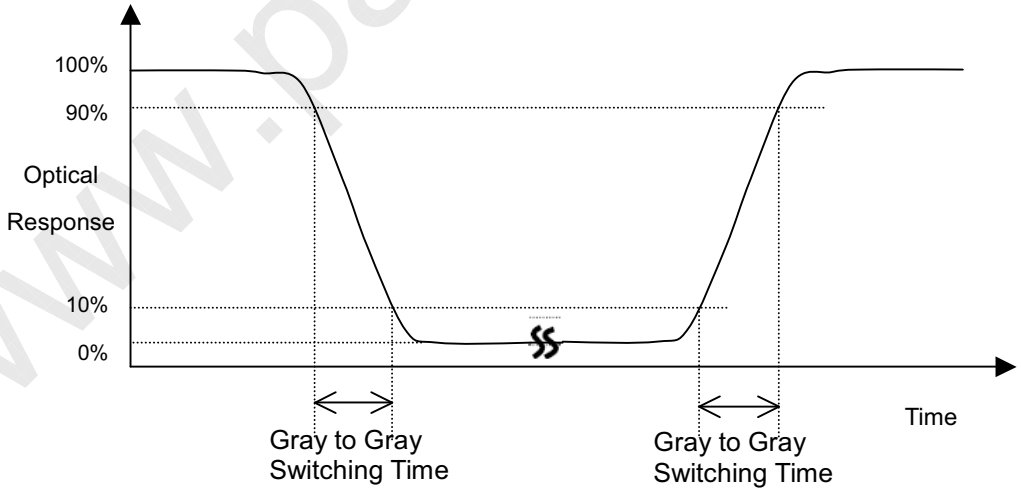
Contrast Ratio (CR) = L255 / L0

L1023: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1), where CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (7).

Note (5) Definition of Gray to Gray Switching Time:

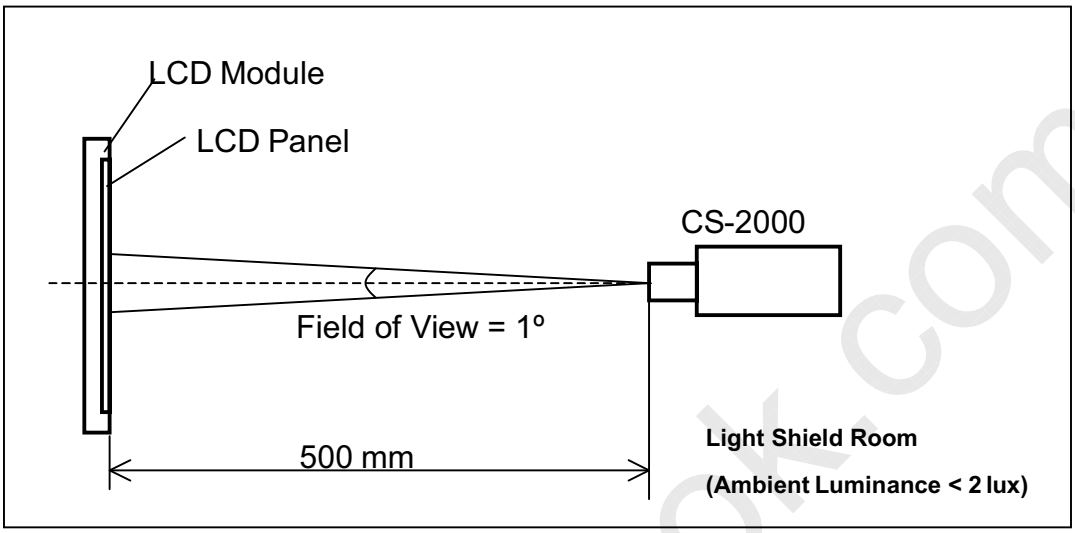


The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0, 63, 127, 191, 255 to each other.

Note (6) Measurement Setup:

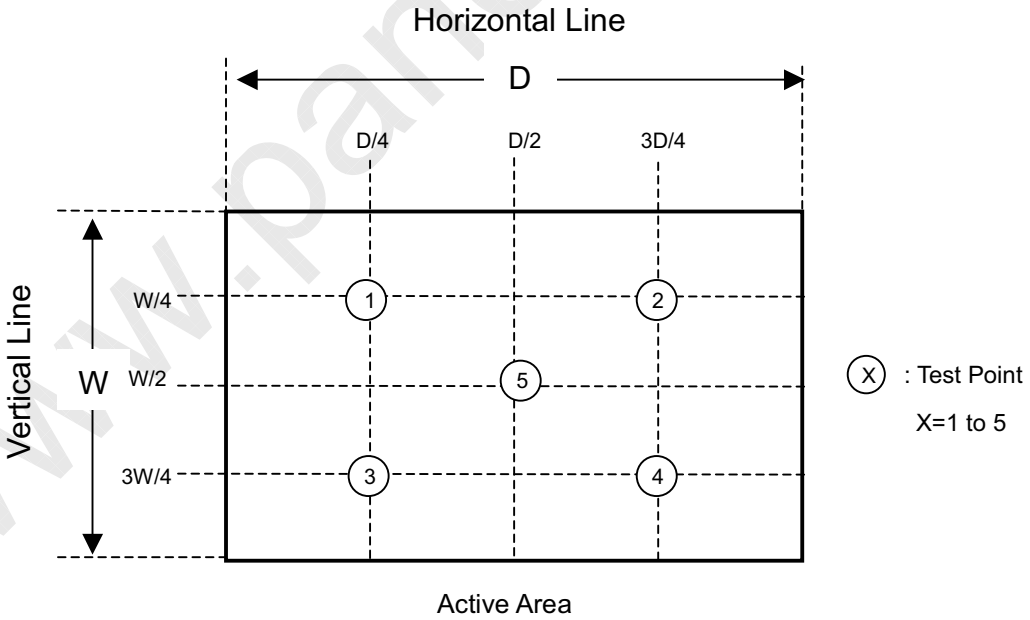
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. DEFINITION OF LABELS

8.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMO internal control.

V400H1-P02

XXXXXXXXXXXXX

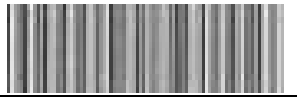
8.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation

P.O. NO._____

Parts ID._____

Carton ID._____ Quantities __12__



XXXXXXXXXXXXX

Made in Taiwan

(a) Model Name: V400H1– P02

(b) Carton ID: CMO internal control

(c) Quantities: 12

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 12pcs LCD TV Panels / 1 Box

(2) Box dimensions: 1108 (L) X 738 (W) X 252 (H)

(3) Weight: approximately 36 Kg

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

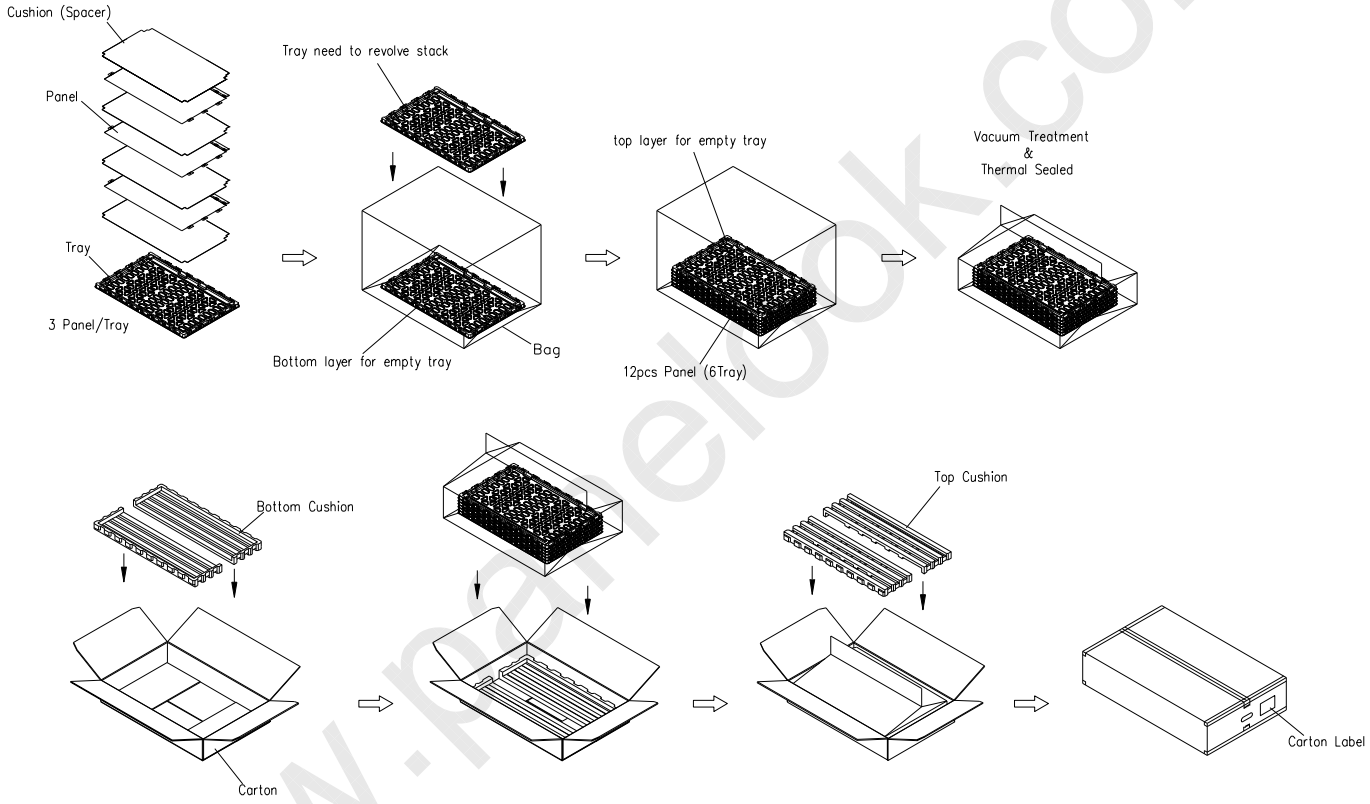
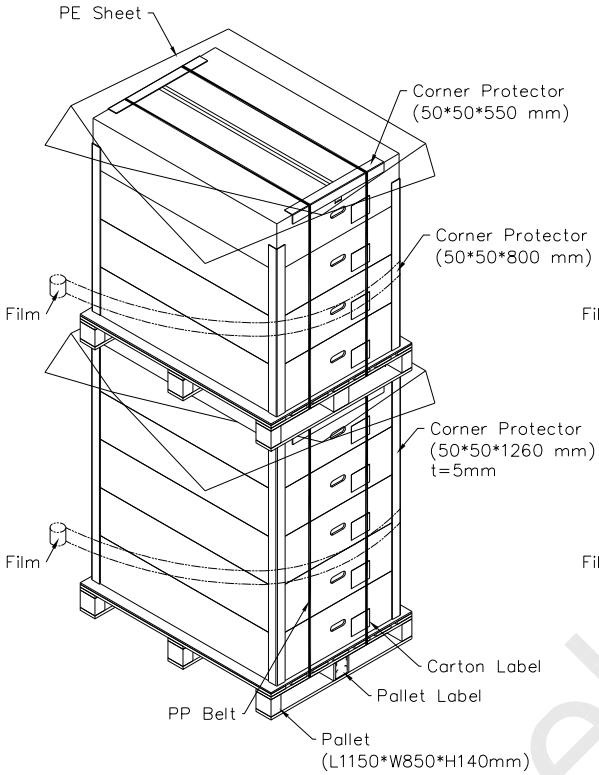
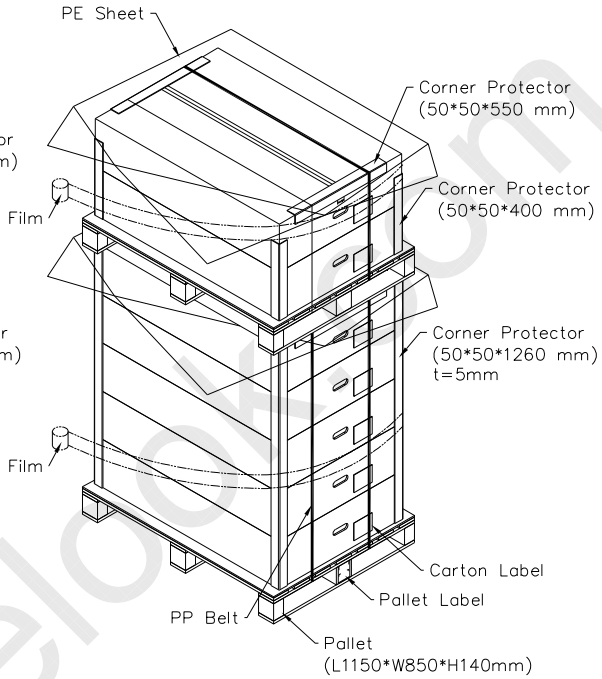


Figure.9-1 packing method

Sea / Land Transportation
(40ft HQ Container)



Sea / Land Transportation



Air Transportation

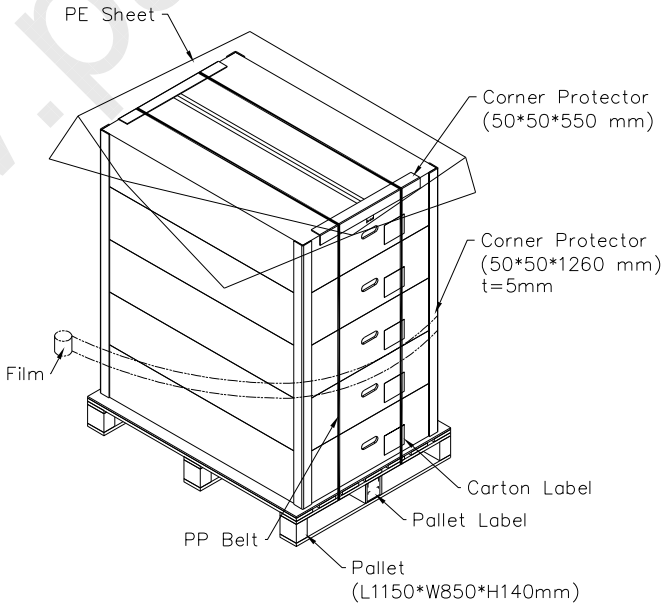


Figure. 9-2 Packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the product during assembly.

(2) To assemble backlight or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel will be damaged.

(4) Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(7) It is dangerous that moisture come into or contacted the product, because moisture may damage the product when it is operating.

(8) High temperature or humidity may reduce the performance of module. Please store this product within the specified storage conditions.

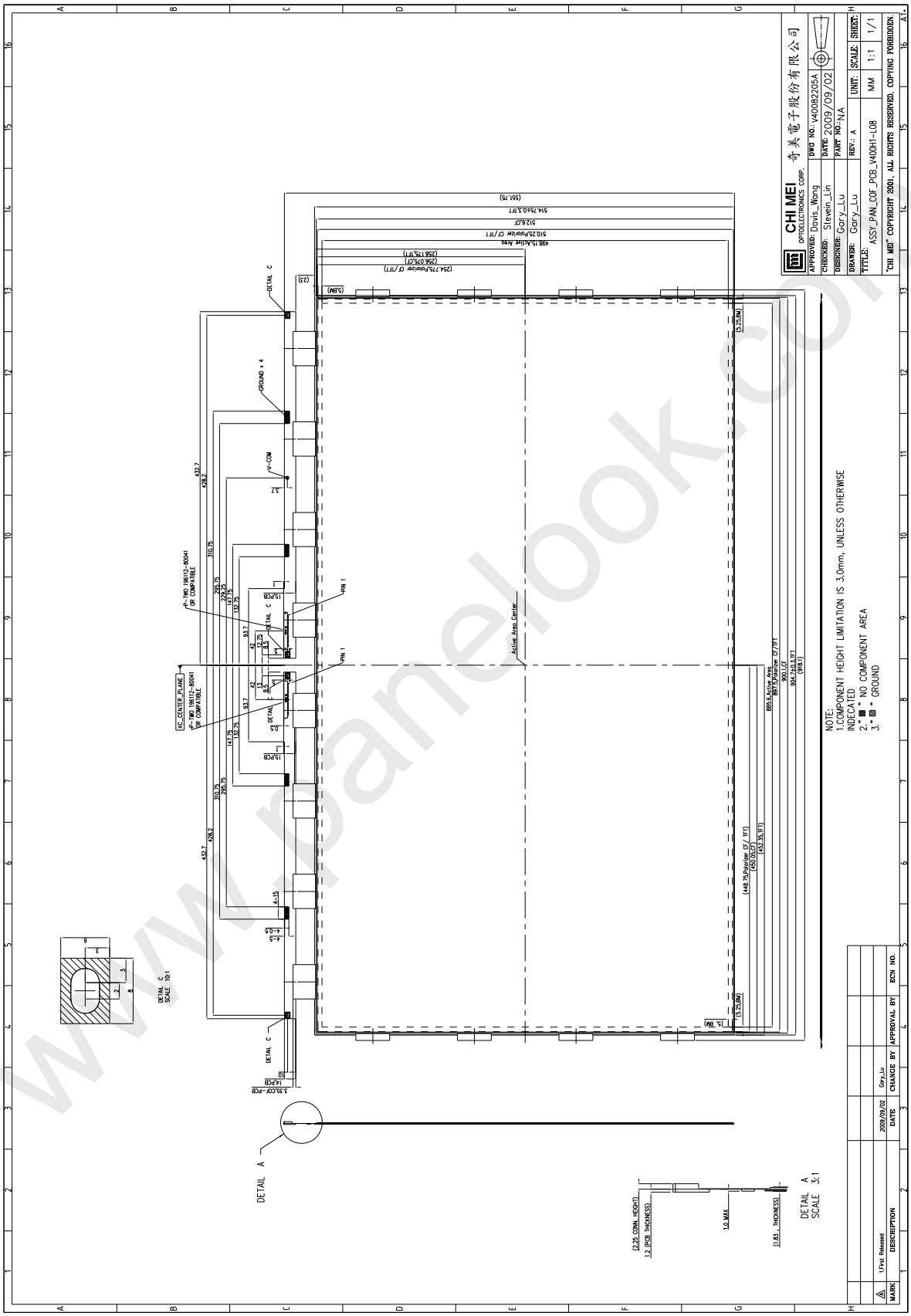
(9) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

10.2 SAFETY PRECAUTIONS

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the product's end of life, it is not harmful in case of normal operation and storage.

11. MECHANICAL CHARACTERISTICS



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