奇美電子
CHIMEI INNOLUX

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: V400HJ2

SUFFIX: PE2

Customer:

CONFIRMED BY   SIGNATURE

Name / Title _____   _____

APPROVED BY   SIGNATURE

Name / Title _____   _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Vincent Chou	Apple Wen

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Dec. 01, 2011	All	All	The approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V400HJ2-PE2 is a 40″ TFT Liquid Crystal Display product with driver ICs and 2 path mini-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit). The backlight unit is not built in.

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	40
Pixels [lines]	1920 × 1080
Active Area [mm]	885.6(H) × 498.15(V) (40″ diagonal)
Sub-Pixel Pitch [mm]	0.15375 (H) × 0.46125 (V)
Pixel Arrangement	RGB Vertical Stripe
Weight [g]	Typ. 1850 g
Physical Size [mm]	905.3×516.9 ×1.82mmTyp.
Display Mode	Transmissive Mode / Normallly Black
Contrast Ratio	Typ.5000:1 (Typical value measure by CMI's Module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H), +88/-88(V) Typ. (CR≧20) (Typical value measure by CMI's module)
Color Chromaticity	R = (0.642,0.331) G = (0.290,0.612) B = (0.149,0.055) W= (0.280,0.290) * Please refer to "color chromaticity" on p.25
Cell Transparency [%]	5.0 %
Polarizer Surface Treatment	Anti-Glare coating (Haze 11%)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	-	1850	-	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position

+/- 0.5mm
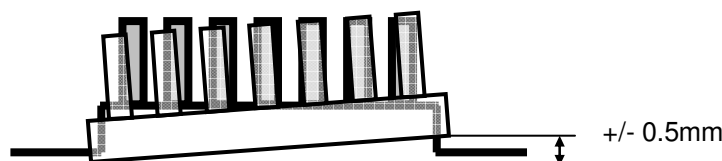
2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1) With CMI Module
Operating Ambient Temperature	TOP	0	50	°C	(1), (2) With CMI Module

Note (1) Temperature and relative humidity range is shown in the figure below.

      (a) 90 ％RH Max. (Ta $\leqq$ 40 °C).

      (b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

      (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.
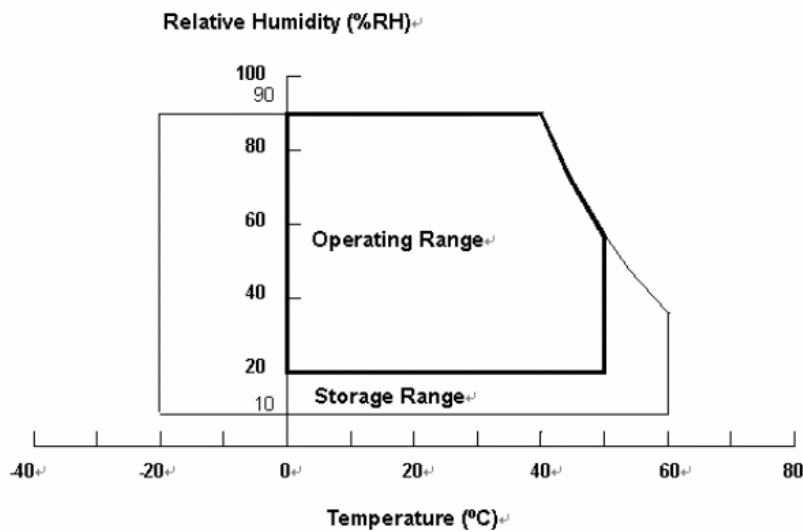
2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Recommended Storage Condition: With shipping package.

Recommended Storage temperature range: 25±5 ℃

Recommended Storage humidity range: 50±10%RH

Recommended Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

(Ta = 25 ± 2 ℃)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	3.2	A	(2)
Power Consumption	White Pattern	P_T	—	4.2	5	W	(3)
	Black Pattern			4.3	5.2		
	Horizontal Pattern			7	8.5		
Power Supply Current	White Pattern		—	—	0.35	0.42	A	(3)
	Black Pattern		—	—	0.36	0.43		
	Horizontal Pattern		—	—	0.58	0.71		
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$|V_{ID}|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition :
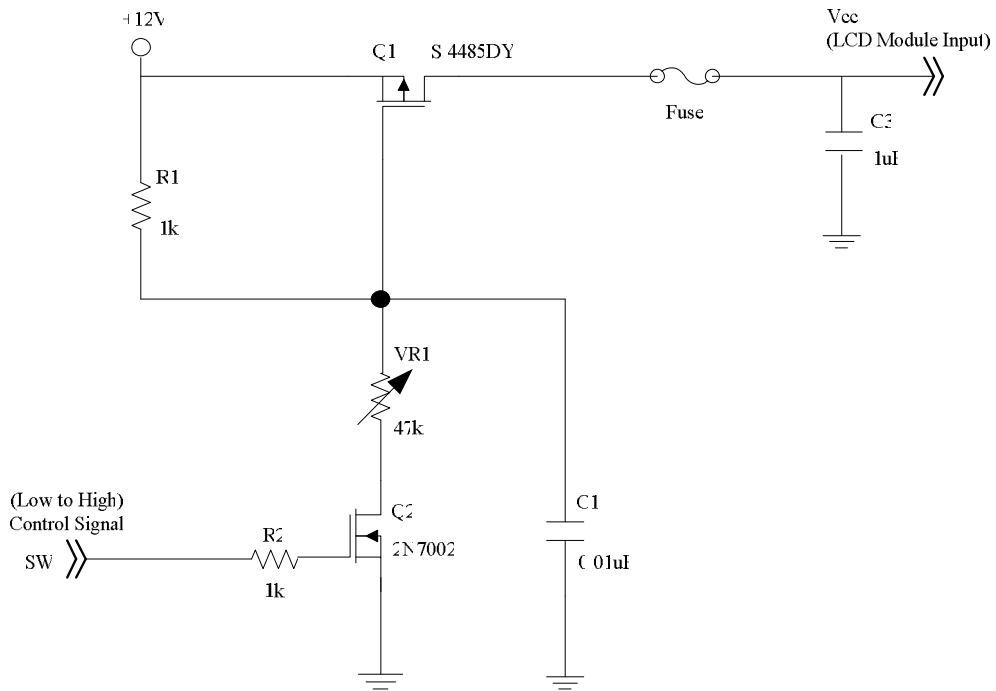
Vcc rising time is 470us
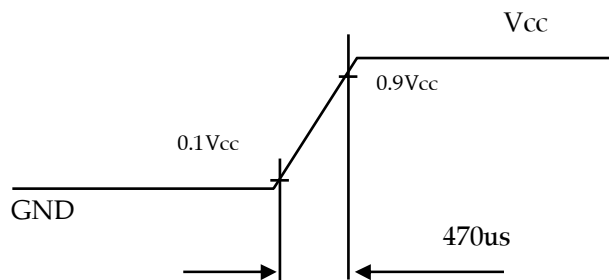
Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

b. Black Pattern

Active Area

Active Area
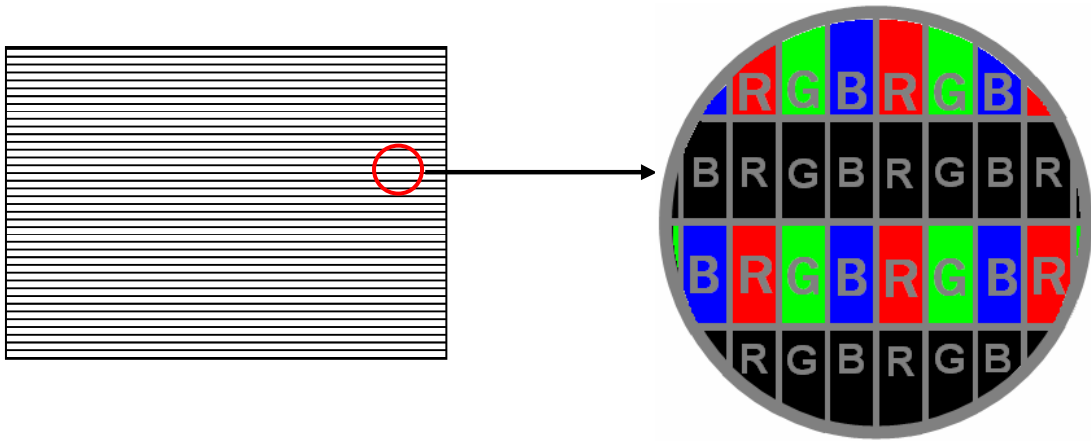
Note (4) The LVDS input characteristics are as follows :
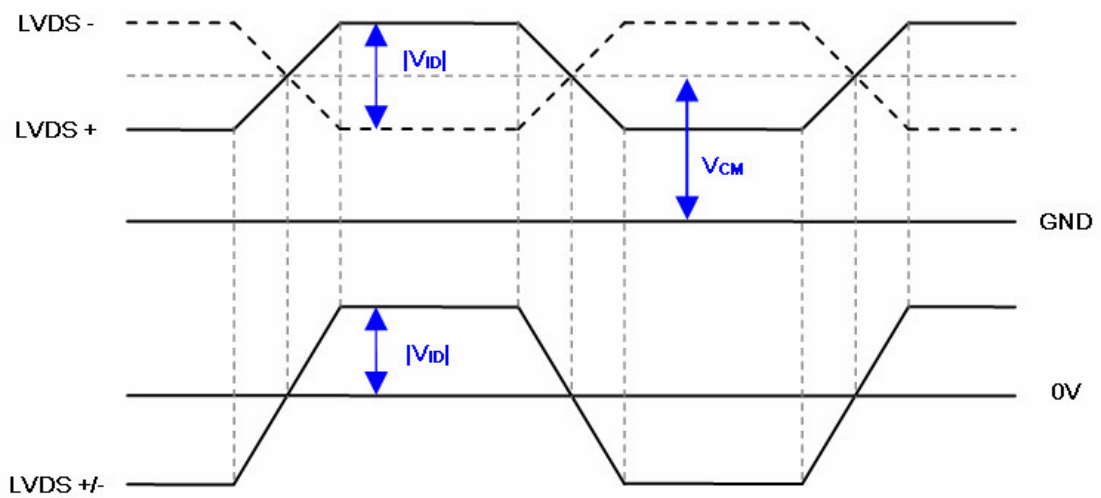
4. INPUT TERMINAL PIN ASSIGNMENT

4.1 TFT LCD OPEN CELL

TFT LCD PANEL

(1920x3x1080)

X(R) Board   X(L) Board

C Board

INPUT CONNECTOR
FI-RE51S-HF or equivalent

ORX_0(+/-)	ERX_0(+/-)	SELLVDS	VCC
ORX_1(+/-)	ERX_1(+/-)	SCL	GND
ORX_2(+/-)	ERX_2(+/-)	SDA	
ORX_3(+/-)	ERX_3(+/-)	WP	
OCLK(+/-)	ECLK(+/-)		
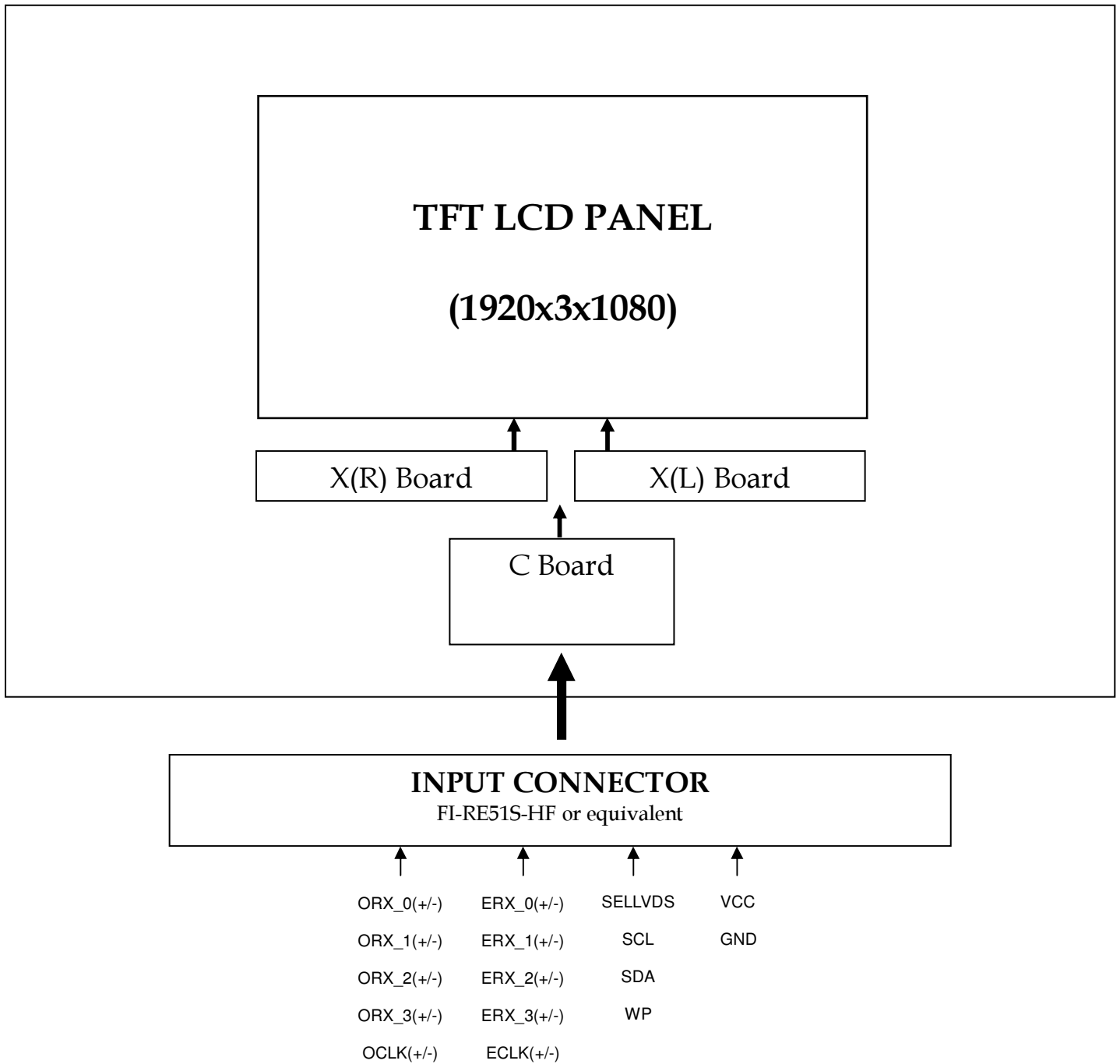
5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD OPEN CELL INPUT

CNF1 Connector Pin Assignment (FI-RE51S-HF or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	N.C.	No Connection	(2)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input	(5)
18	OCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(2)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input	(5)
33	ECLK+	Even pixel Positive LVDS differential clock input	
34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(2)
38	N.C.	No Connection	
39	GND	Ground	
40	SCL	EEPROM Serial Clock (for auto Vcom)	(2)
41	SDA	EEPROM Serial Data (for auto Vcom)	

42	N.C.	No Connection	
43	WP	EEPROM Write Protection (for auto Vcom) (0V~0.7V/Open→Disable, 2.7V~3.3V→Enable)	(2)
44	N.C.	No Connection	
45	SELLVDS	LVDS data format selection (2.7V~3.3V→JEIDA, 0V~0.7V/Open→VESA)	(3)(4)
46	N.C.	No Connection	
47	N.C.	No Connection	
48	N.C.	No Connection	(2)
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) LVDS connector pin order defined as follows
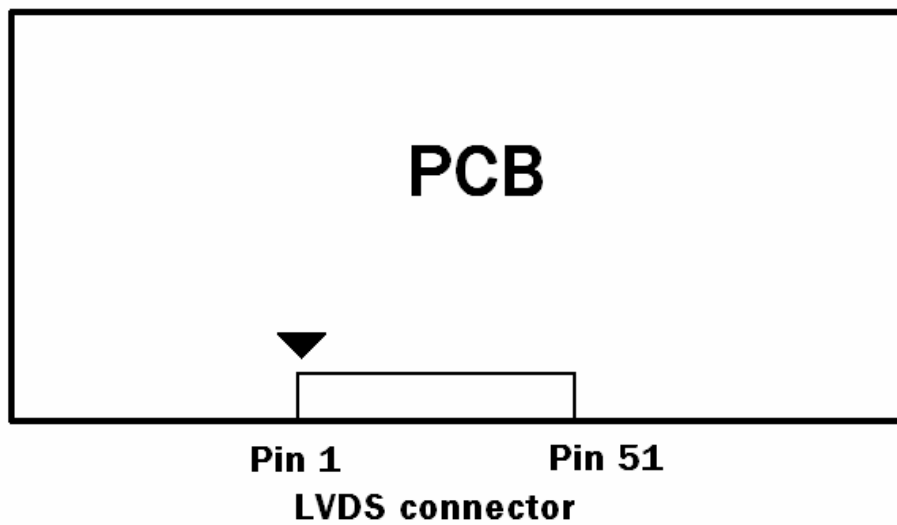
Note (2) Reserved for internal use. Please leave it open.

Note (3) Connect to +3.3V: JEIDA Format, Open or connect to GND: VESA Format.

SELLVDS	Mode
L(default)	VESA
H	JEIDA

L: Connect to GND, H: Connect to +3.3V

Note (4) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)

TCON

Selector (pin45) —— R1 —— R2 —— Setting

R3

System side

LCM side
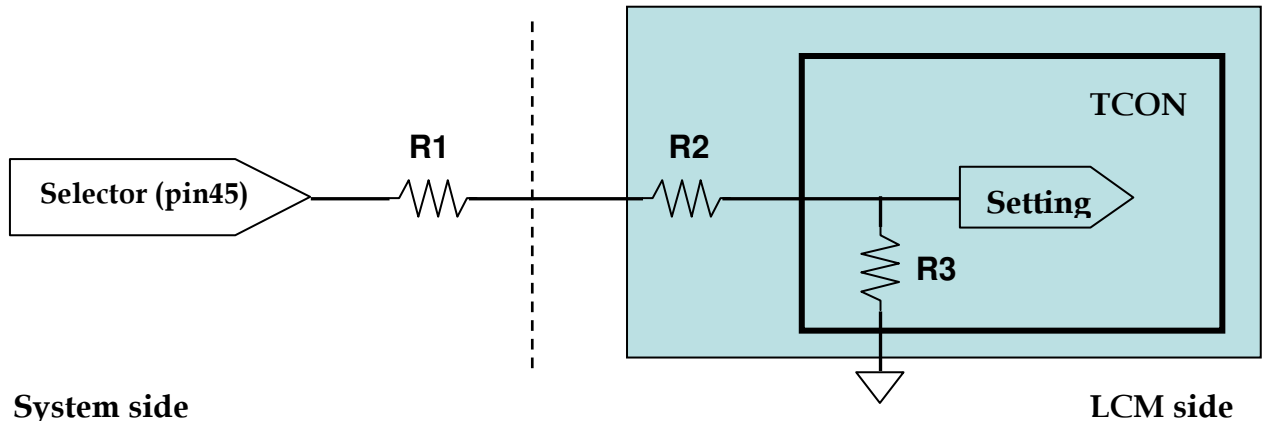
Note (5) LVDS connector mating dimension range request is 0.93mm~1.0mm as follow
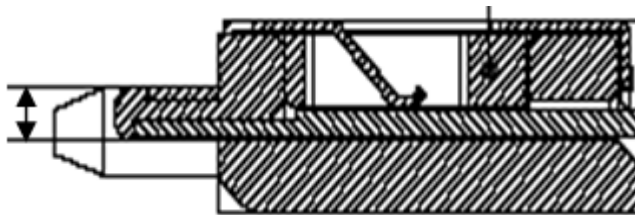
Note (6) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

FHD
1920 x 1080
CELL

XR

Connector

Connector

XL/XC

The screw hole which is distant from the connector is merged with Ground.
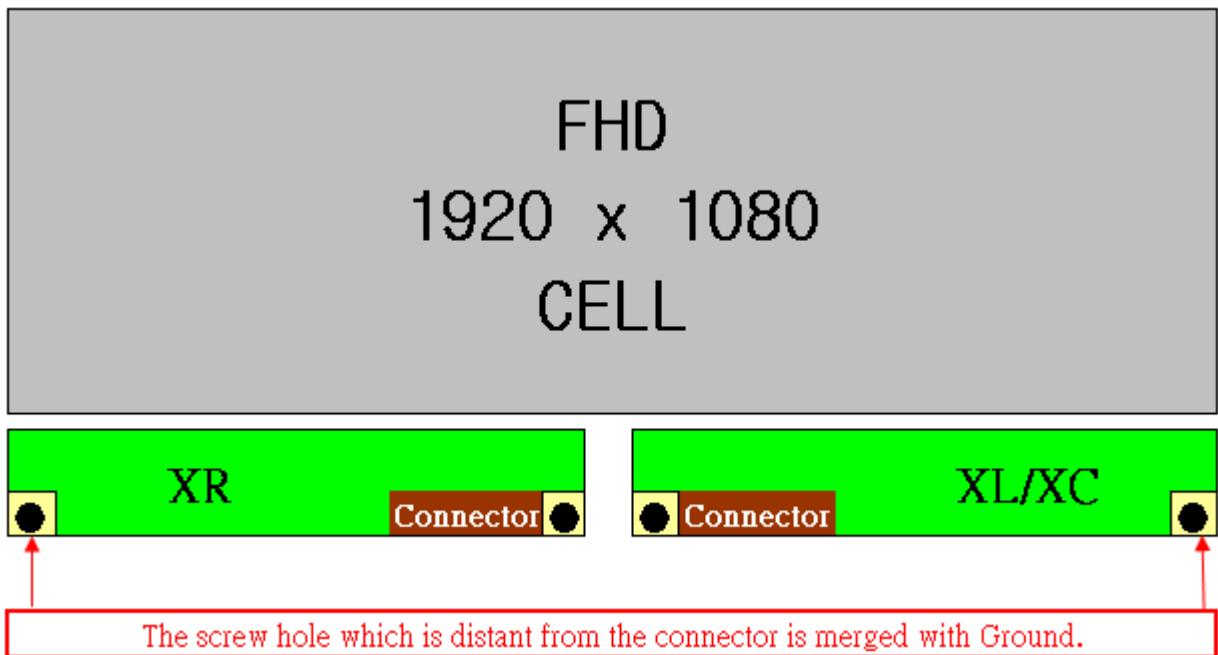
5.2 BLOCK DIAGRAM OF INTERFACE

CNF1

TxIN		RxOUT

ER0-ER7

EG0-EG7

EB0-EB7

DE

OR0-OR7

OG0-OG7

OB0-OB7

DCLK

Host
Graphics
Controller

ERx0+
ERx0-
ERx1+
ERx1-
ERx2+
ERx2-
ERx3+
ERx3-
ECLK+
ECLK-

100Ω 100pF
100Ω
100Ω 100pF
100Ω
100Ω 100pF
100Ω
100Ω 100pF
100Ω
100Ω 100pF
100Ω

PLL

ORx0+
ORx0-
ORx1+
ORx1-
ORx2+
ORx2-
ORx3+
ORx3-
OCLK+
OCLK-

100Ω 100pF
100Ω
100Ω 100pF
100Ω
100Ω 100pF
100Ω
100Ω 100pF
100Ω
100Ω 100pF
100Ω

PLL

ER0-ER7

EG0-EG7

EB0-EB7

DE

OR0-OR7

OG0-OG7

OB0-OB7

DCLK

Timing
Controller

LVDS Transmitter
THC63LVDM83A
(LVDF83A)

LVDS Receiver

5.3 LVDS INTERFACE

VESA LVDS format：(SELLVDS pin=L/Open)

Current cycle

RXCLK±

ORX0±	G0	R5	R4	R3	R2	R1	R0
ORX1±	B1	B0	G5	G4	G3	G2	G1
ORX2±	DE	VS	HS	B5	B4	B3	B2
ORX3±	RSVD	B7	B6	G7	G6	R7	R6
ERX0±	G0	R5	R4	R3	R2	R1	R0
ERX1±	B1	B0	G5	G4	G3	G2	G1
ERX2±	DE	VS	HS	B5	B4	B3	B2
ERX3±	RSVD	B7	B6	G7	G6	R7	R6

JEDIA LVDS format：(SELLVDS pin=H)

Current cycle

RXCLK±

ORX0±	G2	R7	R6	R5	R4	R3	R2
ORX1±	B3	B2	G7	G6	G5	G4	G3
ORX2±	DE	VS	HS	B7	B6	B5	B4
ORX3±	RSVD	B1	B0	G1	G0	R1	R0
ERX0±	G2	R7	R6	R5	R4	R3	R2
ERX1±	B3	B2	G7	G6	G5	G4	G3
ERX2±	DE	VS	HS	B7	B6	B5	B4
ERX3±	RSVD	B1	B0	G1	G0	R1	R0

R0~R7	Pixel R Data (7; MSB, 0; LSB)	DE	Data enable signal
G0~G7	Pixel G Data (7; MSB, 0; LSB)	DCLK	Data clock signal
B0~B7	Pixel B Data (7; MSB, 0; LSB)		

Note (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) /Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) /Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) /Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern:

The adjustment pattern is shown as below. If customer needs below pattern, please directly contact with CMI account FAE.

Frame N

Frame N+1
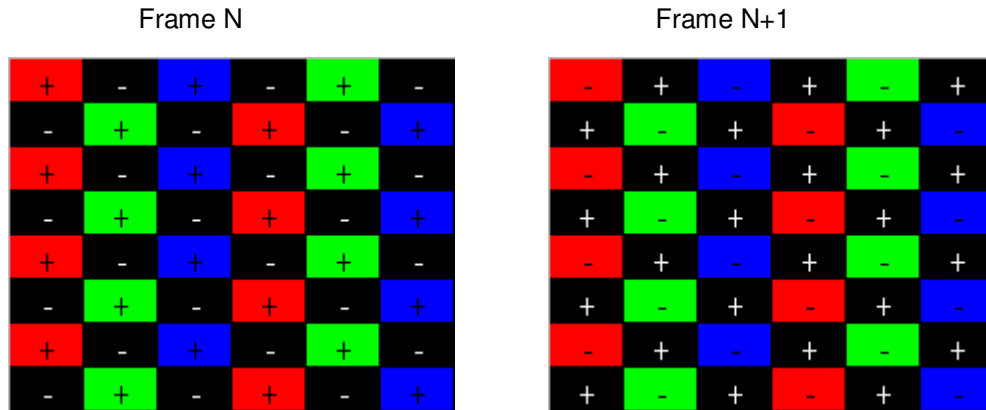
(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com.The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

a. USB Sensor Board.

b. Programmable software.

c. Document: Auto V-com adjustment suggestion OI.

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ℃)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	(1)(5)
	Input cycle to cycle jitter	T_{rcl}	─	─	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	─	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	─	─	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	─	─	ps	(5)
	Hold Time	Tlvhd	600	─	─	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(1)
		F_{r6}	57	60	63	Hz	
	Total	Tv	1090	1125	1480	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	(2)
	Blank	Tvb	10	45	400	Th	(2)
Horizontal Active Display Term	Total	Th	1030	1100	1325	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	(2)
	Blank	Thb	70	140	365	Tc	(2)

Note (1) Please make sure the range of pixel clock has follow the below equation：

$$F_{clkin(max)} \geq F_{r6} \times Tv \times Th$$

$$F_{r5} \times Tv \times Th \geq F_{clkin(min)}$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below：

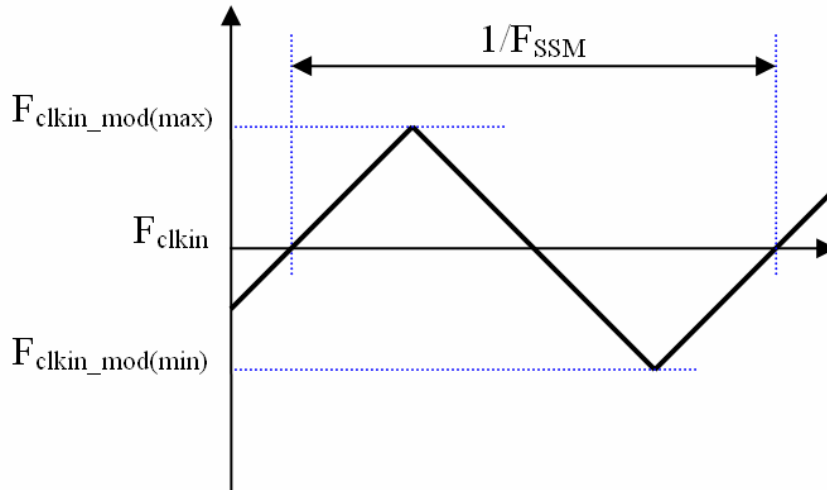## INPUT SIGNAL TIMING DIAGRAM
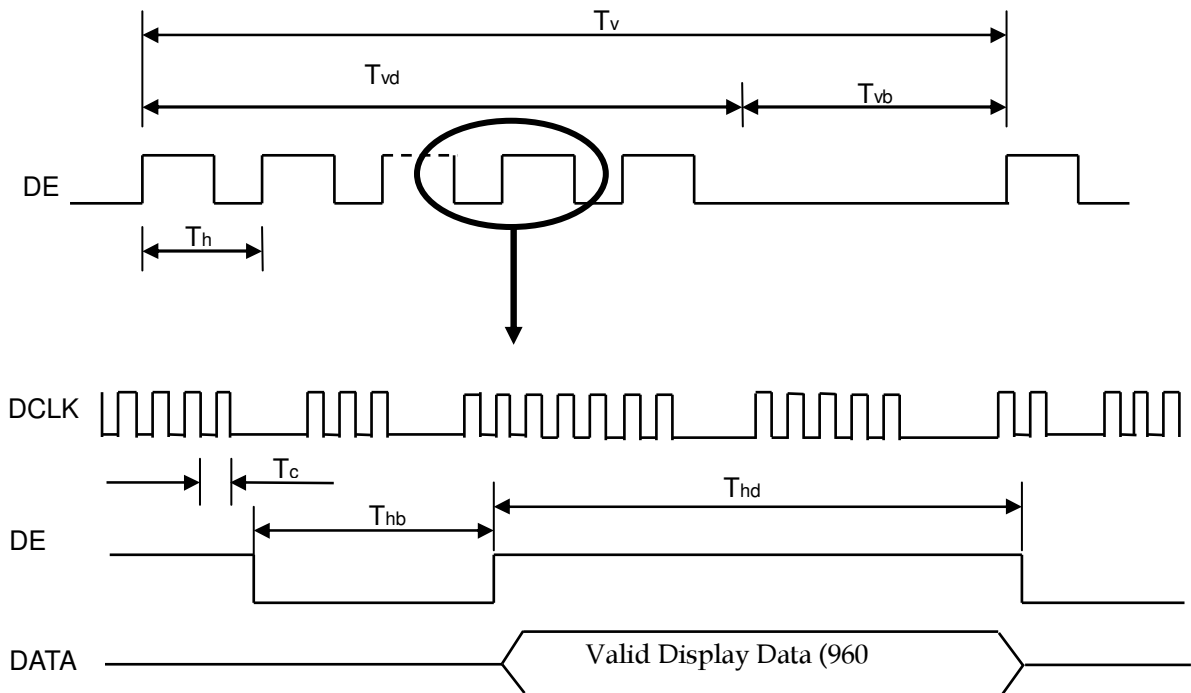
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = │ T$_1$ – T │
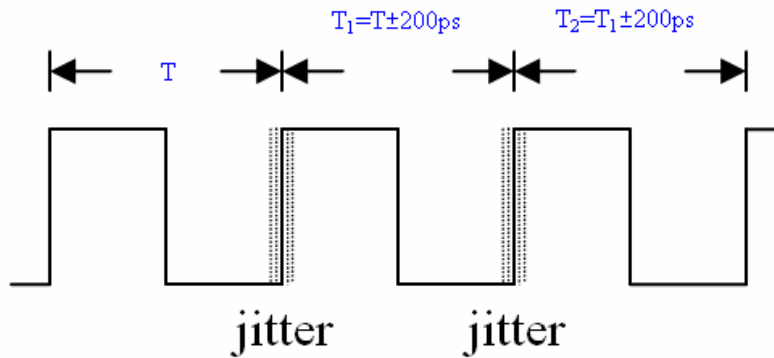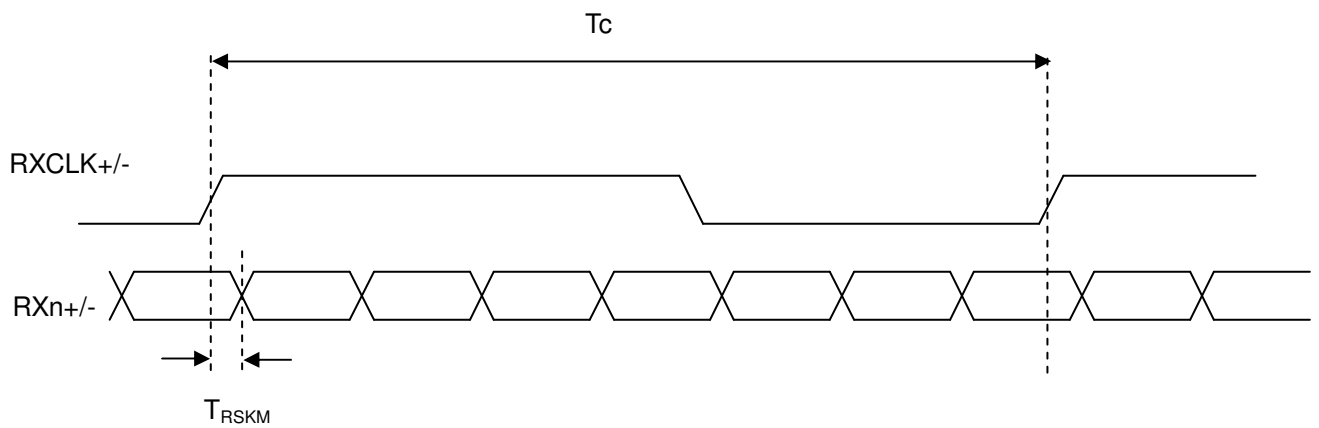

Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.

Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.
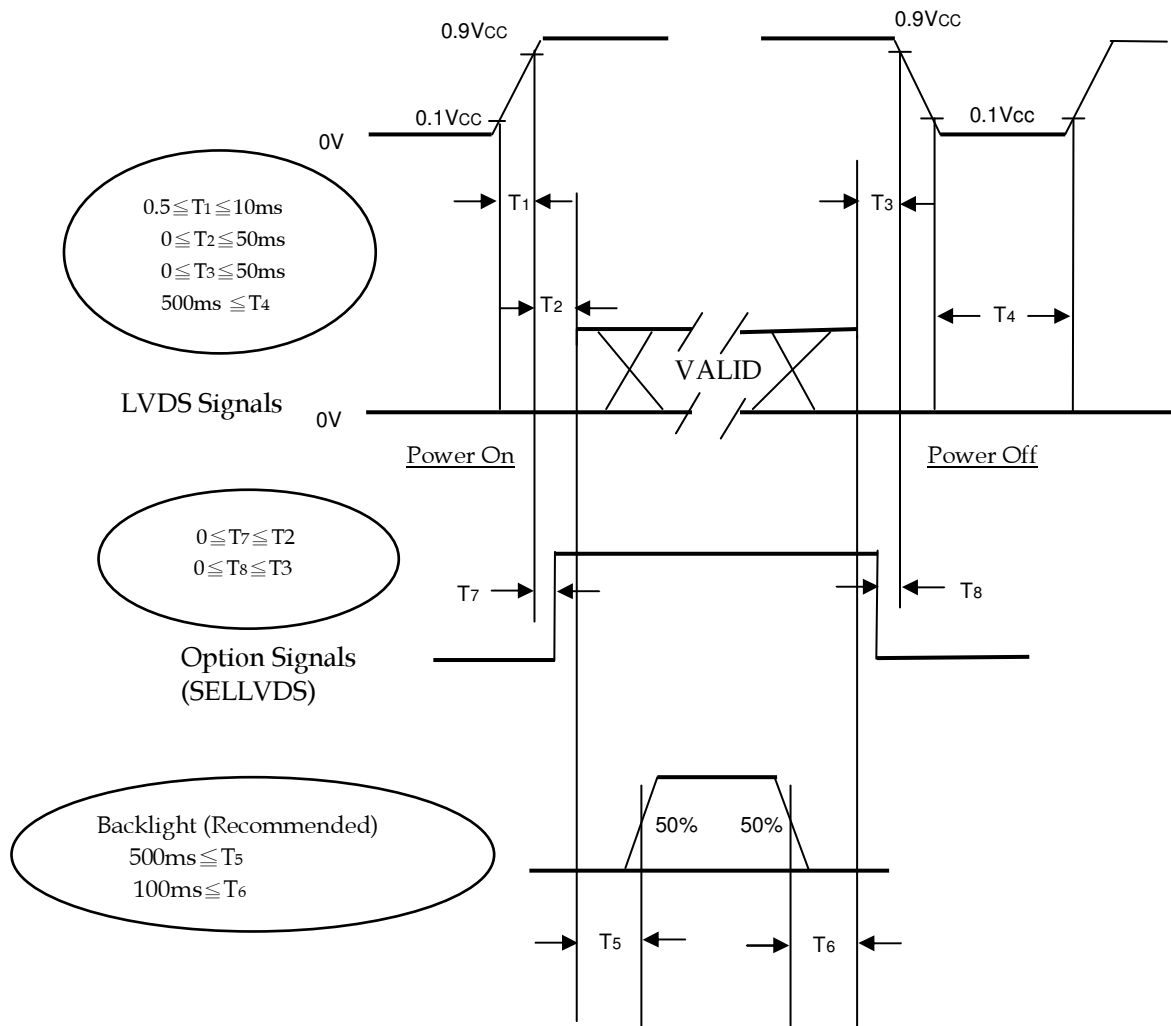
LVDS RECEIVER INTERFACE TIMING DIAGRAM

Note (6) : (ODSEL) = H/L or open for 60/60Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failures.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.
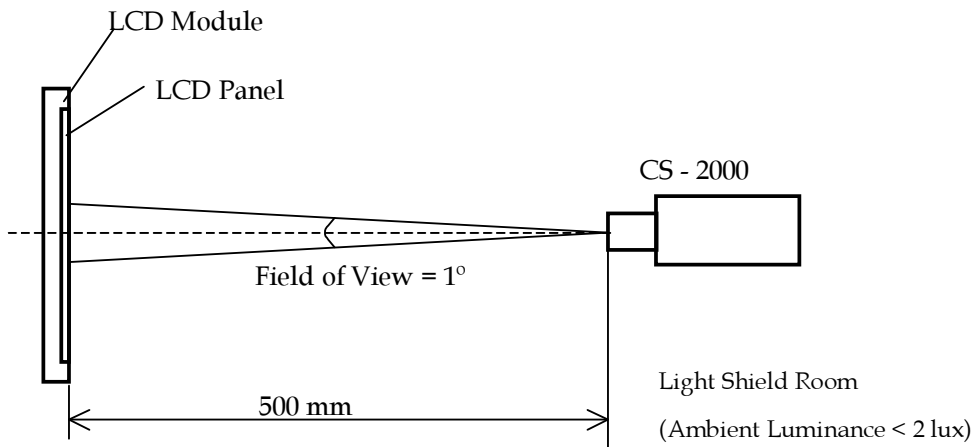
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.

LCD Module

LCD Panel

CS - 2000

Field of View = 1°

500 mm

Light Shield Room

(Ambient Luminance < 2 lux)

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 5.1 and stable environment shown in 5.1.

| Item			Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx		$\theta_x=0°$, $\theta_Y=0°$ Viewing Angle at Normal Direction Standard light source "C" With CMI Module & Tcon Board	-0.03	0.642	+0.03	-	(0)
		Rcy				0.331		-	
	Green	Gcx				0.290		-	
		Gcy				0.612		-	
	Blue	Bcx				0.149		-	
		Bcy				0.055		-	
	White	Wcx				0.280		-	
		Wcy				0.290		-	
Center Transmittance			T%	$\theta_x=0°$, $\theta_Y=0°$ With CMI Module & Tcon Board	-	TBD	-	%	(1),(5)
Contrast Ratio			CR		3500	5000	-	-	(1),(3)
Response Time			Gray to gray		-	9.0	18	ms	(1),(4)
Viewing Angle	Horizontal	θ_x+		CR≥20 With CMI Module & Tcon Board	-	88	-	Deg.	(1),(2)
		θ_x-			-	88	-		
	Vertical	θ_Y+			-	88	-		
		θ_Y-			-	88	-		

Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following :

1. Measure Module's W,R,G,B spectrum and BLU's spectrum. Which BLU is supplied by V400HJ2-LE2.

2. Calculate cell's spectrum.

3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80
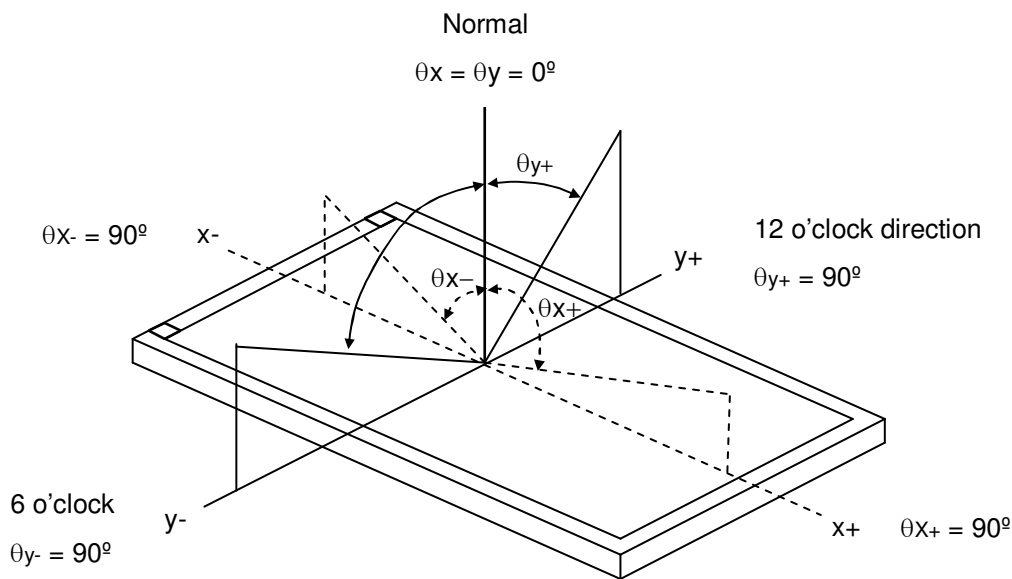
Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.
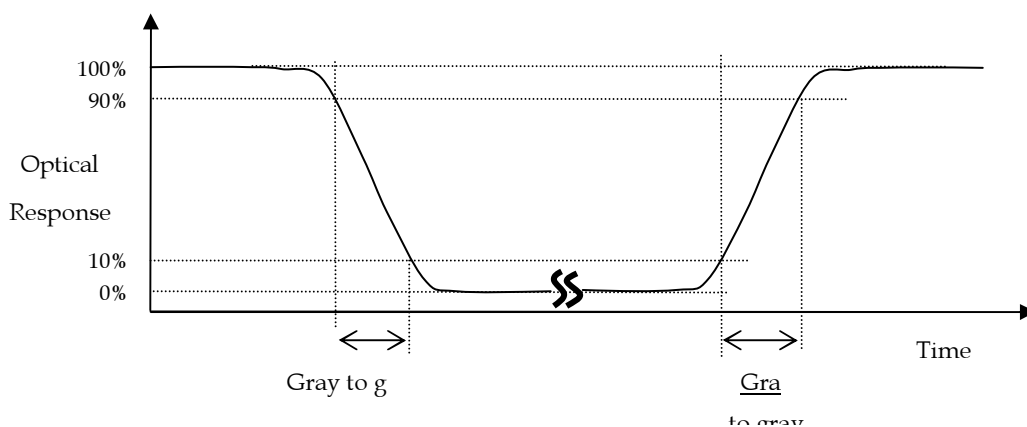
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Response Time (T_R, T_F, Gray to Gray) :

The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223, 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223, 255. to each other.

Note (5) Definition of Transmittance (T%) :

Measure the luminance of gray level 255 at center point of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\%$$

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] The distance between COF edge and rib of BLU is suggested to be larger than 5mm, in order to prevent from damage on COF during module assembly.

[6] Do not design sharp-pointed structure / parting line / tooling gate on the COF position of plastic parts, because the burr will scrape the COF.

[7] If COF would be bended during module assembly, it is suggested not to locate the IC on the bending corner of COF.

[8] The gap between COF IC and any structure of BLU is suggested to be larger than 2mm, in order to prevent from damage on COF IC.

[9] Bezel opening must have no burr. Burr will scrape the panel surface.

[10] It is suggested that bezel of module and bezel of TV set can not press or touch the panel surface. It will make light leakage or scrape.

[11] When module used FFC / FPC, but no FFC / FPC to be attached in the open cell. Customer can refer the FFC / FPC drawing and buy it by self.

[12] The gap between Panel and any structure of Bezel is suggested to be larger than 2mm, in order to prevent from damage on Panel.

[13] Do not plug in or pull out the I/F connector while the module is in operation.

[14] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[15] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[16] When storing modules as spares for a long time, the following precaution is necessary.

    [16.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

    [16.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[17] When ambient temperature is lower than 10ºC, the display quality might be reduced.

[18] The peeling strength of COF is 200gf/cm.

[19] During module assembly process, the static electricity around the environment should be less than 300V.

8.2 SAFETY PRECAUTIONS

[1]   If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[2]   After end of life of the open cell product, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 OPEN CELL LABEL

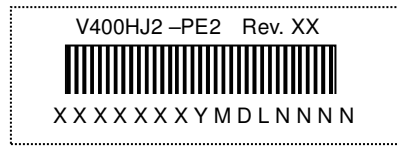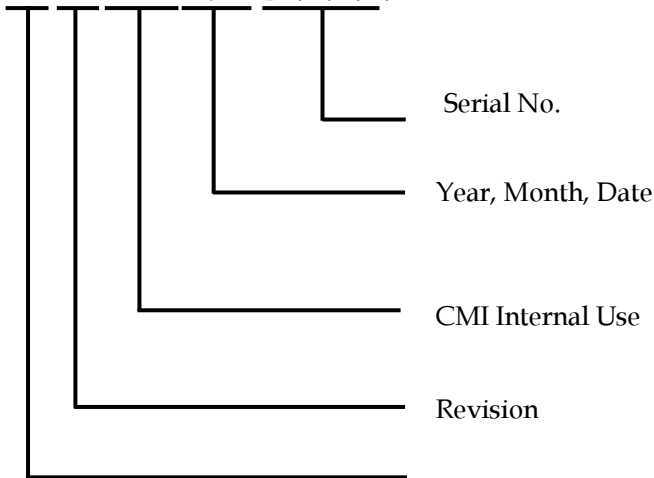The barcode nameplate is pasted on each open cell as illustration for CMI internal control.

```
V400HJ2 –PE2   Rev. XX
||||||||||||||||||||||||||||
X X X X X X X Y M D L N N N N
```

Figure.9-1 Serial No. Label on SPWB and Cell

Model Name: V400HJ2-PE2

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X X Y M D L N N N N

- Serial No.

- Year, Month, Date

- CMI Internal Use

- Revision

Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

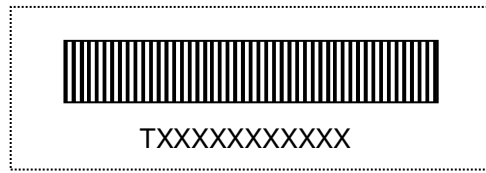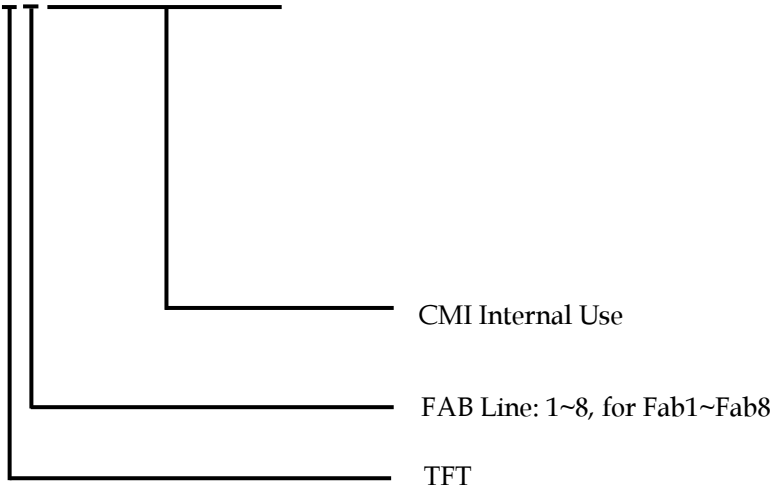Serial No.: Manufacturing sequence of product
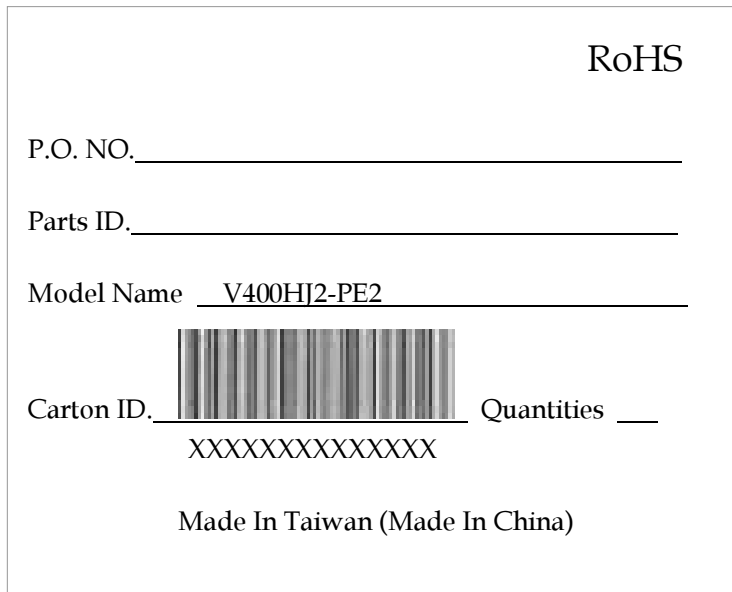
TXXXXXXXXXX

Figure.9-2 Panel ID Label on Cell

Panel ID Label includes the information as below :

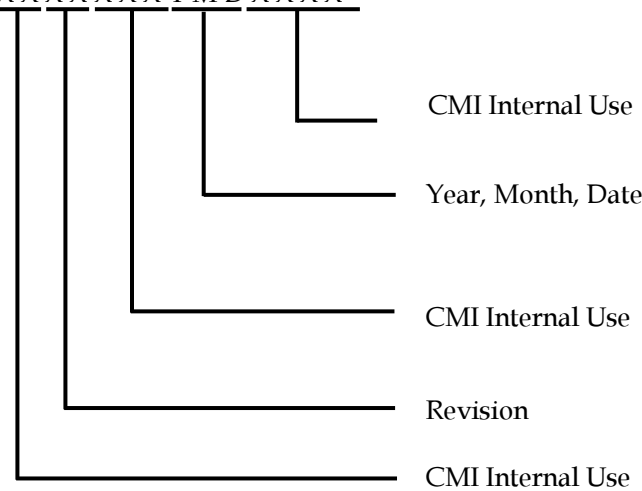Panel ID: T X X X X X X X X X X X

CMI Internal Use

FAB Line: 1~8, for Fab1~Fab8

TFT

9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

RoHS

P.O. NO.

Parts ID.

Model Name   V400HJ2-PE2

Carton ID.   Quantities

XXXXXXXXXXXXX

Made In Taiwan (Made In China)

(a) Model Name: V400HJ2– PE2

(b) Carton ID: X X X X X X X Y M D X X X X

CMI Internal Use

Year, Month, Date

CMI Internal Use

Revision

CMI Internal Use

Serial ID includes the information as below :

Manufactured Date:

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.
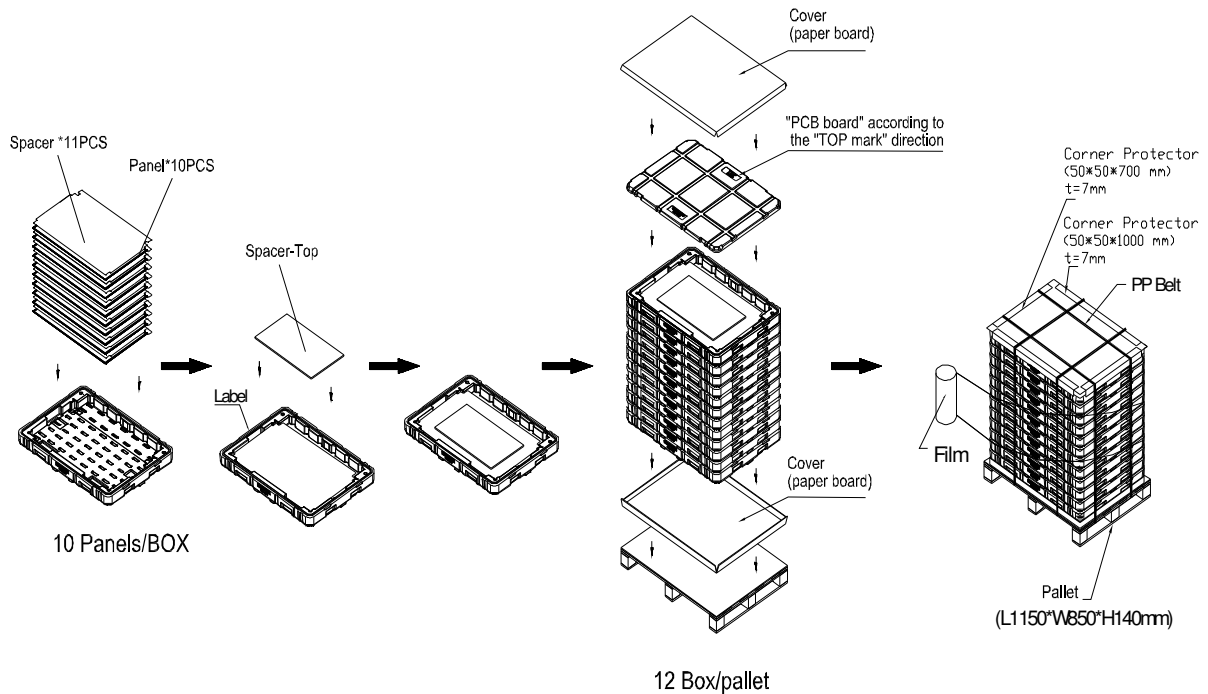
Revision Code: Cover all the change

(c) Quantities: 10

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS
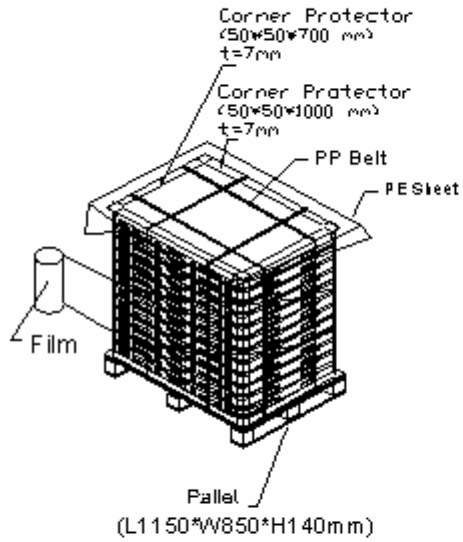
(1) 10 PCS LCD TV Panels / 1 Box

(2) Box dimensions :1110(L) X 810(W) X99(H)mm

(3) Weight : approximately 28Kg

(4) 120 PCS LCD TV Panels/1 Group

10.2 PACKAGING METHOD

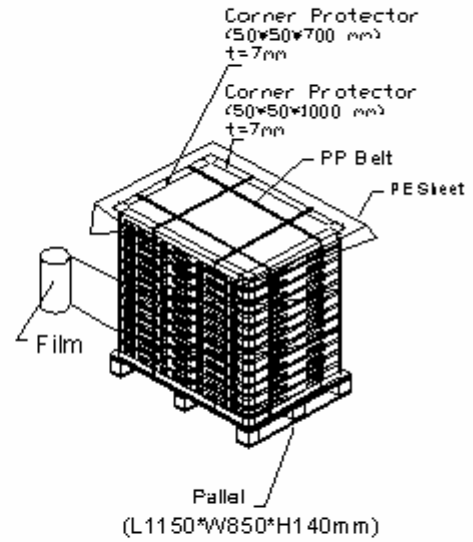Packing method is shown in following figures

Sea / Land Transportation

Corner Protector
(50*50*700 mm)
t=7mm

Corner Protector
(50*50*1000 mm)
t=7mm

PP Belt

PE Sheet

Film

Pallet
(L1150*W850*H140mm)

12 Box / Pallet

Air Transportation

Corner Protector
(50*50*700 mm)
t=7mm

Corner Protector
(50*50*1000 mm)
t=7mm

PP Belt

PE Sheet

Film

Pallet
(L1150*W850*H140mm)

12 Box / Pallet

11. MECHANICAL CHARACTERISTIC