

## TFT LCD Approval Specification

# MODEL NO.: V420B1 - L04

Customer: _____
Approved by: _____
Note:

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**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver.1.0	Apr.24,'07	All	All	Approval Specification was first issued.
Ver.1.1	Jun. 21, 07	29 37	7.2 12	Notes(2) drawing combine with Notes(6). Add ME parts assembly suggest drawing.
	Jun. 21, 07	36	11.2	Figure.11-2 Packing method amend.

## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

V420B1-L04 is a 42" TFT Liquid Crystal Display module with 20-CCFL Backlight unit and 1ch-LVDS interface.

This module supports 1366 x 768 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

### 1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (1500:1)
- Fast response time (Gray to gray average 6 ms)
- High color saturation (CIE1976 85% NTSC)
- HDTV (1366 x 768 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Auto frame rate detection for 60/50Hz
- Optimized response time for 60/50 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- 180 degree rotation display option
- RoHS compliance

### 1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.246(H) x 523.008 (V) (42.02" diagonal)	mm	(1)
Bezel Opening Area	938.3 (H) x 531.3 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch(Sub Pixel)	0.227 (H) x 0.681 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating, Hard coating (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

**1.5 MECHANICAL SPECIFICATIONS**

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	982.0	983.0	984.0	mm	(1), (2)
	Vertical (V)	575.0	576.0	577.0	mm	
	Depth (D)	51.3	52.3	53.3	mm	
Weight		12800	12900	13000	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

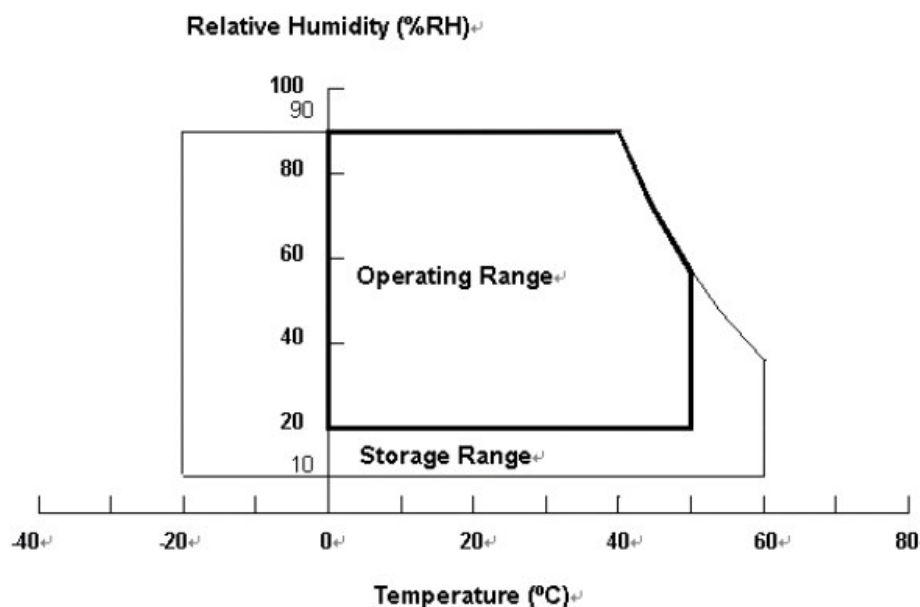
- (a) 90 %RH Max. ( $T_a \leq 40$  °C).
- (b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40$  °C).
- (c) No condensation.
- (d) 40 °C 95% RH is for reference

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for  $\pm X$ ,  $\pm Y$ ,  $\pm Z$ .

Note (4) 10 ~ 500 Hz, 60 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



**2.2 ELECTRICAL ABSOLUTE RATINGS****2.2.1 TFT LCD MODULE**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	6.0	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

**2.2.2 BACKLIGHT INVERTER UNIT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	VW	—	3000	VRMS	
Power Supply Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control, Internal/External PWM Control, Amplitude Dimming Control and Internal/External PWM Selection.



### 2.3 ENVIRONMENT TEST CONDITION

No	Test Item	Codition
1	High temperature storage test	Ta = 60°C, 500hrs
2	Low temperature storage test	Ta = -25°C, 500hrs
3	High temperature high humidity storage test	Ta = 50°C, 90%RH 500hrs (40°C 95%RH 500hrs judge for reference)
4	High temperature operation test	Ta= 50°C, 500hrs
5	Low temperature operation test	Ta=0°C, 500hrs
6	High temperature high humidity operation test	Ta= 40°C, 95%RH 500hrs
7	Thermal shock	Ta= -25°C/ 60min ~ 60°C/ 60min, 100cycles
8	Vibration test (non-operation)	Wave form: Sine wave Vibration level: 1.0G Fre. range : 10~500Hz Duration: X, Y, Z, 60min, One time each direction
9	Shock test (non-operation)	Wave form: half sine wave, 11ms Shock level: 50G ±X, ±Y, ± Z, One time each direction
10	ESD	Storage: Contact mode +/-20kV, Air mode +/-20kV Operation: Contact mode +/-20kV, Air mode +/-20kV Condition: 150pF, 330ohm
11	Package vibration	Wave form: Sine wave Vibration level: 1.0G Fre. range : 5~50Hz Duration: 15min for X, Y, 60 min for Z. One time each direction
12	Package drop	Drop 1 corner, 3 sides, 6 faces, each one for 1 time. Height is 30cm. (Test environment: 25°C)

### 3. ELECTRICAL CHARACTERISTICS

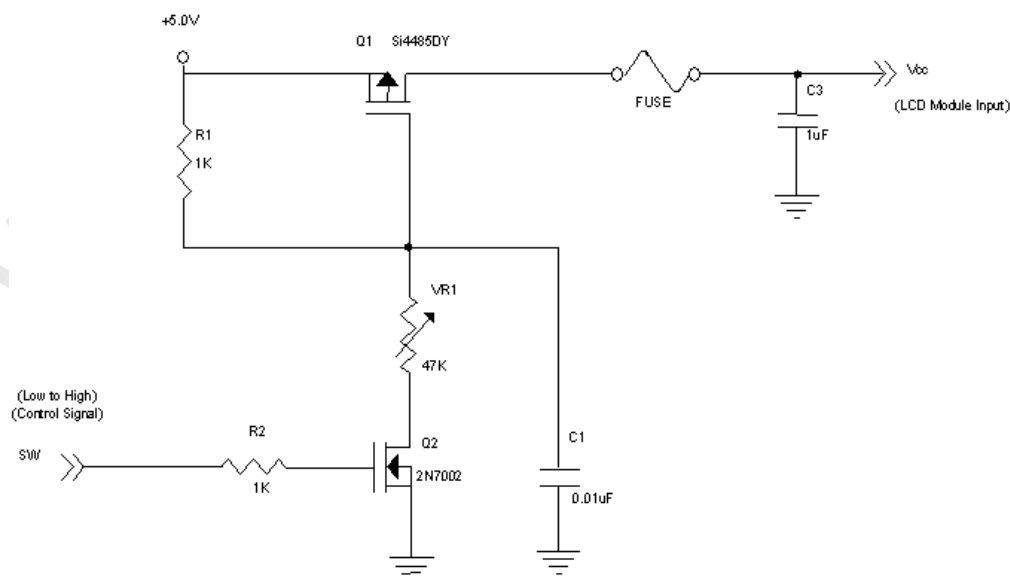
#### 3.1 TFT LCD MODULE

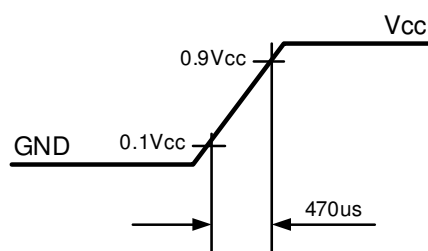
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCC	4.5	5	5.5	V	(1)
Power Supply Ripple Voltage		VRP	-	-	350	mV	
Rush Current		IRUSH	-	-	4.5	A	(2)
Power Supply Current	White	-	-	1.48	2.1	A	(3)
	Black	-	-	0.77	-	A	
	Vertical Stripe	-	-	1.47	-	A	
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	-	-	100	mV	
	Differential Input Low Threshold Voltage	VLVTL	-100	-	-	mV	
	Common Input Voltage	VLVC	1.1	1.25	1.4	V	
	Terminating Resistor	RT	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	VIH	2.4	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



**Vcc rising time is 470us**

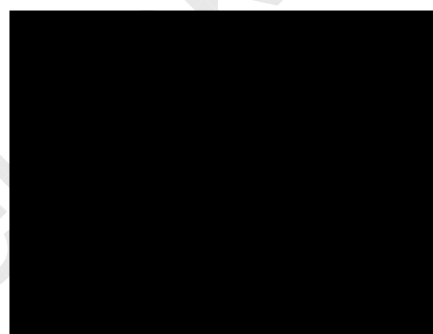
Note (3) The specified power supply current is under the conditions at  $V_{cc} = 5\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^\circ\text{C}$ ,  $f_v = 60\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



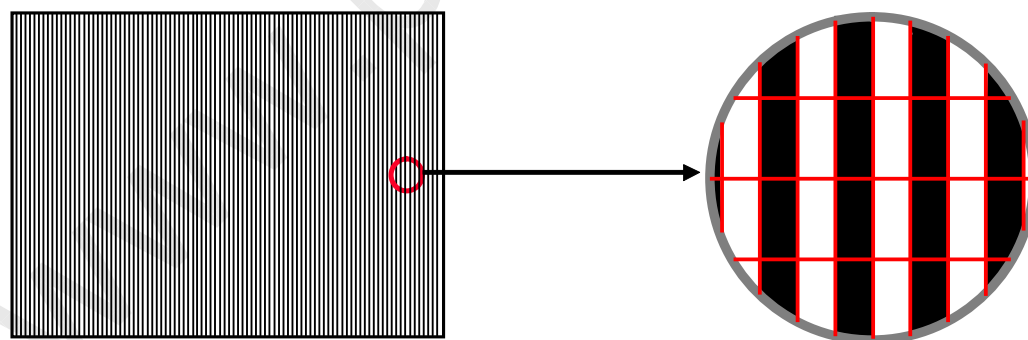
Active Area

b. Black Pattern



Active Area

c. Vertical Stripe Pattern



Active Area

### 3.2 BACKLIGHT UNIT

#### 3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	VL	-	1520	-	VRMS	-
Lamp Current	IL	5.3	5.8	6.3	mARMS	(1)
Lamp Turn On Voltage	VS	-	-	2370	VRMS	Ta = 0 °C
		-	-	2160	VRMS	Ta = 25 °C
Operating Frequency	FL	40	-	70	KHz	
Lamp Life Time	LBL	50,000	60,000	-	Hrs	(2)

#### 3.2.2 INVERTER CHARACTERISTICS

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P <sub>BL</sub>	-	170	180	W	(5), IL = 5.8mA
Power Supply Voltage	VBL	22.8	24.0	26.4	VDC	
Power Supply Current	IBL	-	7.1	7.5	A	Non Dimming
Input Inrush Current	-	-	-	11	Apeak	
Input Ripple Noise	-	-	-	912	mVP-P	VBL=22.8V
Oscillating Frequency	FW	47	50	53	kHz	
Dimming frequency	FB	150	160	170	Hz	
Minimum Duty Ratio	DMIN	-	25	-	%	

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

Note (2) The lamp starting voltage VS should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

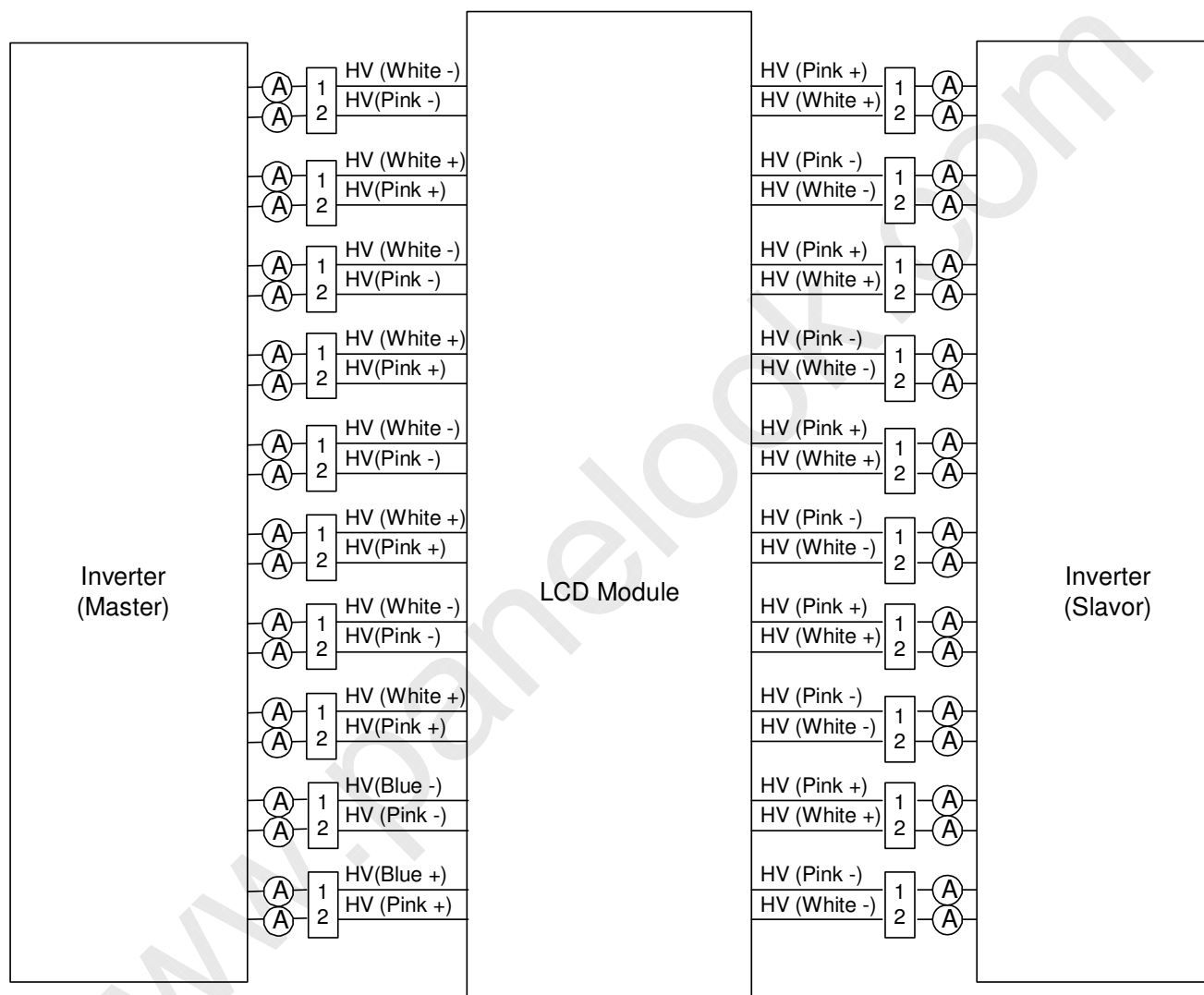
Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ± 2°C and IL = 6.0~

7.0mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6)



## 3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter	Symbol	Test Condition	Value			Unit	Note	
			Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	3.3	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	VSEL	—	3.0	3.3	3.6	V	Open/High (3.3V): Internal PWM dimming.
	LO		—	0	—	0.8	V	GND: External PWM dimming
Internal PWM Control Voltage	MAX	VPDIM	VSEL = H	—	3.3	—	V	Max. Duty Ratio
	MIN		VSEL = H	—	0	—	V	Min. Duty Ratio
External PWM Control Voltage	HI		VSEL = L	3.0	3.3	3.6	V	ON Duration
	LO		VSEL = L	0	—	0.8	V	OFF Duration
Amplitude dimming	Max	VADIM	—	—	3.3	—	V	110% Luminance
	Typ		—	—	1.6	—	V	Open/1.6V: 100% Luminance
	Min		—	—	0	—	V	80% Luminance
Control Signal Rising Time	Tr	—	—	—	100	ms		
Control Signal Falling Time	Tf	—	—	—	100	ms		
VBL Rising Time	Tr1	—	30	—	50	ms		
VBL Falling Time	Tf1	—	30	—	50	ms		
PWM Delay Time	TPWM	—	100	—	300	ms		
Input impedance	RIN	—	1	—	—	MΩ		
BLON Delay Time	Ton	—	300	—	500	ms		
BLON Off Time	Toff	—	300	—	500	ms		

Note (1) The power sequence and control signal timing are shown in the following figure.

Note (2) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) VADIM (amplitude dimming) is control signal for Inverter's output power to backlight lamp bulb. Input signal should be able to control amplitude of Inverter output voltage. From 0V to 3.3V, Inverter output voltage should be able to vary to control brightness of lamp from 80% to 110% luminance variation. Approximate 1.6V might be 100% luminance control point.

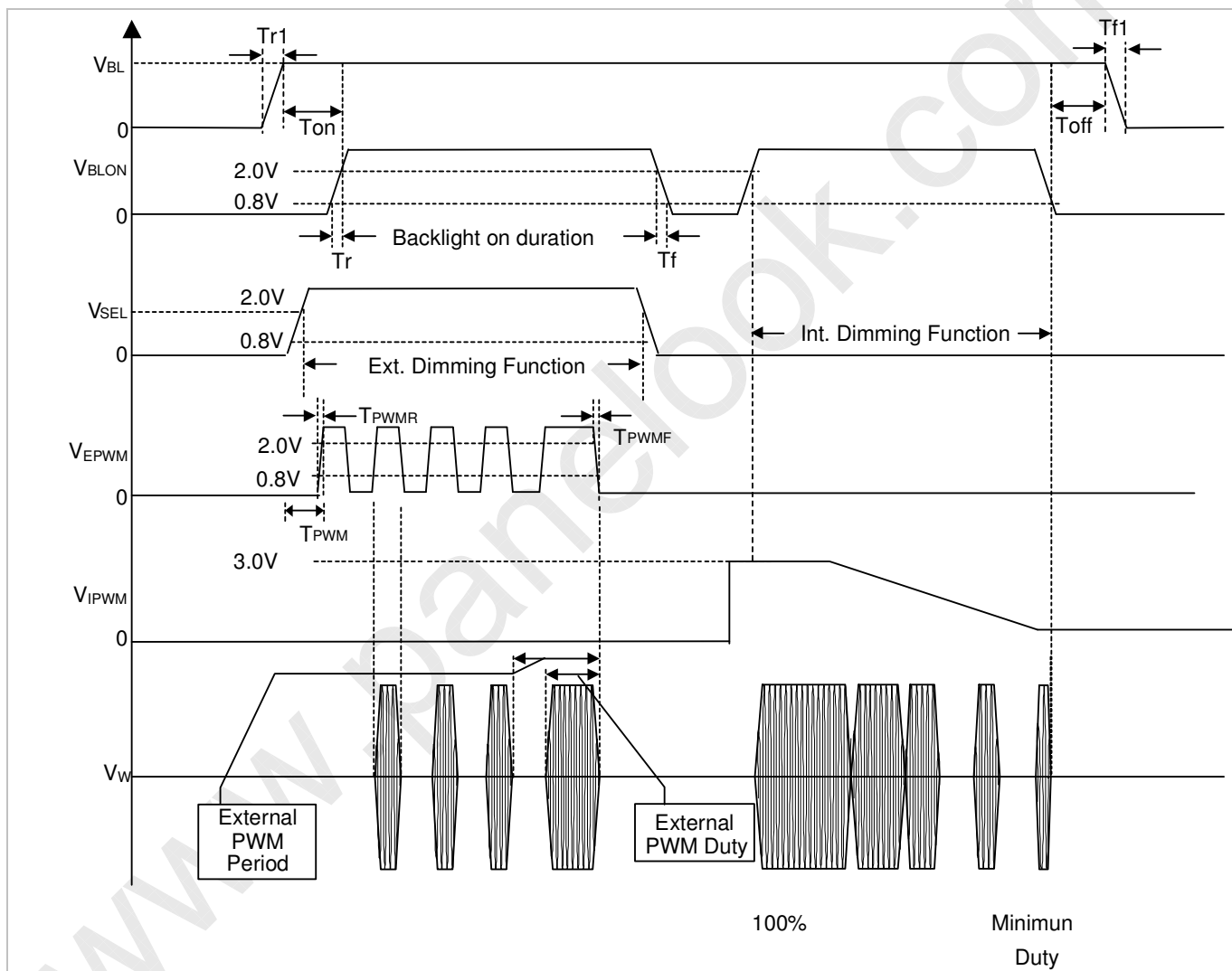
Note (4) VPDIM is PWM duty control input for +3.3V TTL level signal or DC voltage by Pin 14 input. This input signal is (a) continuous pulse signal with +3.3V, TTL level signal spec, or (b) DC power with 0~3.3V. If this is Open or +3.3V, 100% duty (i.e. +3.3V, DC level), backlight should perform 100% luminance. Duty ratio of this input signal should be proportional relationship in certain range of control without any kind of inherent side effect like waterfall effect on screen. Guaranteed duty range and dimming ratio should be specified with supplementary measurement result.

Note (5) Pin 14 is the selection pin for PWM control method; if this pin is connected to GND, VPDIM input of Pin 13 should have logic level duty signal for PWM control. If this is set to High or Open, Pin 13 should have DC level signal therefore the Inverter should have Saw Tooth Wave Generator to generate internal PWM

signal. Default setting is "Not Connected", Pin 13 of PWM control should have DC Level signal for PWM.

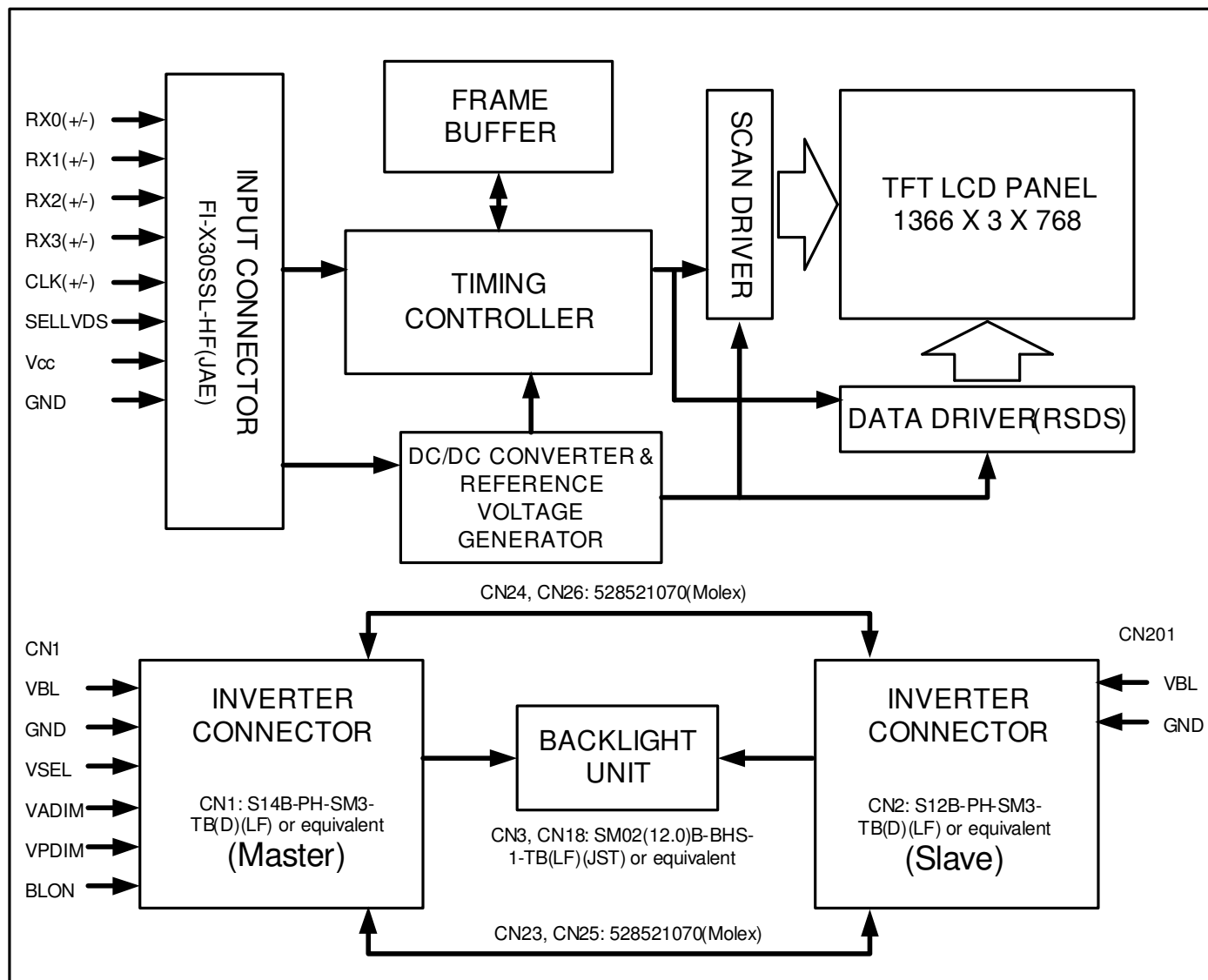
Note (6) Pin 14 vs. Pin 11/13 control function table:

	Pin 11 (DC Power Control Duty Amplitude) Function Always Turn On Default: Open/1.6V: 100%	Pin 13 Default: Open/High: 100%
Pin 14 = GND	GND: 80%; Open/1.6V: 100%;	External PWM (AC Signal Control Duty)
Pin 14 = Open/High	High (3.3V) 110%, Luminance	Internal PWM (DC Power Control Duty)



## 4. BLOCK DIAGRAM OF INTERFACE

### 4.1 TFT LCD MODULE





## 5. INPUT TERMINAL PIN ASSIGNMENT

### 5.1 TFT LCD Module Input

Pin	Name	Description	Note
1	VCC	+5V power supply	
2	VCC	+5V power supply	
3	VCC	+5V power supply	
4	VCC	+5V power supply	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground or Open	
9	SELLVDS	LVDS data format Selection	(2)
10	GND	Ground	
11	GND	Ground	
12	RX0-	Pixel Negative LVDS differential data input. Channel 0	
13	RX0+	Pixel Positive LVDS differential data input. Channel 0	
14	GND	Ground	
15	RX1-	Pixel Negative LVDS differential data input. Channel 1	
16	RX1+	Pixel Positive LVDS differential data input. Channel 1	
17	GND	Ground	
18	RX2-	Pixel Negative LVDS differential data input. Channel 2	
19	RX2+	Pixel Positive LVDS differential data input. Channel 2	
20	GND	Ground	
21	CLK-	Pixel Negative LVDS differential clock input.	
22	CLK+	Pixel Positive LVDS differential clock input.	
23	GND	Ground	
24	RX3-	Pixel Negative LVDS differential data input. Channel 3	
25	RX3+	Pixel Positive LVDS differential data input. Channel 3	
26	GND	Ground	
27	N.C.	Ground or Open	(3)
28	N.C.	Ground or Open	(3)
29	GND	Ground or Open	
30	GND	Ground or Open	

Note (1) Connector part No: FI-X30SSL-HF (JAE).

Note (2) Low : VESA LVDS Format, High or open : JEIDA LVDS Format (default).

Note (3) Reserved for internal use. We strongly suggest it open.

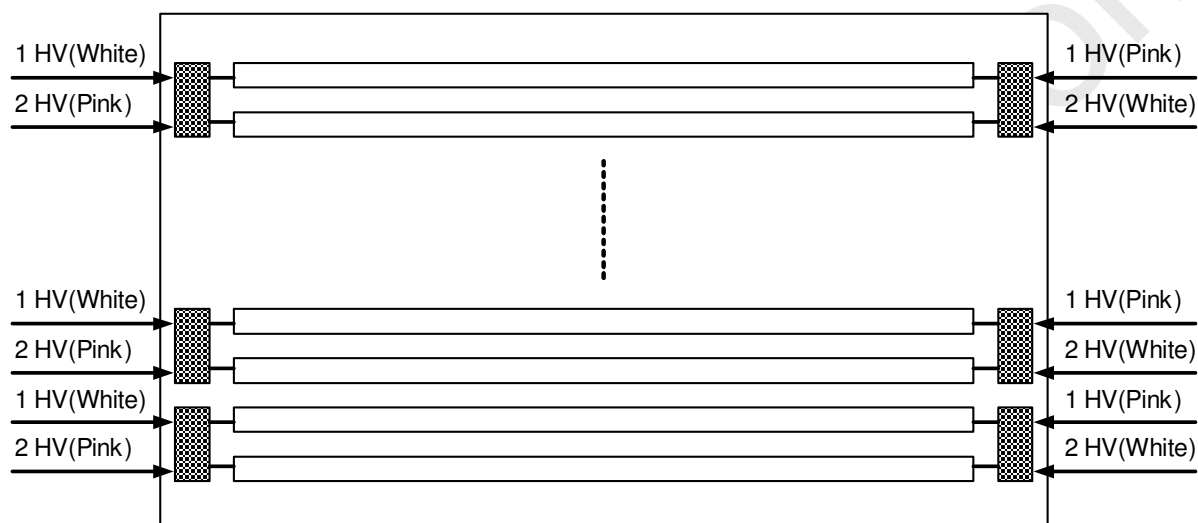
## 5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN3-CN22: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST. The mating header on inverter part number is SM02(12.0)B-BHS-1-TB(LF).



**5.3 INVERTER UNIT**

CN1: S14B-PH-SM3-TB(D)(LF)(JST) or equivalent

Pin No	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	VADIM	GND: 80% Luminance; Open/1.6V: 100% Luminance; High (3.3V) 110% Luminance,
12	BLON	BL ON/OFF
13	VPDIM	Open/High (+3.3V, 100% Duty) for 100% Luminance.
14	VSEL	GND: External PWM dimming; Open/High (3.3V): Internal PWM dimming.

CN201: S12B-PH-SM3-TB(D)(LF)(JST) or equivalent

Pin No	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN3-CN22: SM02(12.0)B-BHS-1-TB(LF)(JST) or equivalent

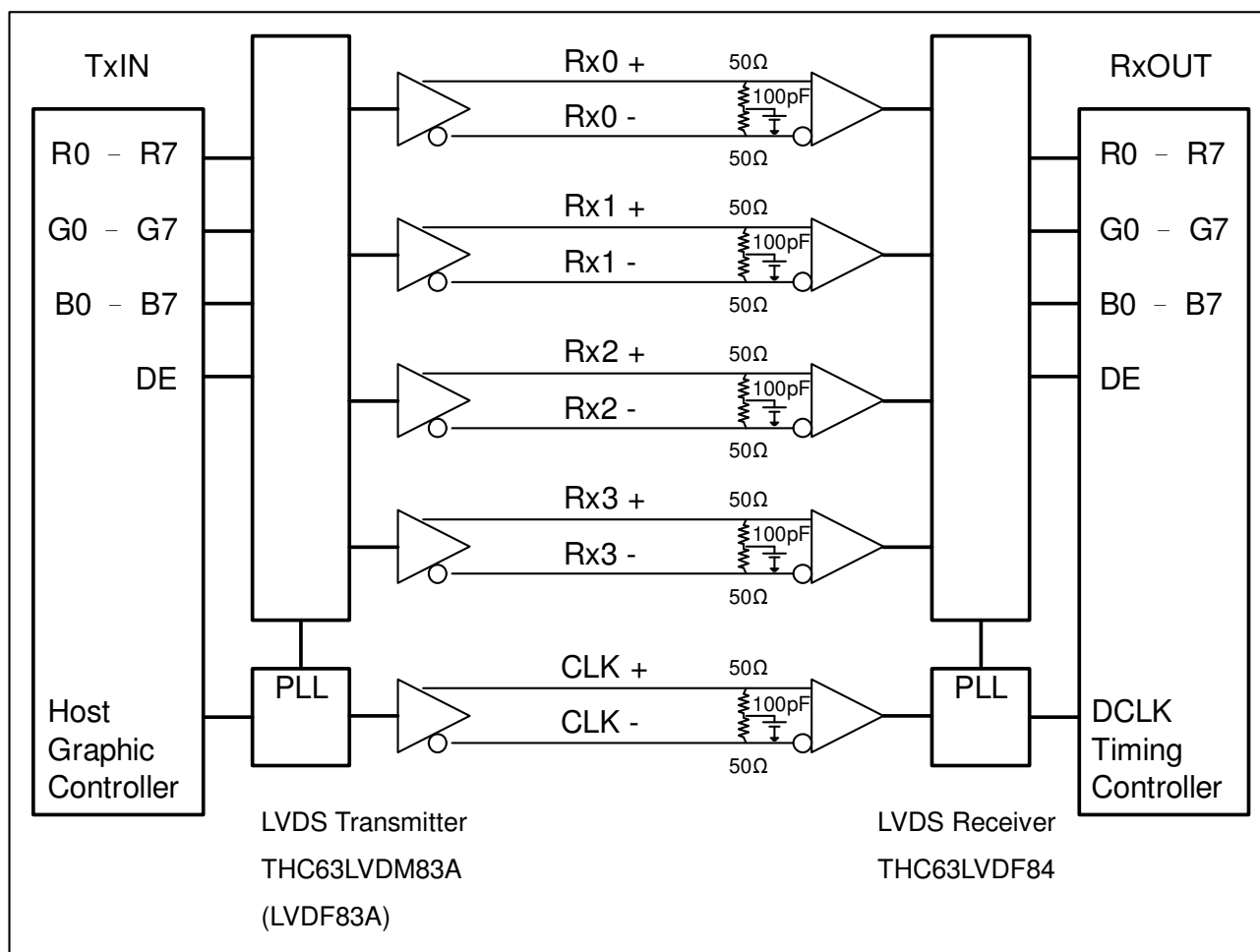
Pin No	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN23-CN26: 528521070 (Molex)

Pin No	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board

Note (1) Floating of any control signal is not allowed.

## 5.4 BLOCK DIAGRAM OF INTERFACE



R0~R7: Pixel R data

G0~G7: Pixel G data

B0~B7: Pixel B data

DE: Data enable signal

DCLK: Data clock signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

## 5.5 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83 A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	LVDS_SEL =L or OPEN	LVDS_SEL = H	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	LVDS_SEL =L or OPEN	LVDS_SEL = H
24 bit	R0	R2	51	TxIN0	TA OUT0+	Rx 0+	27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2			30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4	TA OUT0-	Rx 0-	33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6			35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9	TA OUT1+	Rx 1+	39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12			43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27			TA OUT2-	Rx 2-	7	Rx OUT27
	R7	R1	2	TxIN5	34	Rx OUT5			R7	R1
	G6	G0	8	TxIN10	41	Rx OUT10			G6	G0
	G7	G1	10	TxIN11	42	Rx OUT11			G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
RSVD 1	RSVD 1	25	TxIN23	2			Rx OUT23	NC	NC	
RSVD 2	RSVD 2	27	TxIN24	TA OUT3-			Rx 3-	3	Rx OUT24	NC
RSVD 3	RSVD 3	28	TxIN25		5	Rx OUT25		NC	NC	
DCLK			31	TxCLK IN	TxCLK OUT+	RxCLK IN+	26	RxCLK OUT	DCLK	
					TxCLK OUT-	RxCLK IN-				

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".



**5.6 COLOR DATA INPUT ASSIGNMENT**

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red Gray Scale	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green Gray Scale	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green (253)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	
	Green (254)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Green (255)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0		
Blue Gray Scale	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 6. INTERFACE TIMING

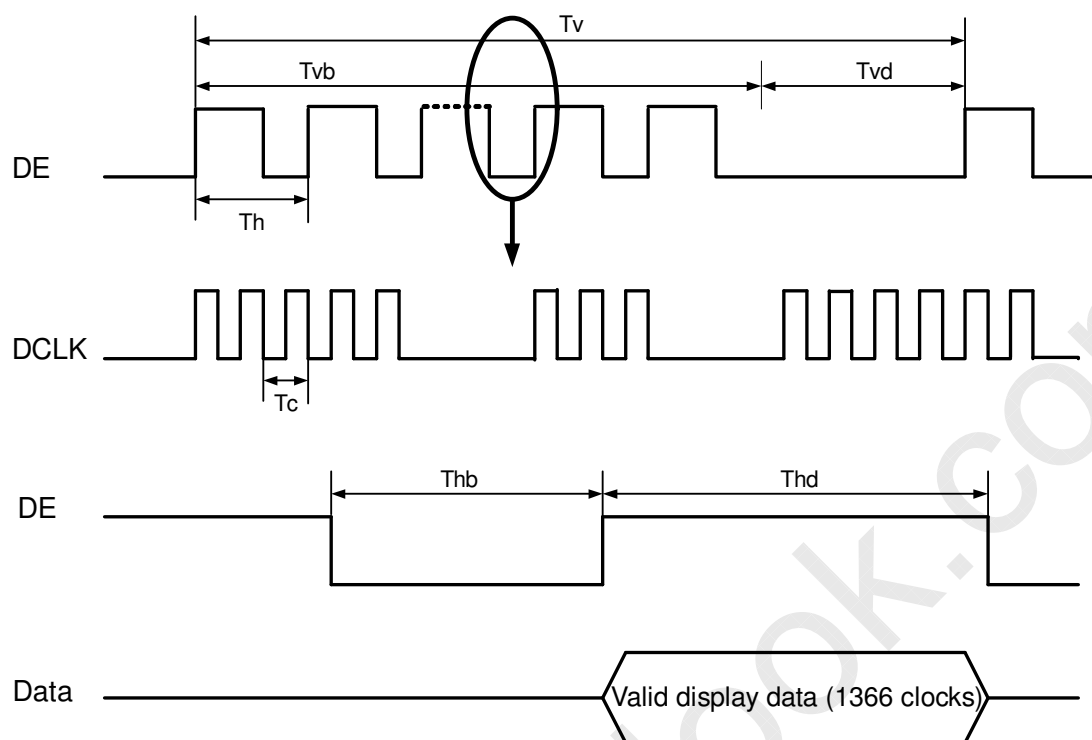
### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

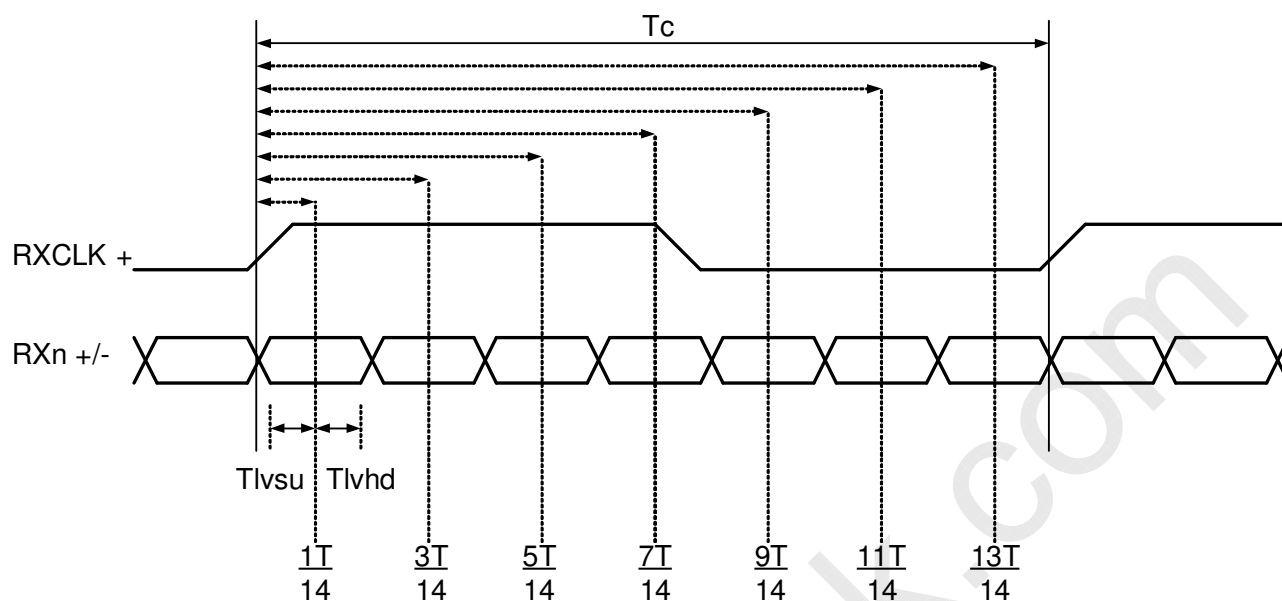
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	86	88	MHZ	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	400	-	-	ps	-
	Hold Time	Tlvhd	400	-	-	ps	-
Vertical Active Display Term	Frame Rate		57	60	63	Hz	
			47	50	53	Hz	
	Total	Tv	778	795	980	Th	Tv=Tvd+Tvb
	Display	Tvd	768	768	768	Th	-
	Blank	Tvb	10	27	212	Th	-
Horizontal Active Display Term	Total	Th	1442	1798	1936	Tc	Th=Thd+Thb
	Display	Thd	1366	1366	1366	Tc	-
	Blank	Thb	76	432	570	Tc	-

Note : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.



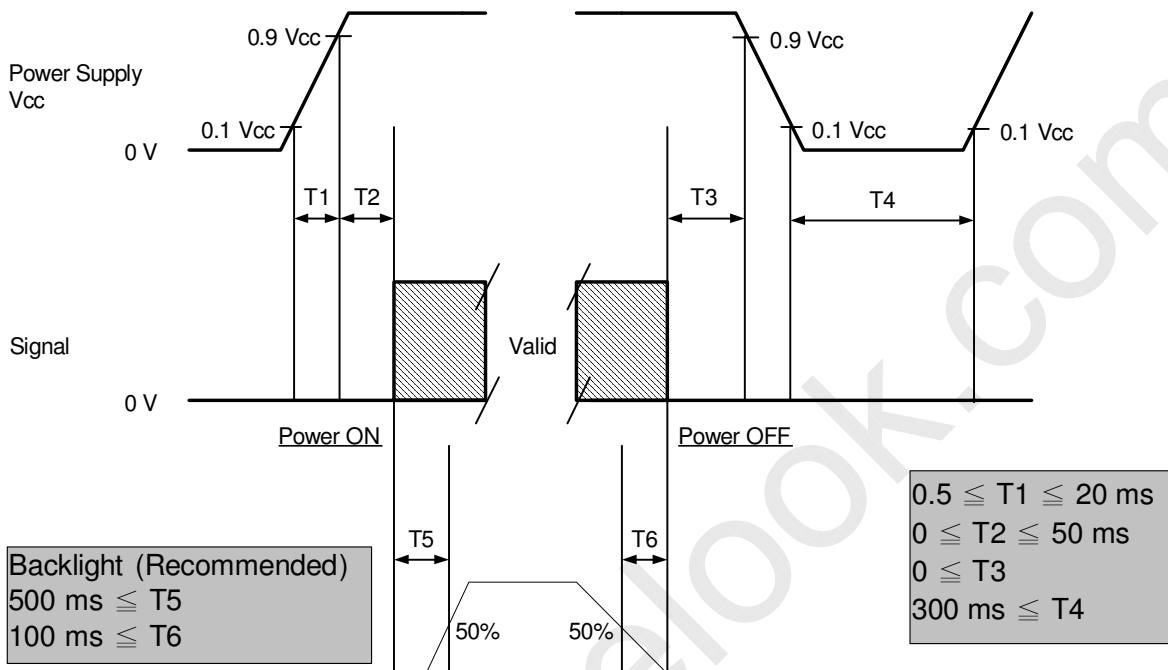
**INPUT SIGNAL TIMING DIAGRAM**

**LVDS INPUT INTERFACE TIMING DIAGRAM**

## 6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.

### POWER ON/OFF SEQUENCE



Note.

The supply voltage of the external system for the module input should follow the definition of Vcc.

Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

T4 should be measured after the module has been fully discharged between power off and on period.

Interface signal shall not be kept at high impedance when the power is on.

## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	5	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	5.8±0.5	mA
Oscillating Frequency (Inverter)	FW	50±3	KHz
Vertical Frame Rate	Fr	60	Hz

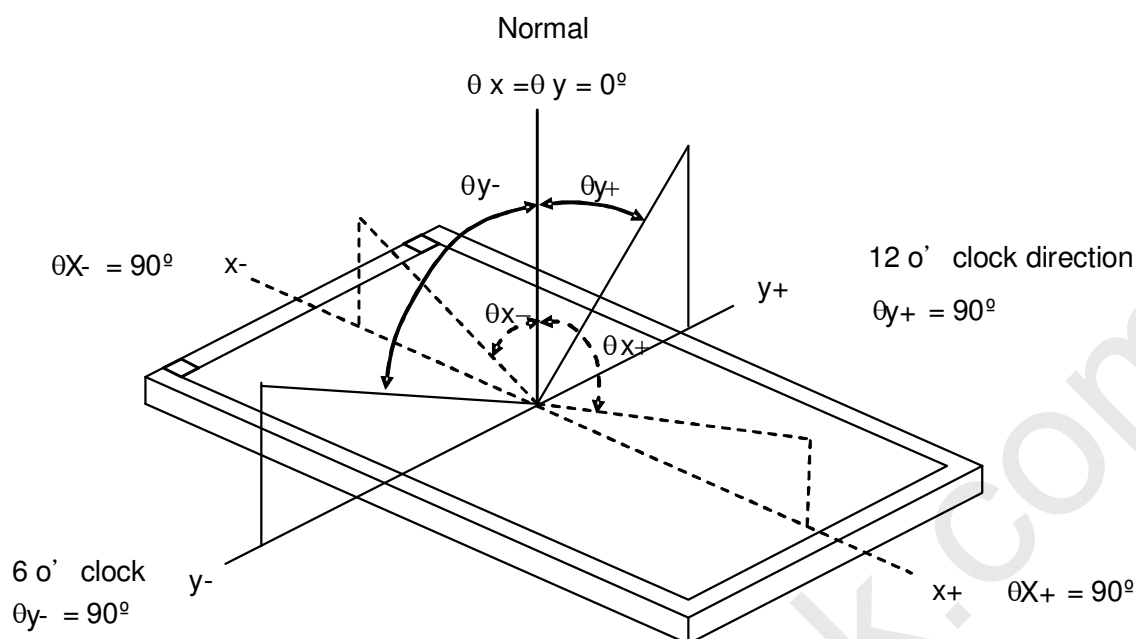
### 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio	CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Angle at Normal Direction	1200	1500		-	Note (2)	
Response Time	Gray to Gray			6	12	ms	Note (3)	
Center Luminance of White	LC		400	500		cd/m <sup>2</sup>	Note (4)	
White Variation	$\delta W$				1.25	-	Note (6)	
Color Chromaticity	Red		Rx	Typ. -0.03	0.644	Typ. +0.03	-	Note (5)
			Ry		0.333		-	
	Green		Gx		0.272		-	
			Gy		0.591		-	
	Blue		Bx		0.143		-	
			By		0.070		-	
	White	Wx	0.280		-			
		Wy	0.285		-			
Color Gamut	C.G	81	85		%	CIE 1976 NTSC		
Viewing Angle	Horizontal	$\theta_{x+}$	80	88		Deg.	Note (1)	
		$\theta_{x-}$	80	88				
	Vertical	$\theta_{y+}$	80	88				
		$\theta_{y-}$	80	88				

Note (1) Definition of Viewing Angle ( $\theta_x, \theta_y$ ):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculate by following expression

$$\text{Contrast Ratio (CR)} = L_{255}/L_0$$

L<sub>255</sub> : Luminance of gray level 255

L<sub>0</sub> : Luminance of gray level 0

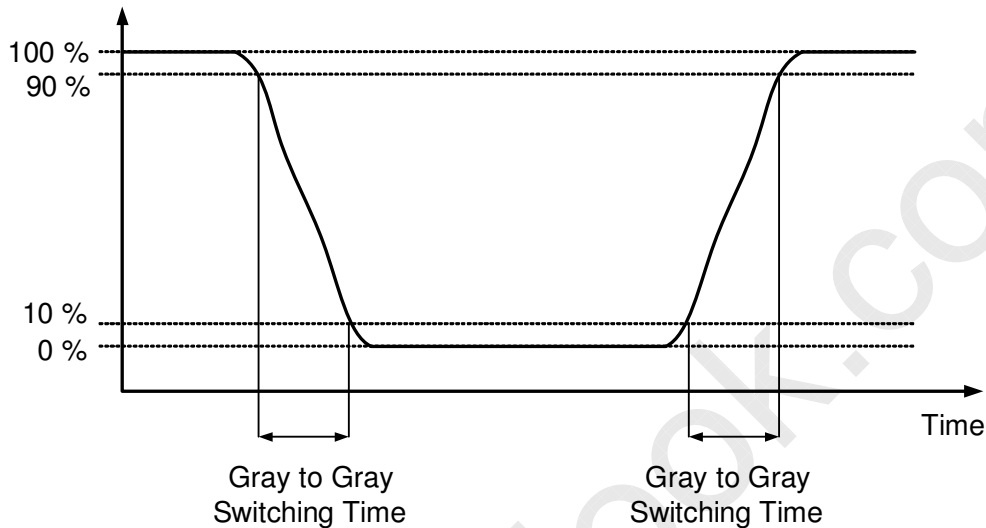
CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6)

Note (3) Definition of Gray-to-Gray Switching Time:

The driving signal means the signal of luminance 0%, 20%, 40%, 60%, 80%, 100%.

Gray to gray average time means the average switching time of luminance 0%, 20%, 40%, 60%, 80%, 100% to each other.

### Optical Response



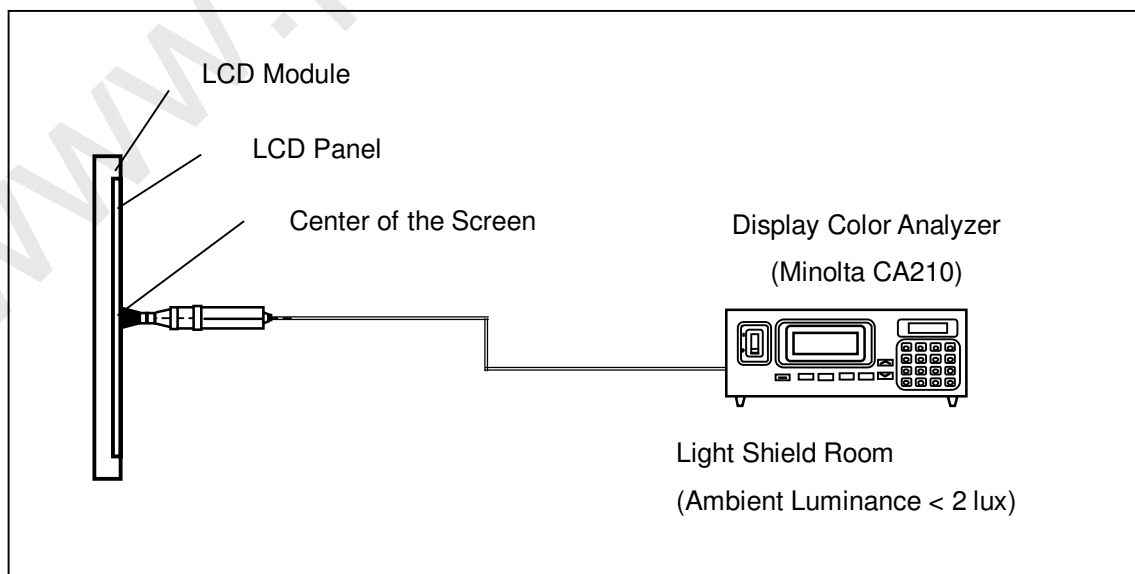
Note (4) Definition of Luminance of White (LC, LAVE):

Measure the luminance of gray level 255 at center point and 9 points

$LC = L(5)$ , where  $L(X)$  is corresponding to the luminance of the point  $X$  at the figure in Note (6).

Note (5) Measurement Setup:

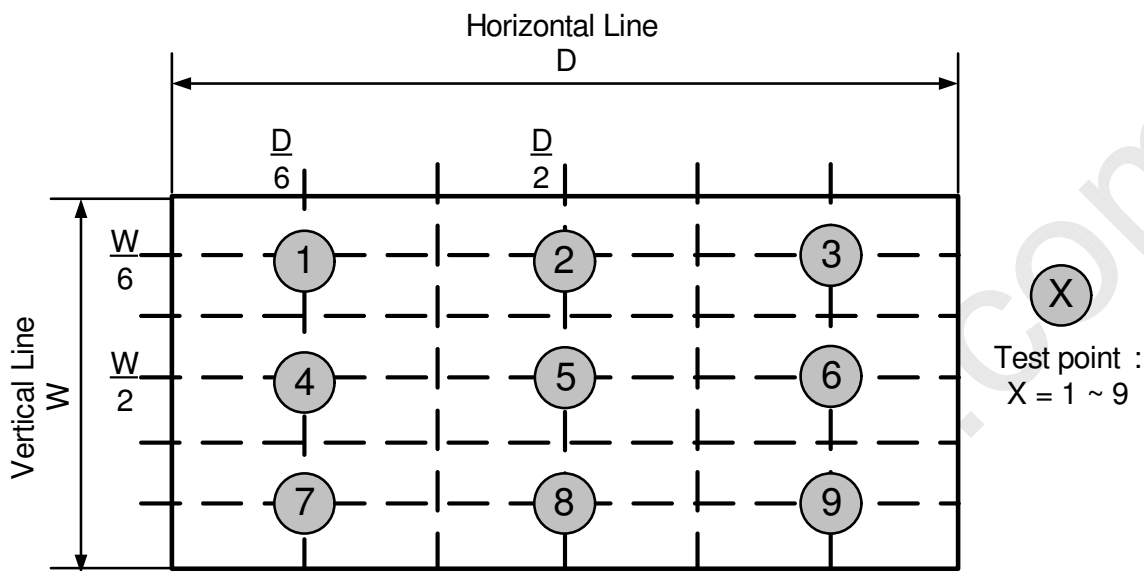
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (6) Definition of White Variation ( $\delta W$ ):

Measure the luminance of gray level 255 at 9 points

$$\delta W = \frac{\text{Maximum [L (1), L (2), L (3), L (4), L (5), L (6), L (7), L (8), L (9)]}}{\text{Minimum [L (1), L (2), L (3), L (4), L (5), L (6), L (7), L (8), L (9)]}}$$



## 8. PRECAUTIONS

### 8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [ 1 ] Do not apply rough force such as bending or twisting to the module during assembly.
- [ 2 ] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [ 3 ] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [ 4 ] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [ 5 ] Do not plug in or pull out the I/F connector while the module is in operation.
- [ 6 ] Do not disassemble the module.
- [ 7 ] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [ 8 ] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [ 9 ] When storing modules as spares for a long time, the following precaution is necessary.
  - [ 9.1 ] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
  - [ 9.2 ] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [ 10 ] When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

### 8.2 SAFETY PRECAUTIONS

- [ 1 ] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [ 2 ] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [ 3 ] After the module's end of life, it is not harmful in case of normal operation and storage.



## 9. REGULATORY STANDARD

### 9.1 SAFETY

Regulatory	Item	Standard
Audio / Video Apparatus	UL	UL 60065: 2003
	cUL	CAN/CSA C22.2 No.60065-03
	CB	IEC 60065:2001

### 9.2 EMC

[ 1 ] FFC class B part15.

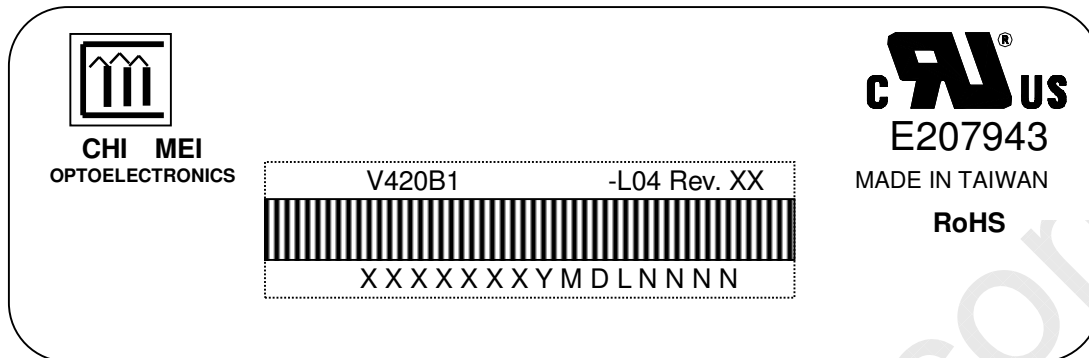
[ 2 ] CISPR20.

Note (1) CMO product can support to meet FFC class B part15 and CISPR20 standard.

## 10. DEFINITION OF LABELS

### 10.1 CMO MODULE LABEL

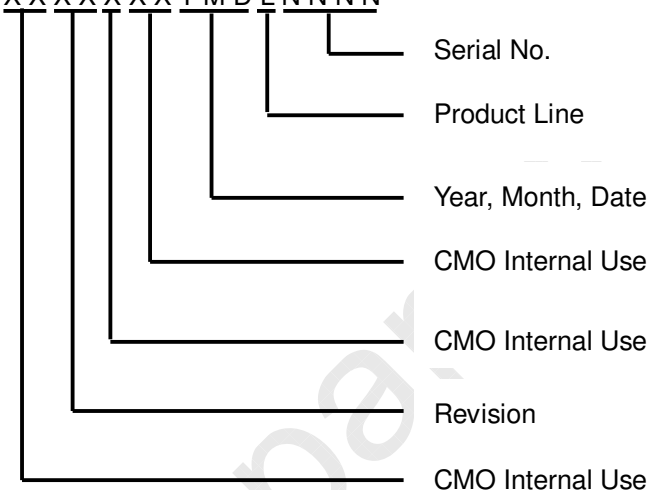
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V420B1-L04

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

## 11. PACKAGING

### 11.1 PACKAGING SPECIFICATIONS

3 LCD TV modules / 1 Box

Box dimensions: 1080(L) X 282 (W) X 685(H)

Weight: approximately 45Kg (3 modules per box)

### 11.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method.

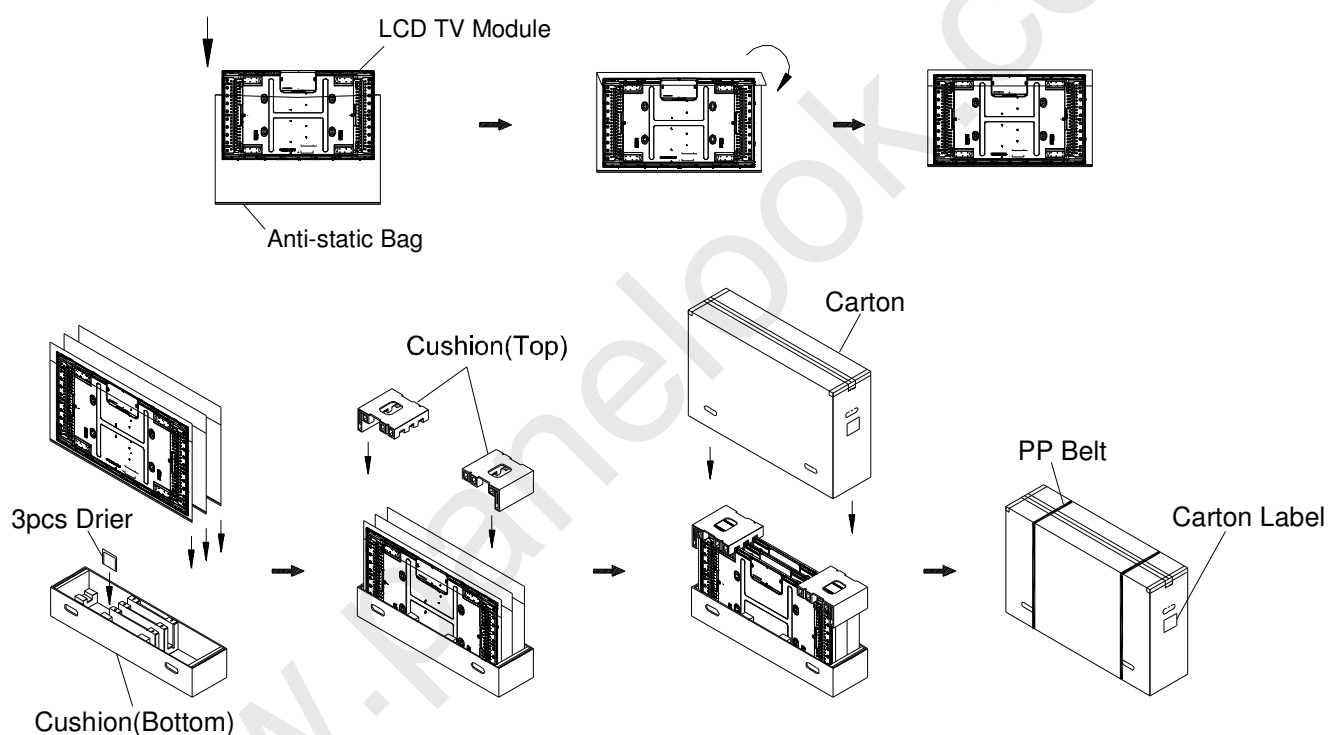
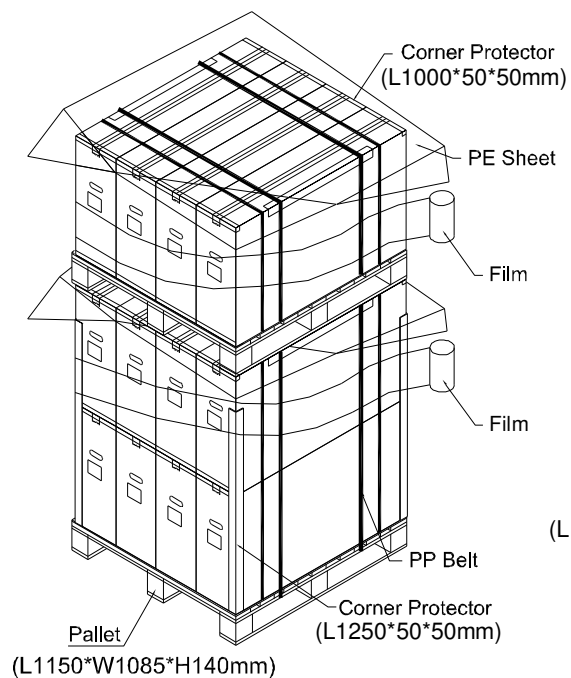


Figure.11-1 packing method

## Sea / Land Transportation (40ft HQ Container)



## Air Transportation &amp; Sea / Land Transportation (40ft Container)

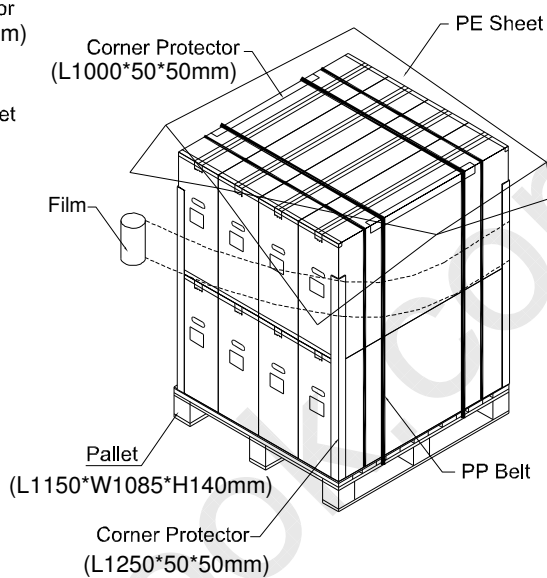
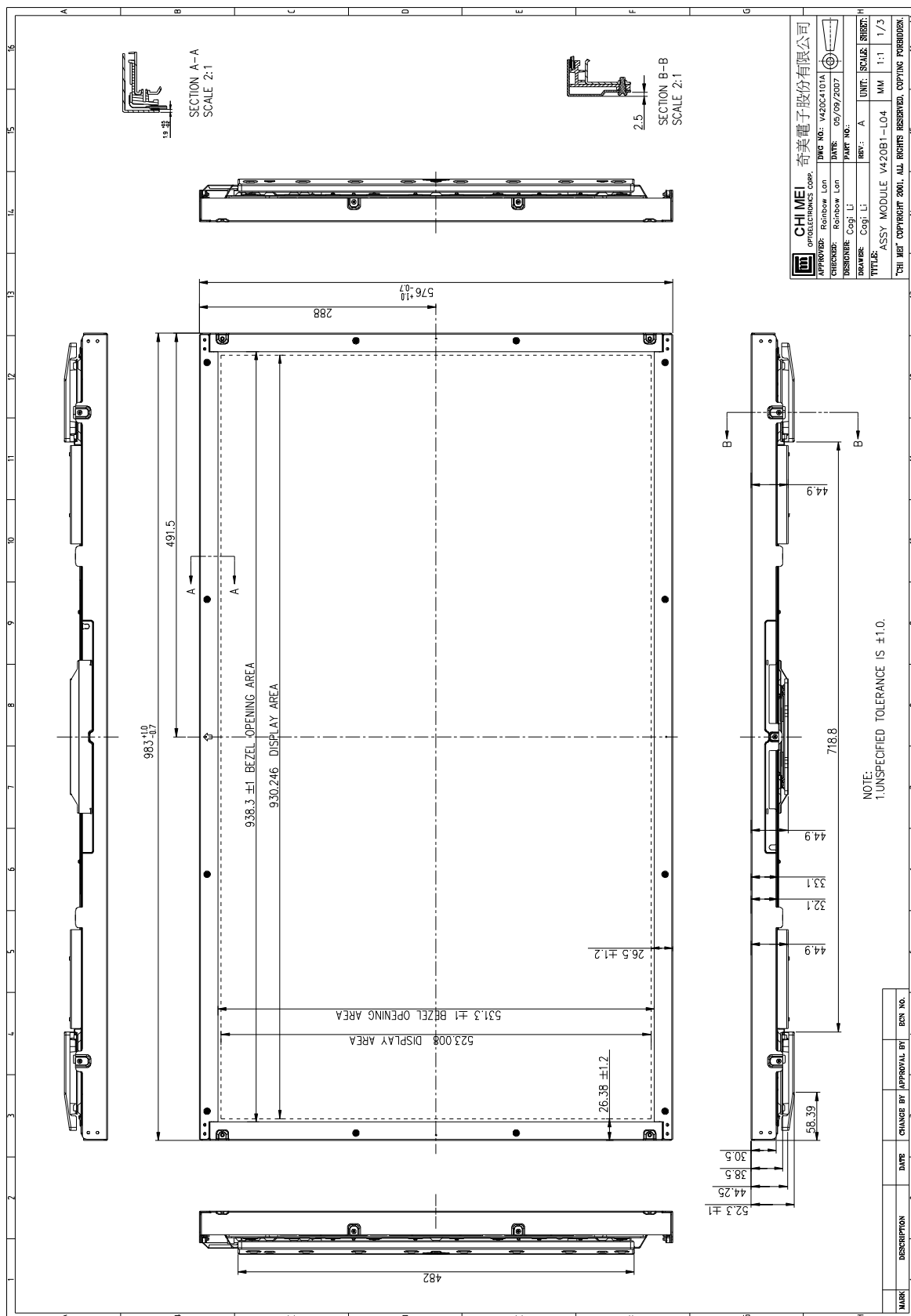
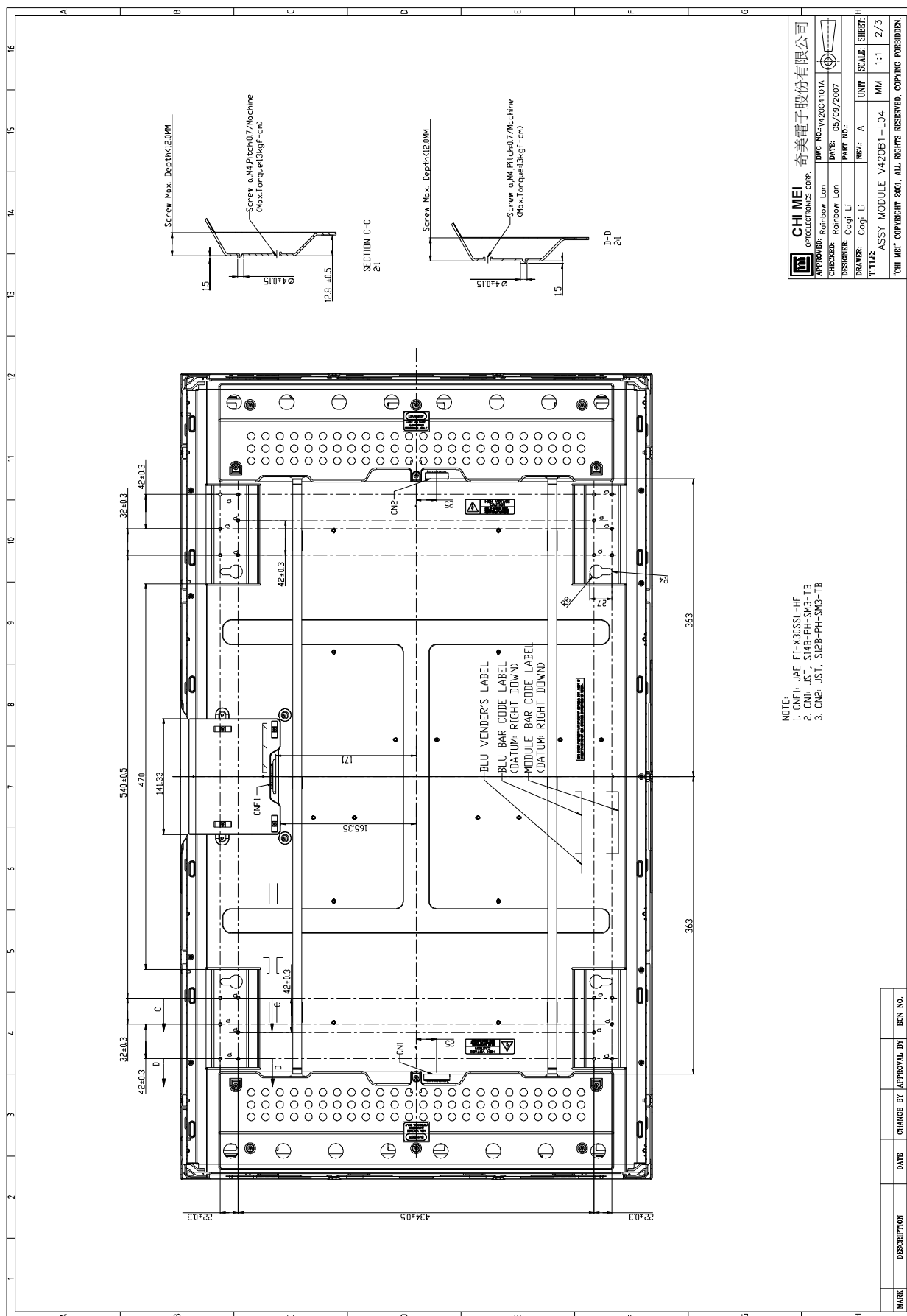


Figure.11-2 Packing method

12. MECHANICAL CHARACTERISTICS

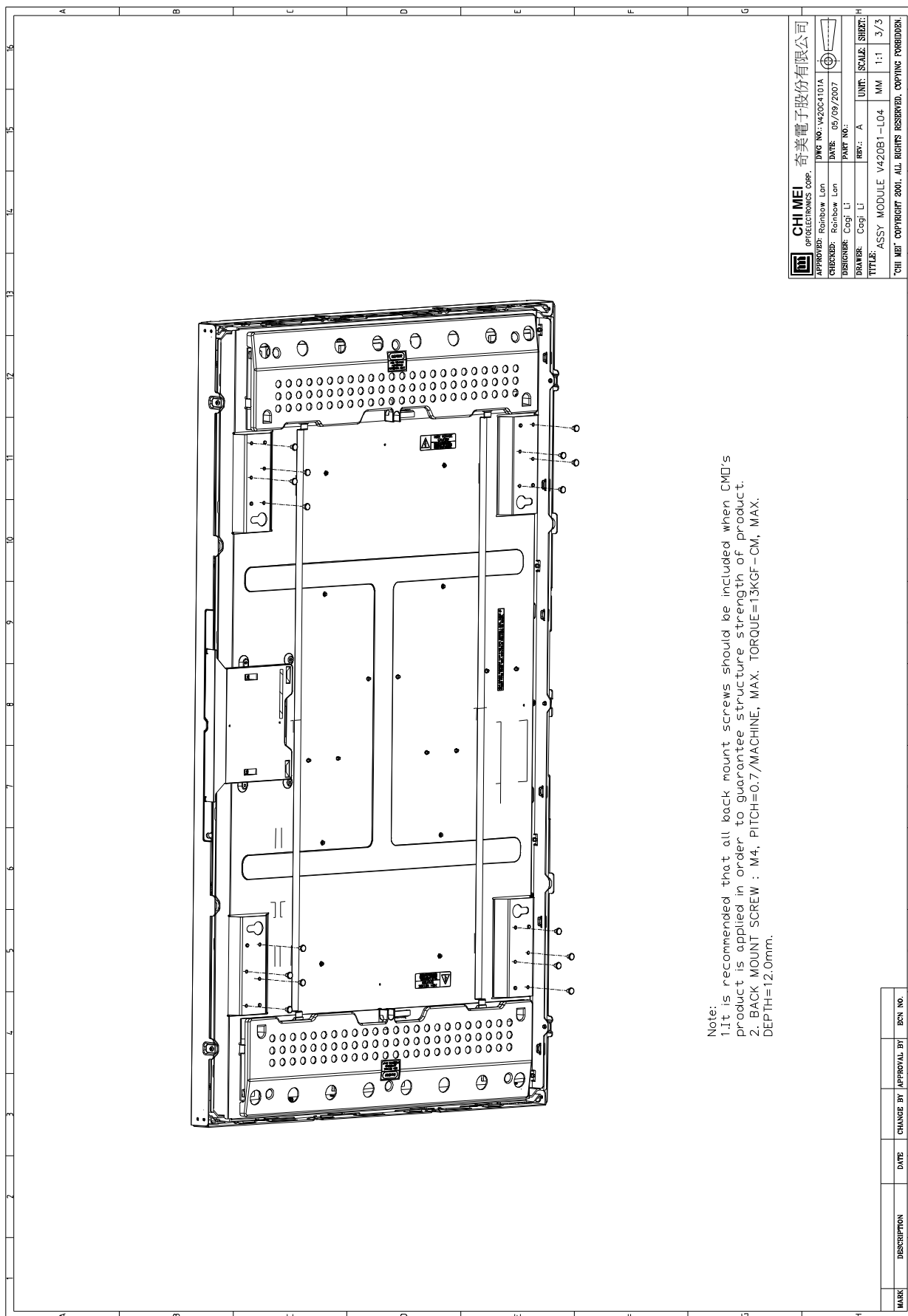




<b>CHI MEI</b> OPTOELECTRONICS CORP.		奇美電子股份有限公司	
APPROVER: Rainbow Lon	DATE: 05/09/2007	DFWG NO.: V420C4101A	UNF. SCALE: 1:1
CHECKER: Rainbow Lon	PARF. NO.:	DESIGNER: Cagt Li	MM: 2/3
DRAWER: Cagt Li	REV.: A	TITLE: ASSY MODULE V420B1-L04	SHEET: 2/3
CHI MEI COPYRIGHT 2001. ALL RIGHTS RESERVED. COPYING FORBIDDEN.			

- NOTE:  
 1. CNF1: JAE F1-X30SSL-HF  
 2. CN1: JST S14B-PH-SM3-TB  
 3. CN2: JST S12B-PH-SM3-TB

MARK	DESCRIPTION	DATE	CHANGE BY	APPROVAL BY	SCN NO.



<b>CHI MEI</b> OPTOELECTRONICS CORP.		奇美電子股份有限公司	
APPROVED: Rainbow Len	CHKD BY: Rainbow Len	DATE: 05/09/2007	DWG NO.: V420C4101A
DESIGNER: Cagj Li	DRAWN: Cagj Li	UNIT: A	SCALE: SHIRT: H
TITLE: ASSY MODULE V420B1-L04	MM 1:1	3/3	
"CHI MEI" COPYRIGHT 2001. ALL RIGHTS RESERVED. COPYING FORBIDDEN.			

Note:  
1. It is recommended that all back mount screws should be included when CM's product is applied in order to guarantee structure strength of product.  
2. BACK MOUNT SCREW : M4, PITCH=0.7/MACHINE, MAX. TORQUE=13KGF-CM, MAX. DEPTH=12.0mm.

MARK	DESCRIPTION	DATE	CHANGE BY	APPROVAL BY	ECN NO