

TFT LCD Approval Specification

MODEL NO.: V420H1 – LH7

Customer: _____
Approved by: _____
Note:

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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 0.0	Oct. 30, 2008	All	All	The tentative specification was first issued.
Ver. 1.0	Dec. 24, 2008	5 11 11-12 13-14 20 30 35	1.1 3.2.1 3.2.2 3.2.3 5.3 7.2 10.2	Modified "8 bit + FRC" to "10 bit" Updated lamp specification Updated electrical specification Updated inverter interface characteristics Updated inverter pin 12 define Updated optical specifications Updated packaging method
Ver. 1.1	Dec. 31, 2008	13	3.2.3	Add note(4)
Ver. 2.0	Jun. 1, 2009	5 9 11 11 13 26 29 30	1.2 3.1 3.2.1 3.2.2 3.2.3 6.1 7.1 7.2	Modified Response Time Modified Power Supply Current and Rush Current Modified Lamp Input Voltage, Current, and Turn On Voltage Modified Power Consumption, Power Supply Current, Input Ripple Noise, and Minimum Duty Ratio Modified Note(1)-(7) Modified Internal PWM Control Voltage and Status Signal Deleted Note (4) Updated frame rate 120Hz/100Hz max/min Modified Lamp Current Modified Response Time and Color Chromaticity

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420H1-LH7 is a 42" TFT Liquid Crystal Display module with 12-CCFL Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 1.07G colors (10bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (4000:1)
- Fast response time (Gray to gray average 4.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.24(H) x 523.26 (V) (42.02" diagonal)	mm	(1)
Bezel Opening Area	937.24 (H) x 530.26 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 11%)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	-	983.0	-	mm	(1), (2)
	Vertical (V)	-	576.0	-	mm	
	Depth (D)	-	50.8	-	mm	
Weight		-	10400	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

2. ABSOLUTE MAXIMUM RATINGS**2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

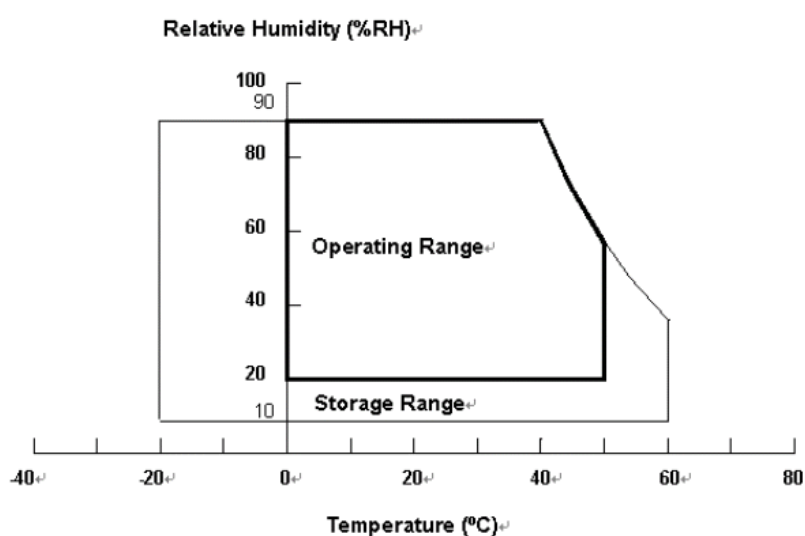
- (a) 90 %RH Max. ($T_a \leq 40$ °C).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	VW	—	3000	VRMS	
Power Supply Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.

3. ELECTRICAL CHARACTERISTICS

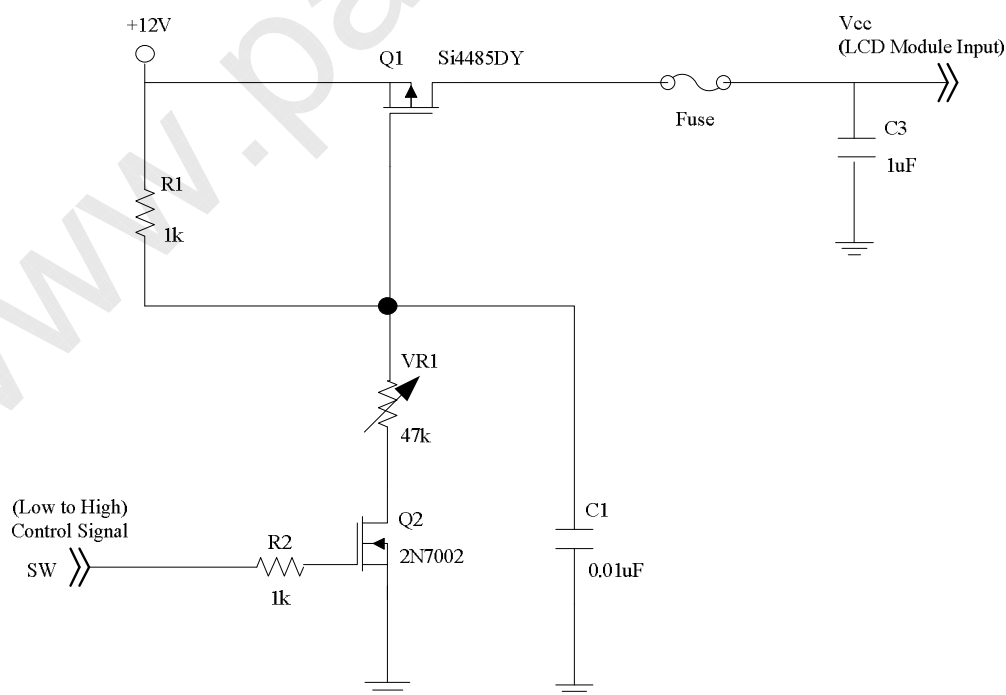
3.1 TFT LCD MODULE

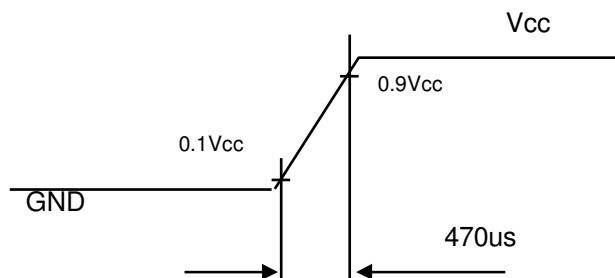
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Power Supply Ripple Voltage		V _{RP}	-	-	350	mV	
Rush Current		I _{RUSH}	-	-	5.0	A	(2)
Power Supply Current		White Pattern	-	1.6	2.0	A	(3)
		Vertical Stripe	-	1.5	-	A	
		Black Pattern	-	1.0	-	A	
LVDS interface	Common Input Voltage	V _{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R _T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

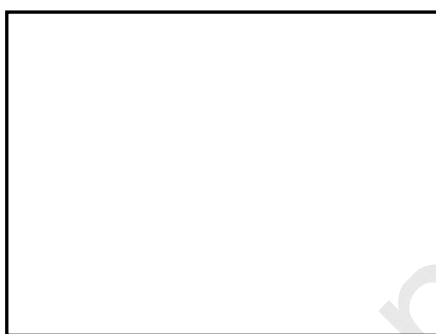
Note (2) Measurement condition:



Vcc rising time is 470us


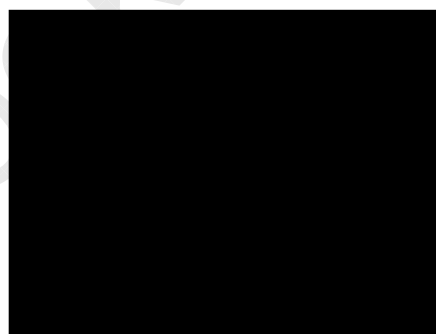
Note (3) The specified power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^\circ\text{C}$, $f_v = 120\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



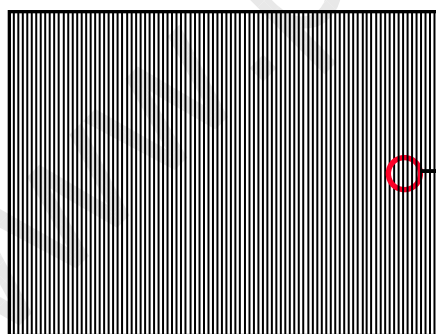
Active Area

b. Black Pattern

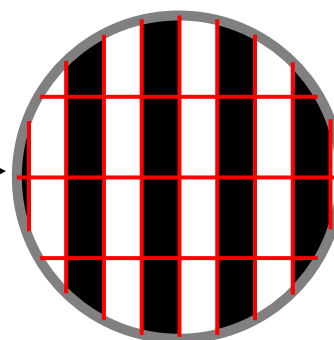


Active Area

c. Vertical Stripe Pattern



Active Area



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LAMP SPECIFICATION

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	VL	-	1090	-	VRMS	-
Lamp Current	IL	9.7	10.2	10.7	mARMS	(1)
		8.2	8.7	9.2		
Lamp Turn On Voltage	VS	-	-	1910	VRMS	Ta = 0 °C(2)
		-	-	1520	VRMS	Ta = 25 °C(2)
Operating Frequency	FL	35	-	70	KHz	
Lamp Life Time	LBL	50,000	60,000	-	Hrs	(4)

3.2.2 ELECTRICAL SPECIFICATION

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL}	-	130	133	W	(5),(6) IL = 10.2 mA
			110	112		(5),(6) IL = 8.7 mA
Power Supply Voltage	V _{BL}	22.8	24.0	25.2		
Power Supply Current	I _{BL}		5.4	5.6	A	Non Dimming
			4.6	4.7		
Input Ripple Noise	-	-		912	mV _{p-p}	V _{BL} =22.8V
Oscillating Frequency	F _w	39	42	45	kHz	(3)
Dimming Frequency	F _B	150	160	170	Hz	
Minimum Duty Ratio	D _{MIN}	10	20	-	%	(7)

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

Note (2) The lamp starting voltage V_s should be applied to the lamp for more than 1 second after startup.

Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the

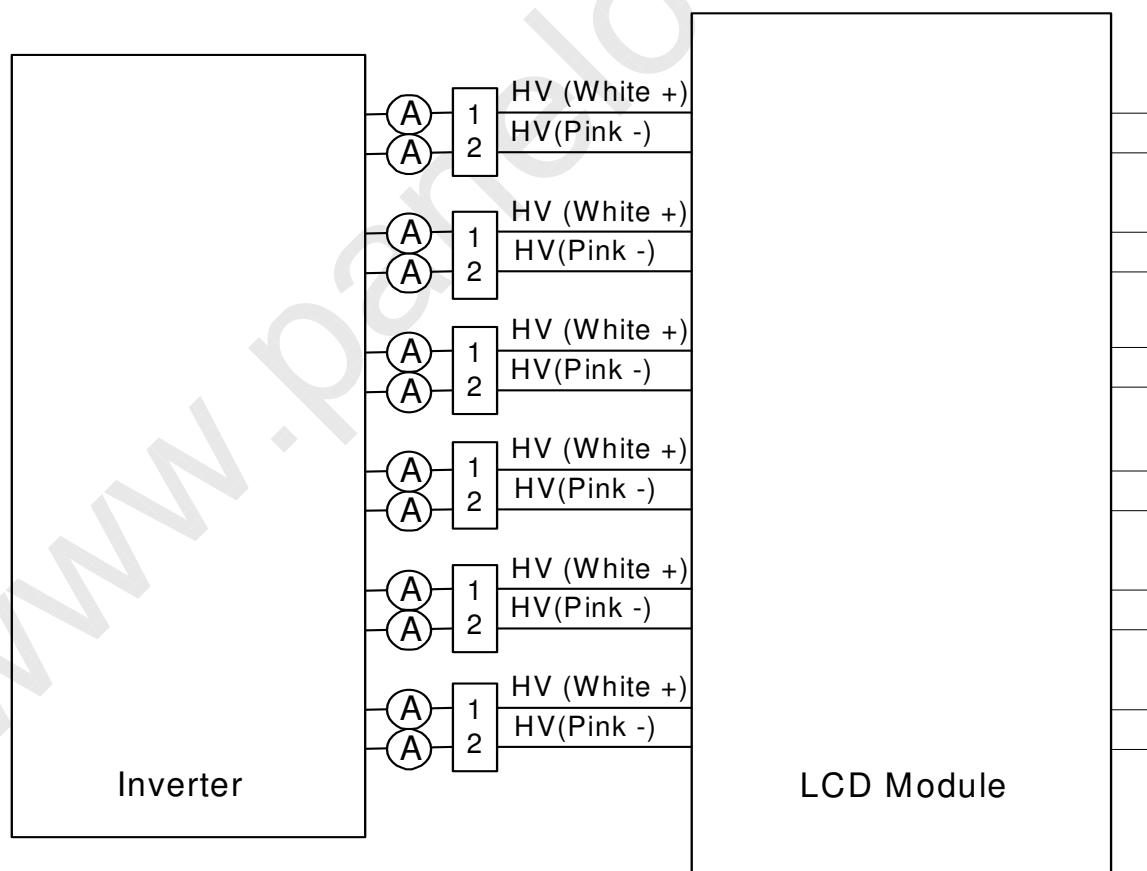
lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at $T_a = 25 \pm 2^\circ\text{C}$ and $I_L = 8.2 \sim 10.7\text{mA}_{\text{rms}}$.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL} . Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 42" backlight unit under input voltage 24V, average lamp current 6.1 mA and lighting 30 minutes later.

Note (7) 10% minimum duty ratio is only valid for electrical operation



3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	5.0	5.0	V	
	OFF		—	0	0.8	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	—	2.85	3.0	3.15	V	Maximum duty ratio
	MIN		—	—	0	—	V	Minimum duty ratio
Status Signal	HI	Status	—	3.0	3.3	3.6	V	Normal
	LO		—	0	0.8	0.8	V	Abnormal
VBL Rising Time		$Tr1$	—	30	—	—	ms	10%-90% V_{BL}
VBL Falling Time		$Tf1$	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input Impedance		R_{IN}	—	1	—	—	MΩ	
PWM Delay Time		T_{PWM}	—	100	—	—	ms	
BLON Delay Time	T_{on}	—	—	300	—	—	ms	
	T_{on1}	—	—	300	—	—	ms	
BLON Off Time		T_{off}	—	300	—	—	ms	

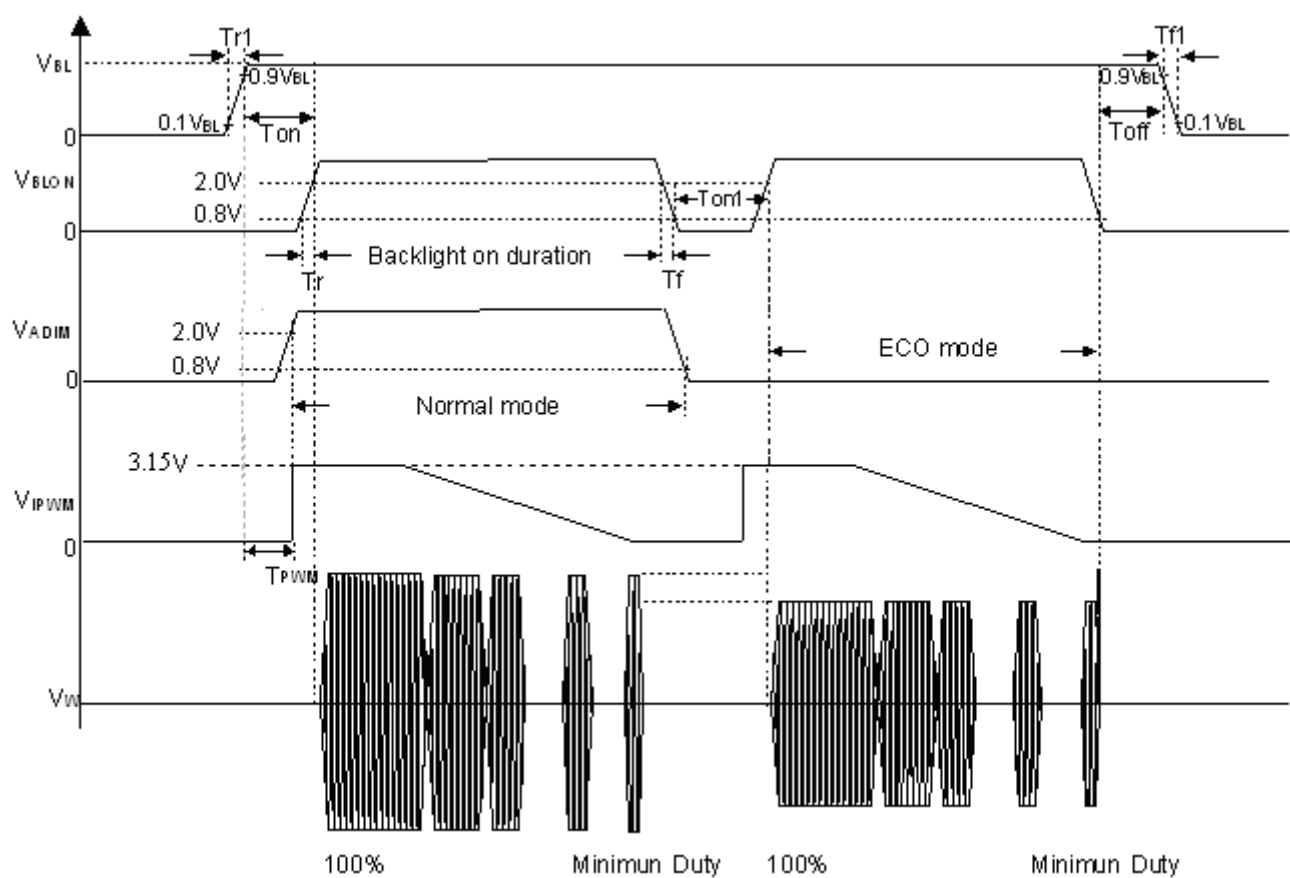
Note (1) The dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure.

Note (3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

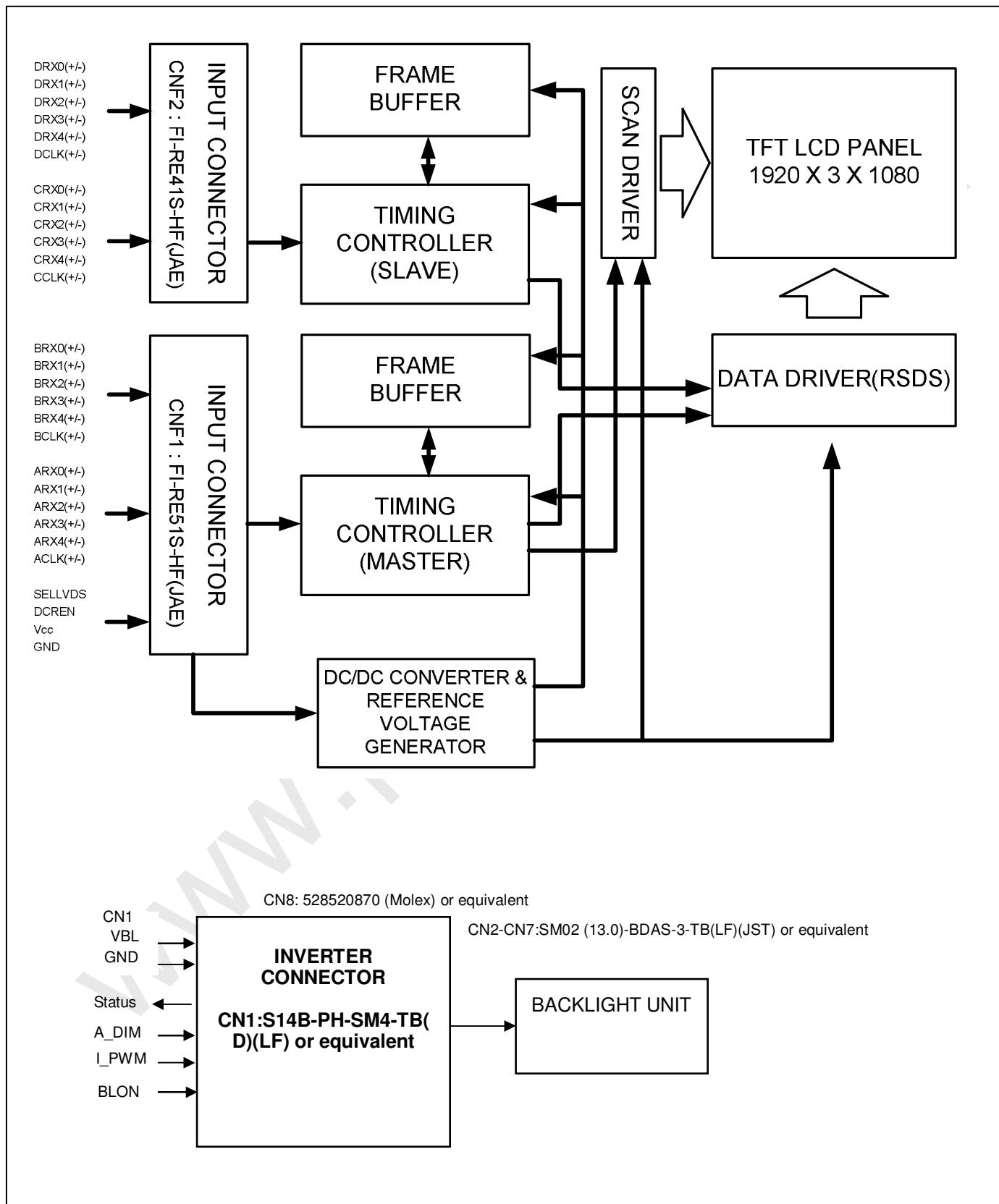
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Pin Assignment (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	(1)
11	GND	Ground	
12	ARX0-	First pixel Negative LVDS differential data input. Channel 0	
13	ARX0+	First pixel Positive LVDS differential data input. Channel 0	
14	ARX1-	First pixel Negative LVDS differential data input. Channel 1	
15	ARX1+	First pixel Positive LVDS differential data input. Channel 1	
16	ARX2-	First pixel Negative LVDS differential data input. Channel 2	
17	ARX2+	First pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ACLK-	First pixel Negative LVDS differential clock input.	
20	ACLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ARX3-	First pixel Negative LVDS differential data input. Channel 3	
23	ARX3+	First pixel Positive LVDS differential data input. Channel 3	
24	ARX4-	First pixel Negative LVDS differential data input. Channel 4	
25	ARX4+	First pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	(1)

28	BRX0-	Second pixel Negative LVDS differential data input. Channel 0	
29	BRX0+	Second pixel Positive LVDS differential data input. Channel 0	
30	BRX1-	Second pixel Negative LVDS differential data input. Channel 1	
31	BRX1+	Second pixel Positive LVDS differential data input. Channel 1	
32	BRX2-	Second pixel Negative LVDS differential data input. Channel 2	
33	BRX2+	Second pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	BCLK-	Second pixel Negative LVDS differential clock input.	
36	BCLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	BRX3-	Second pixel Negative LVDS differential data input. Channel 3	
39	BRX3+	Second pixel Positive LVDS differential data input. Channel 3	
40	BRX4-	Second pixel Negative LVDS differential data input. Channel 4	
41	BRX4+	Second pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF2 Connector Pin Assignment (FI-RE41S(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)

6	N.C.	No Connection	(1)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	(1)
9	GND	Ground	
10	CRX0-	Third pixel Negative LVDS differential data input. Channel 0	
11	CRX0+	Third pixel Positive LVDS differential data input. Channel 0	
12	CRX1-	Third pixel Negative LVDS differential data input. Channel 1	
13	CRX1+	Third pixel Positive LVDS differential data input. Channel 1	
14	CRX2-	Third pixel Negative LVDS differential data input. Channel 2	
15	CRX2+	Third pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	CCLK-	Third pixel Negative LVDS differential clock input.	
18	CCLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CRX3-	Third pixel Negative LVDS differential data input. Channel 3	
21	CRX3+	Third pixel Positive LVDS differential data input. Channel 3	
22	CRX4-	Third pixel Negative LVDS differential data input. Channel 4	
23	CRX4+	Third pixel Positive LVDS differential data input. Channel 4	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	(1)
26	DRX0-	Fourth pixel Negative LVDS differential data input. Channel 0	
27	DRX0+	Fourth pixel Positive LVDS differential data input. Channel 0	
28	DRX1-	Fourth pixel Negative LVDS differential data input. Channel 1	
29	DRX1+	Fourth pixel Positive LVDS differential data input. Channel 1	
30	DRX2-	Fourth pixel Negative LVDS differential data input. Channel 2	
31	DRX2+	Fourth pixel Positive LVDS differential data input. Channel 2	
32	GND	Ground	
33	DCLK-	Fourth pixel Negative LVDS differential clock input.	
34	DCLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	DRX3-	Fourth pixel Negative LVDS differential data input. Channel 3	

37	DRX3+	Fourth pixel Positive LVDS differential data input. Channel 3	
38	DRX4-	Fourth pixel Negative LVDS differential data input. Channel 4	
39	DRX4+	Fourth pixel Positive LVDS differential data input. Channel 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	(1)

Note (1) Please be reserved to open.

Note (2) Low or Open: VESA Format (Default), High: JEIDA Format.

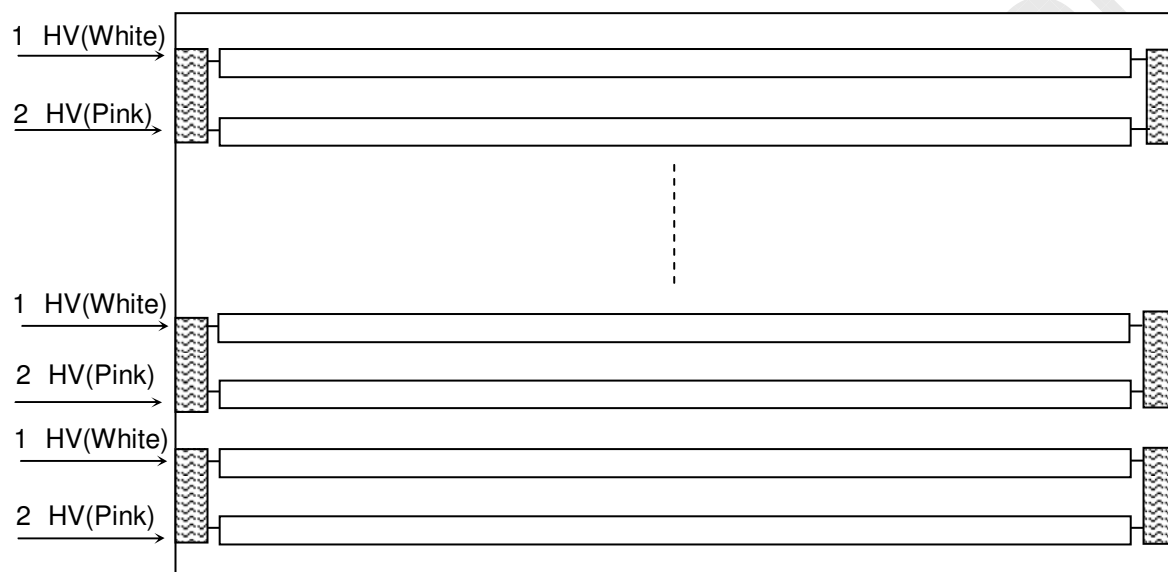
Note (3) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9,1913, 1917
2nd Port	Second Pixel	2, 6, 10,1914, 1918
3rd Port	Third Pixel	3, 7, 11,1915, 1919
4th Port	Fourth Pixel	4, 8, 12,1916, 1920

5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

Pin	Name	Description	Wire Color
1	HV	High Voltage	White
2	HV	High Voltage	Pink



5.3 INVERTER UNIT

CN1: S14B-PH-SM4-TB(D)(LF)(JST) or equivalent

Pin No	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	STATUS	Normal (3.3V) Abnormal(GND)
12	A_DIM	Amplitude Dimming Control HI (2.0V ~ 5.0V) LO(0~0.8V)
13	I_PWM	Internal PWM Control Signal
14	BLON	BL ON/OFF

CN2-CN7: SM02 -BDAS-3-TB(JST) or equivalent

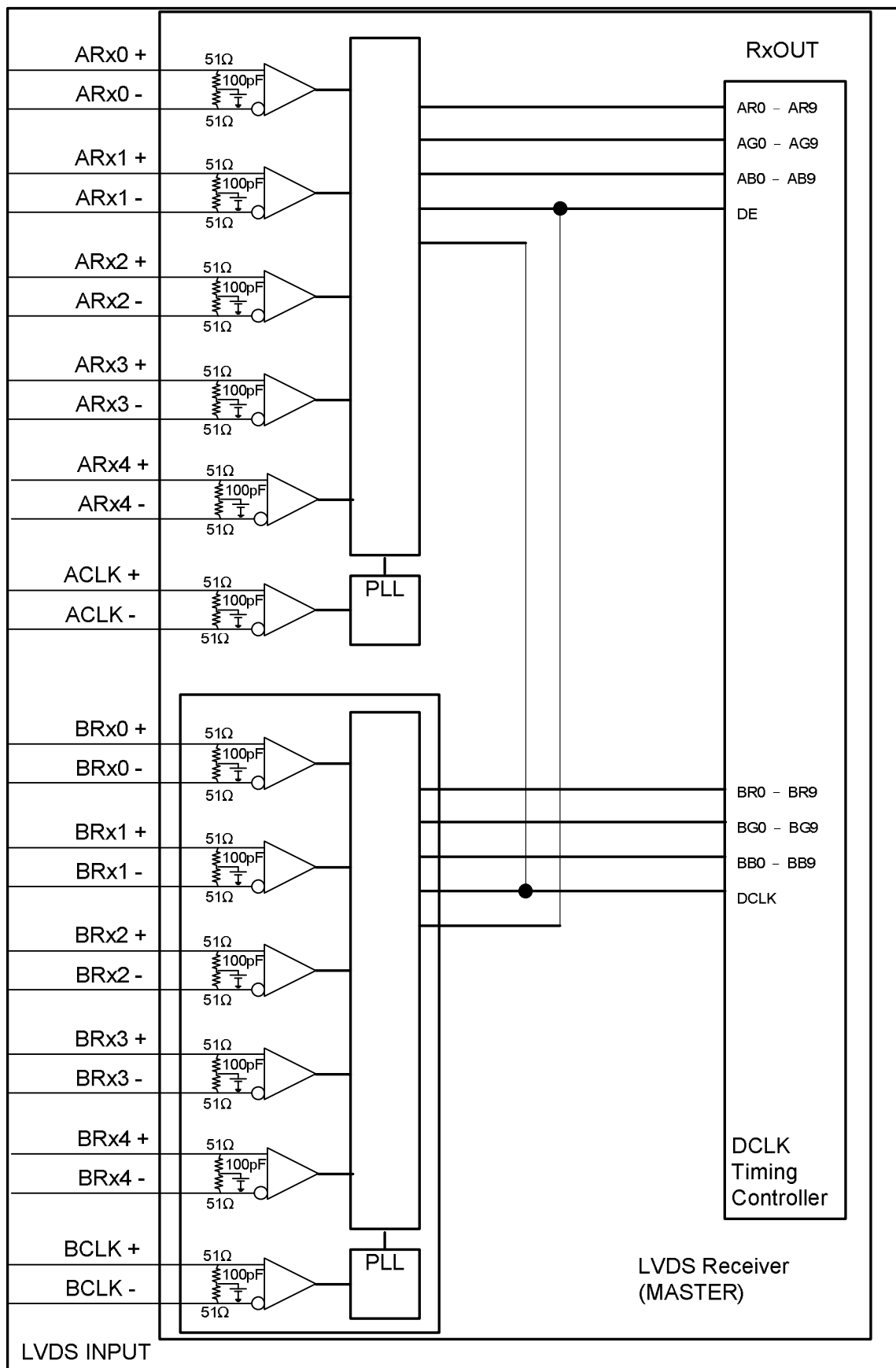
Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN8: 528520870 (Molex) or equivalent

Pin No.	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board

Note (1) Floating of any control signal is not allowed.

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

Notes (1) The system must have the transmitter to drive the module.

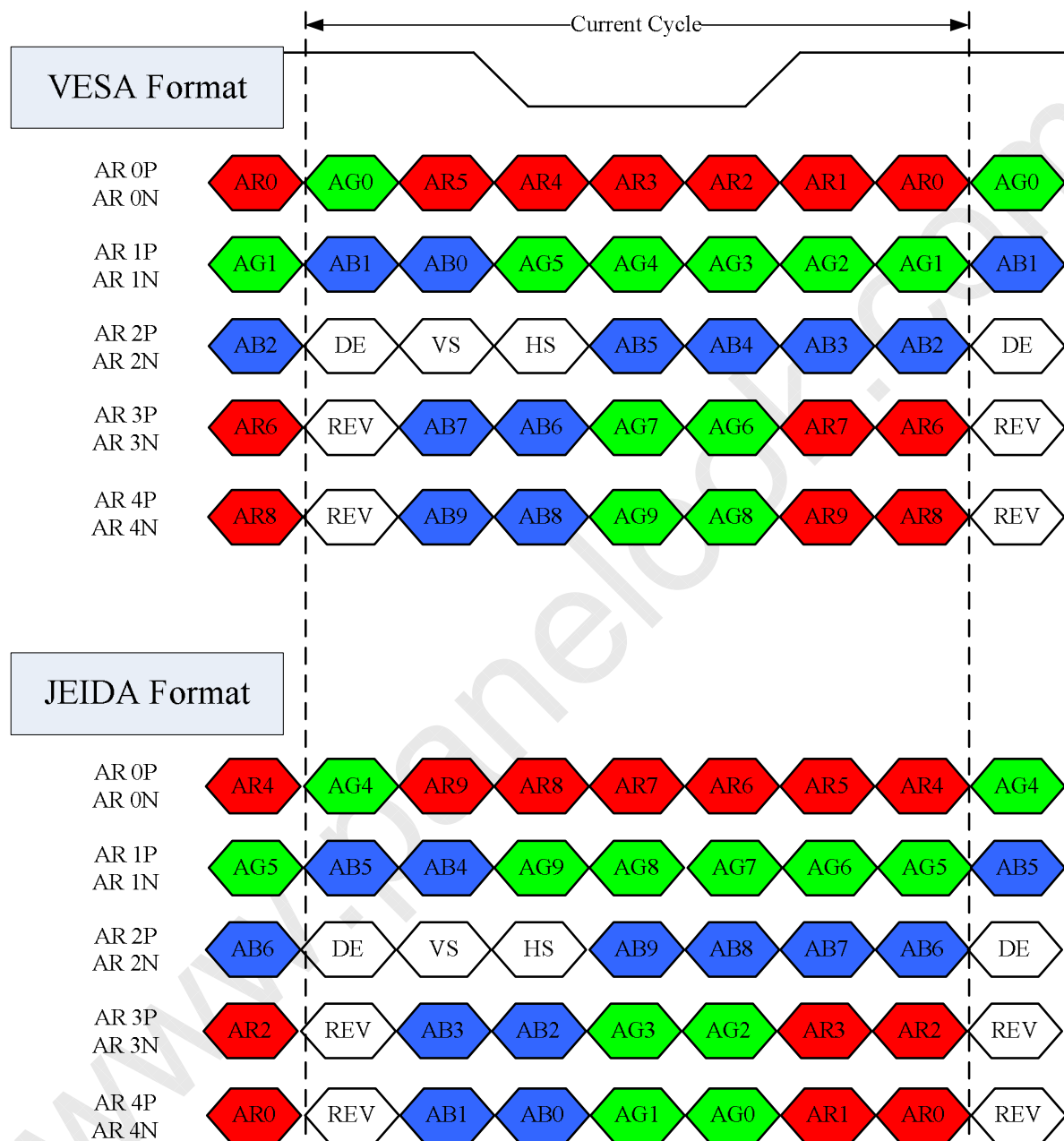
Notes (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Notes (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.5 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

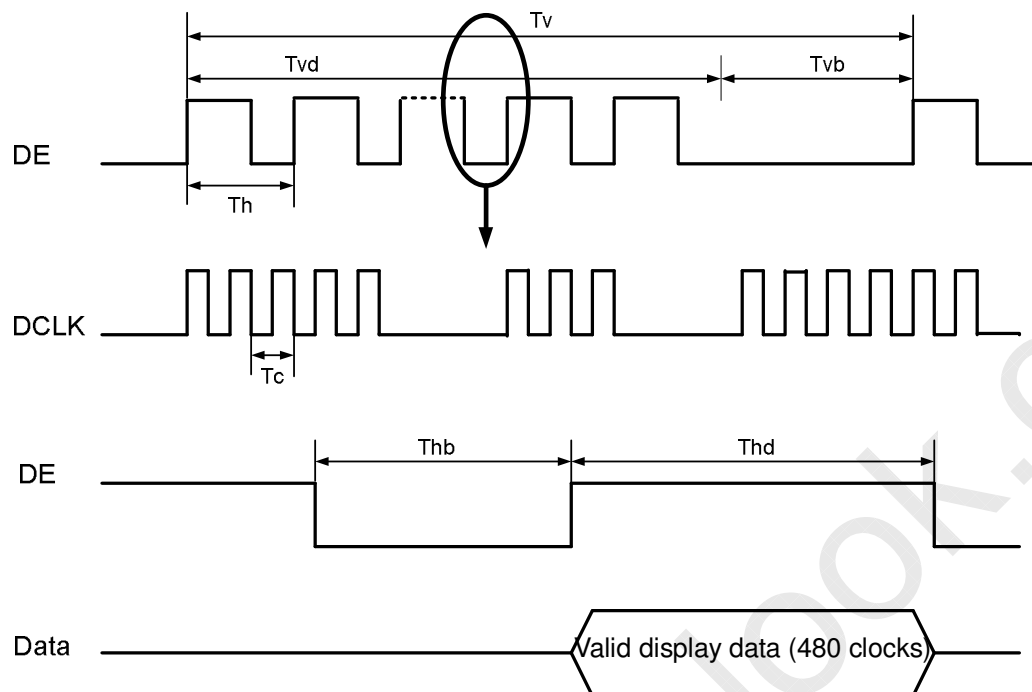
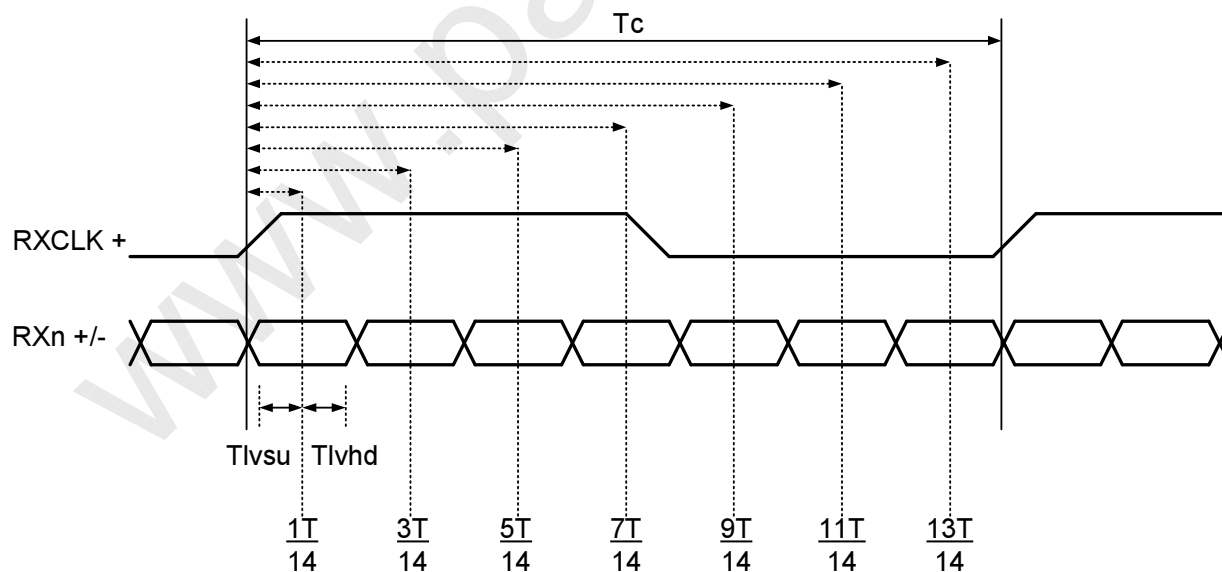
(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	80	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate		117	120	123	Hz	
	Total	Tv	1115	1125	1139	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	59	Th	-
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	60	70	95	Tc	-

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	80	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
	Frame Rate		97	100	103	Hz	
	Total	Tv	1115	1125	1139	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	59	Th	-
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	60	70	95	Tc	-

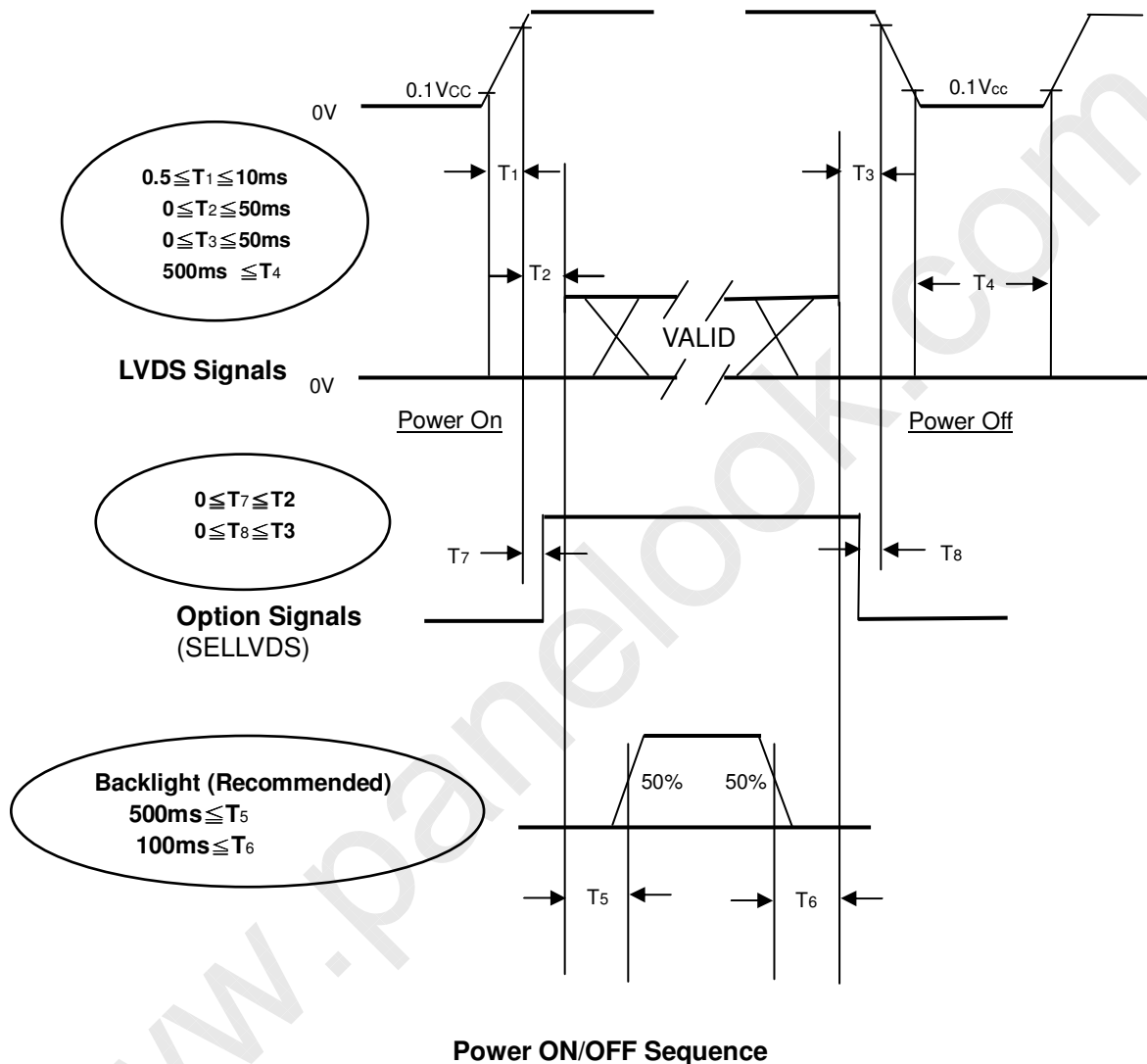
Note : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM**LVDS INPUT INTERFACE TIMING DIAGRAM**

6.2 POWER ON/OFF SEQUENCE

($T_a = 25 \pm 2 \text{ }^\circ\text{C}$)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of V_{cc} .

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of V_{cc} is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.

Note (4) T_4 should be measured after the module has been fully discharged between power off and on period.

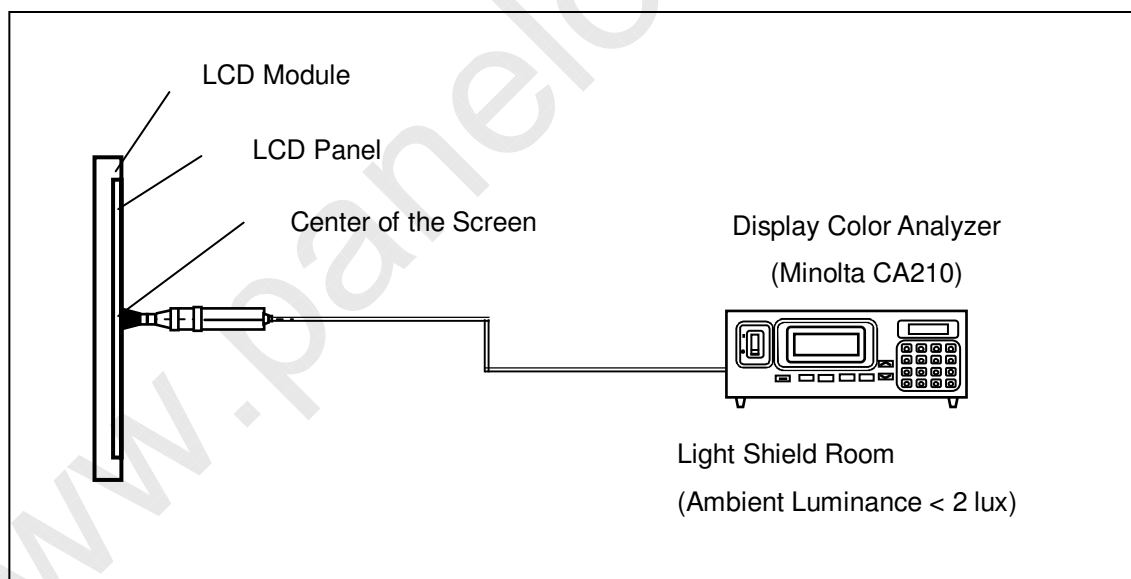
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	10.2	mA
Oscillating Frequency (Inverter)	FW	TBD	KHz
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



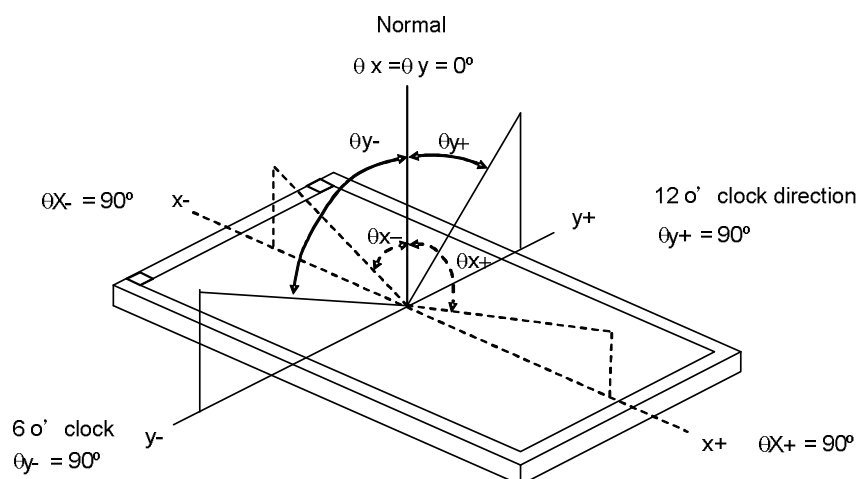
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR			4000	-	-	Note (2)
Response Time		Gray to gray		-	4.5	-	ms	Note (3)
Center Luminance of White		LC		-	500	-	cd/m ²	Note (4)
White Variation		δW		-	-	1.3	-	Note (6)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	Typ. -0.03	0.640	Typ. +0.03	-	-
		Ry			0.332		-	
	Green	Gx			0.267		-	
		Gy			0.595		-	
	Blue	Bx			0.150		-	
		By			0.063		-	
	White	Wx			0.280		-	
		Wy			0.285		-	
	Color Gamut	C.G					-	
Viewing Angle	Horizontal	θ_{x+}	CR \geq 20	80	88	-	Deg.	Note (1)
		θ_{x-}		80	88	-		
	Vertical	θ_{Y+}		80	88	-		
		θ_{Y-}		80	88	-		
Gamma			-	2.2	-	-	-	

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

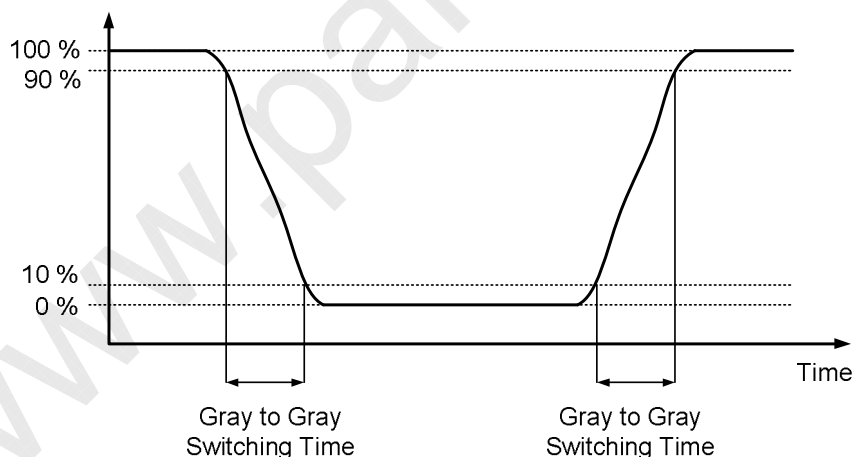
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:

Optical Response



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892, 1023 to each other.

Note (4) Definition of Luminance of White (L_C , L_{AVE}):

Measure the luminance of gray level 1023 at center point and 5 points

$L_C = L(5)$, where $L(X)$ is corresponding to the luminance of the point X at the figure in Note (6).

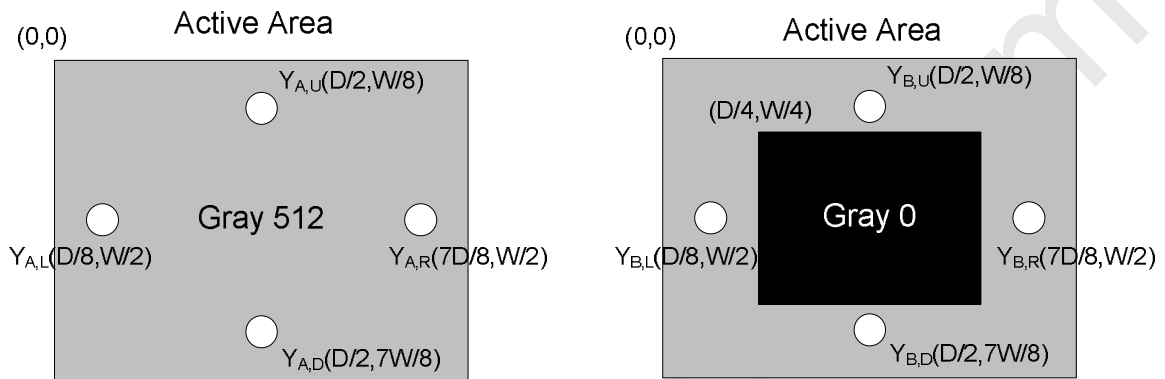
Note (5) Definition of Cross Talk (CT):

$$CT = |YB - YA| / YA \times 100 (\%)$$

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m²)

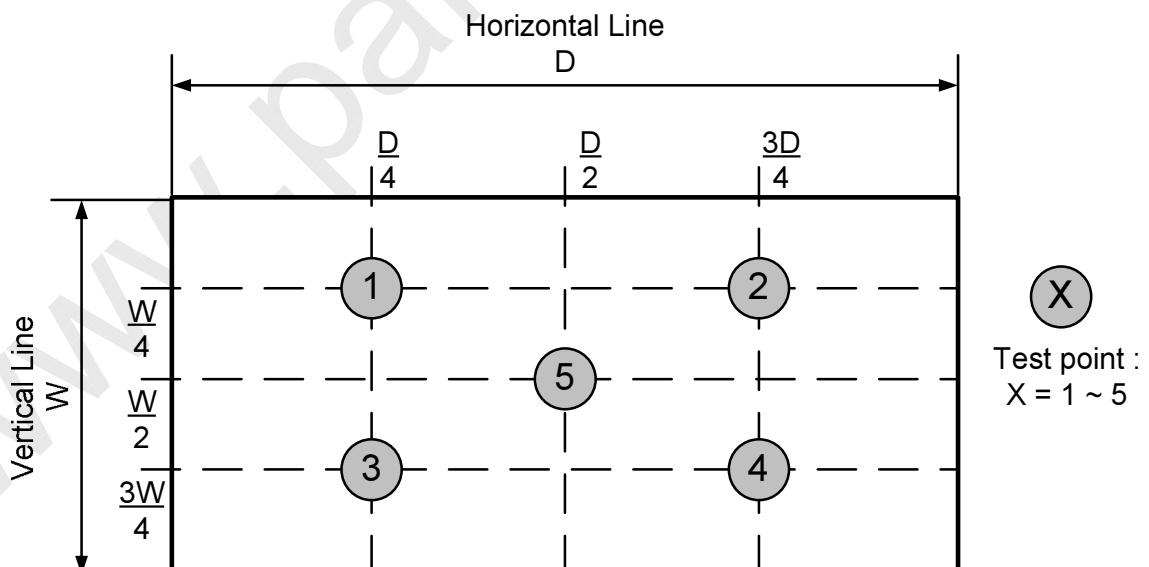
YB = Luminance of measured location with gray level 0 pattern (cd/m²)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$



Note (7) ECO mode:

ECO mode was selected by inverter pin: A_DIM.

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [1] Do not apply rough force such as bending or twisting to the module during assembly.
- [2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [5] Do not plug in or pull out the I/F connector while the module is in operation.
- [6] Do not disassemble the module.
- [7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [8] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [9] When storing modules as spares for a long time, the following precaution is necessary.
 - [9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
 - [9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [10] When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

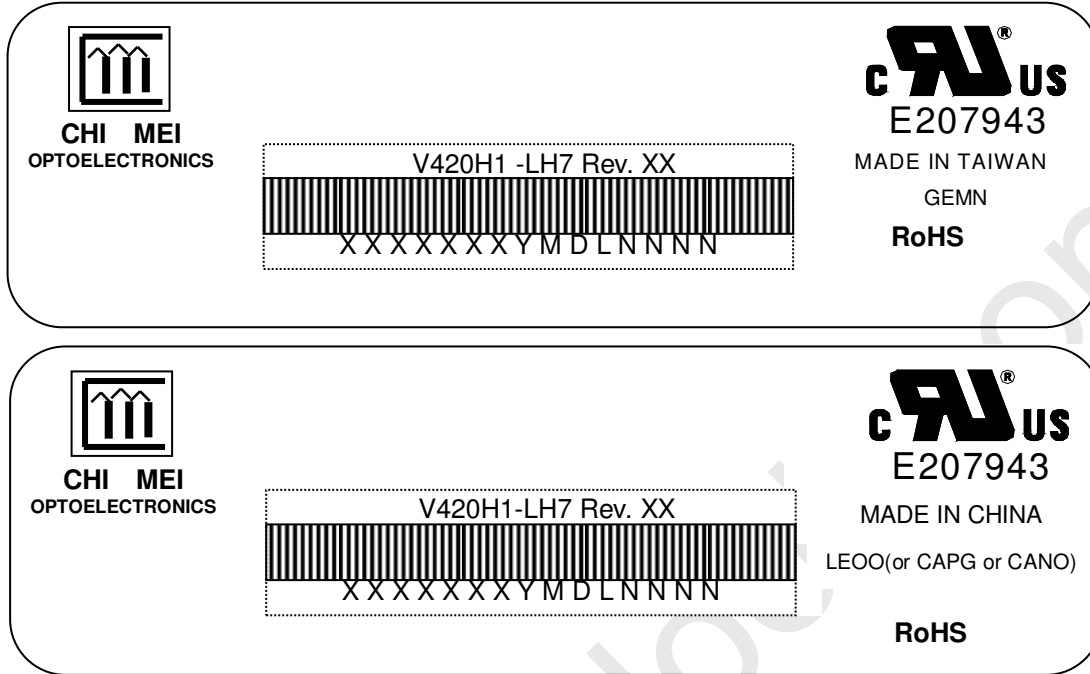
8.2 SAFETY PRECAUTIONS

- [1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

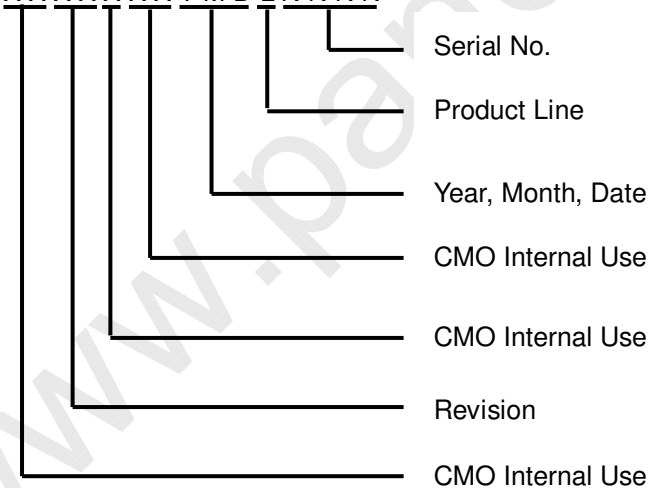
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V420H1-LH7

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

- (1) 4 LCD TV modules / 1 Box
- (2) Box dimensions : 1100(L)x317(W)x670(H)mm
- (3) Weight : Approx. 53.17Kg(4 modules per carton)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

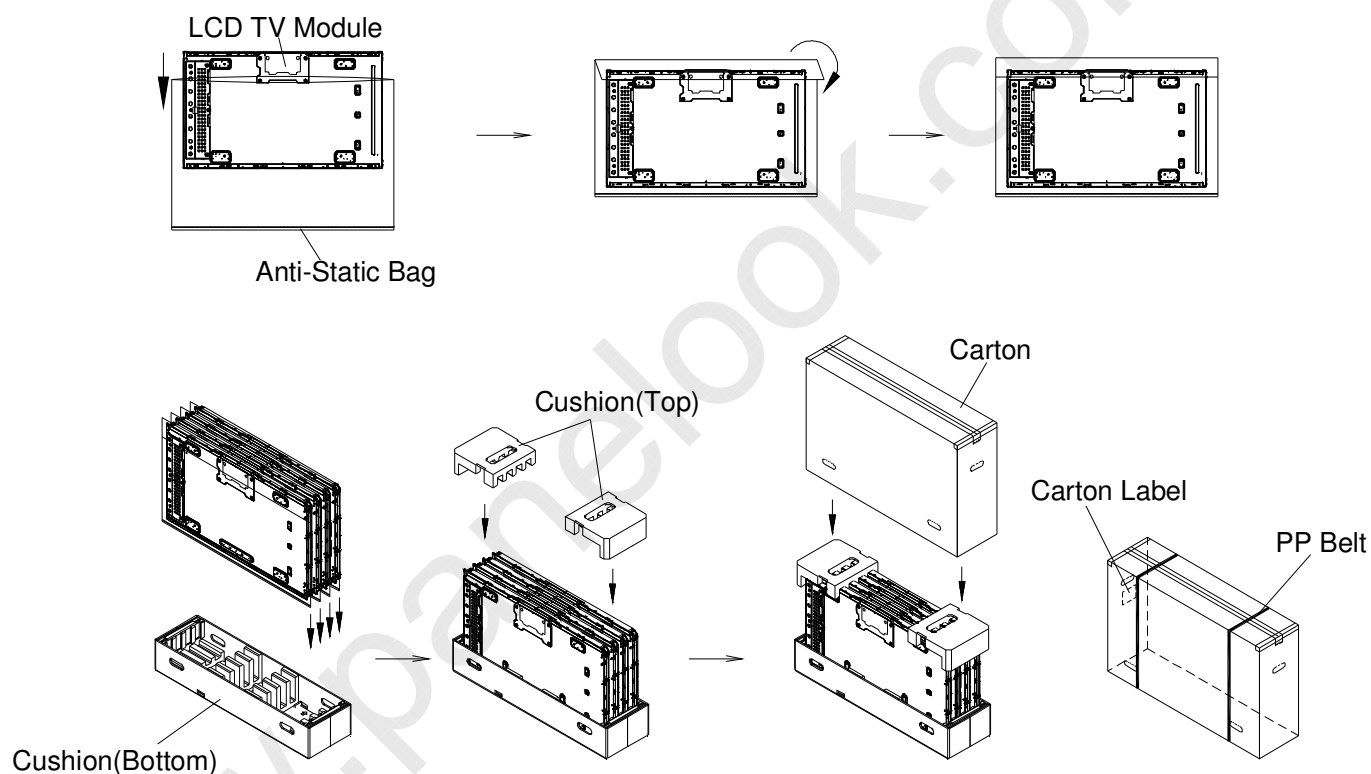
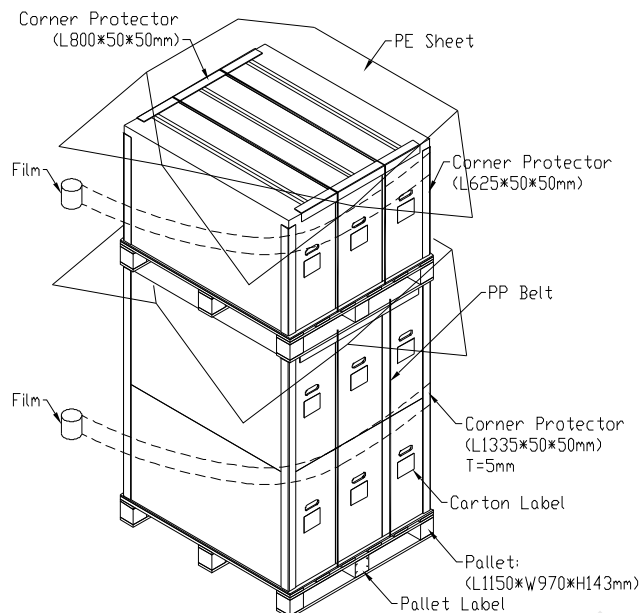


Figure.10-1 packing method



Sea / Land Transportation
(40ft HQ Container)



Air Transportation
&
Sea / Land Transportation
(40ft Container)

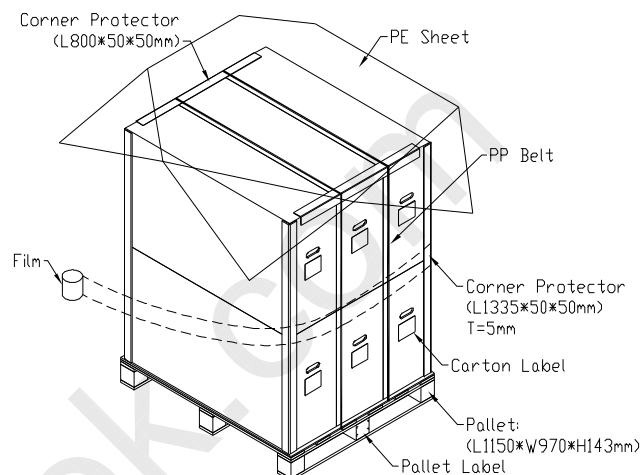
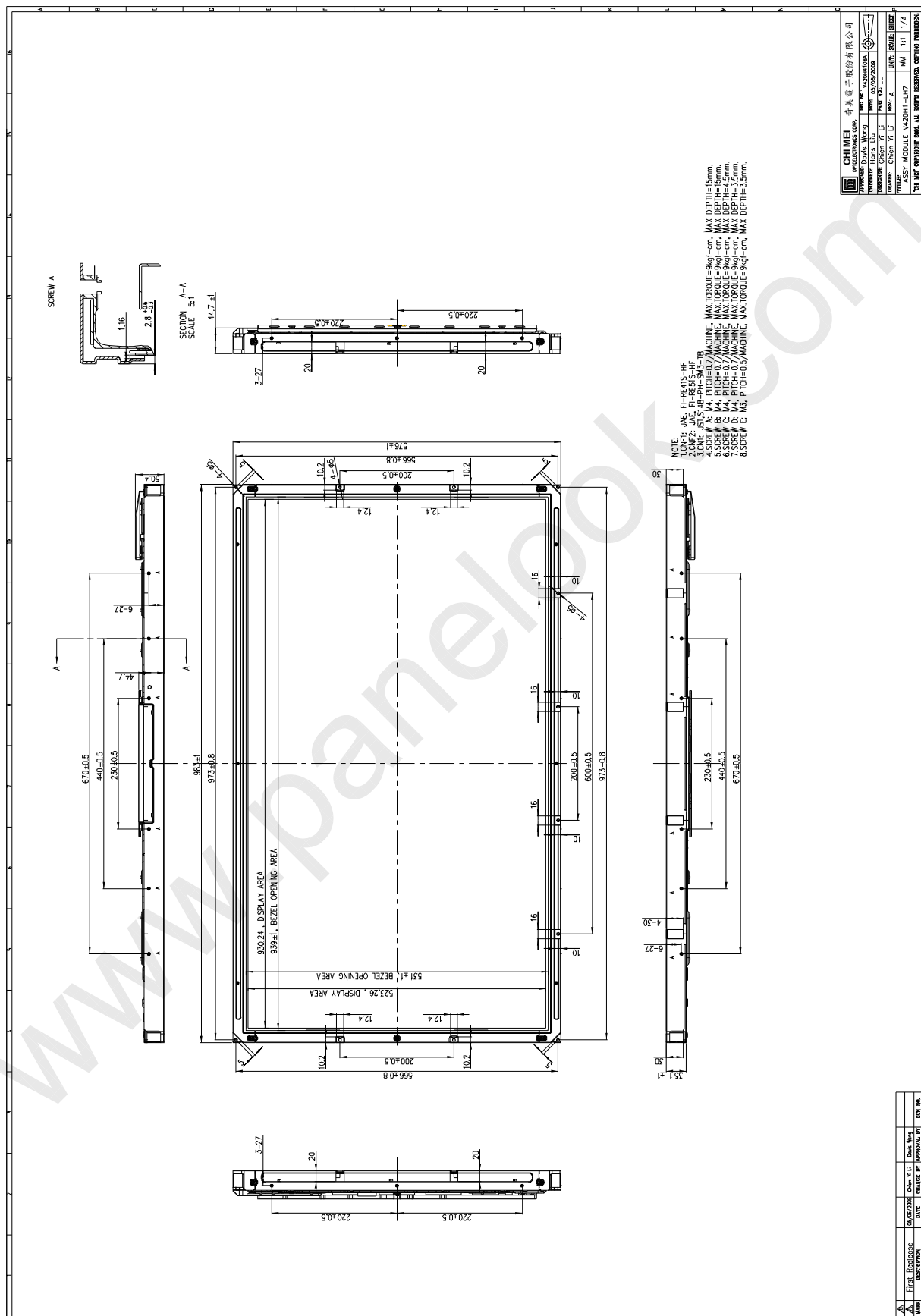
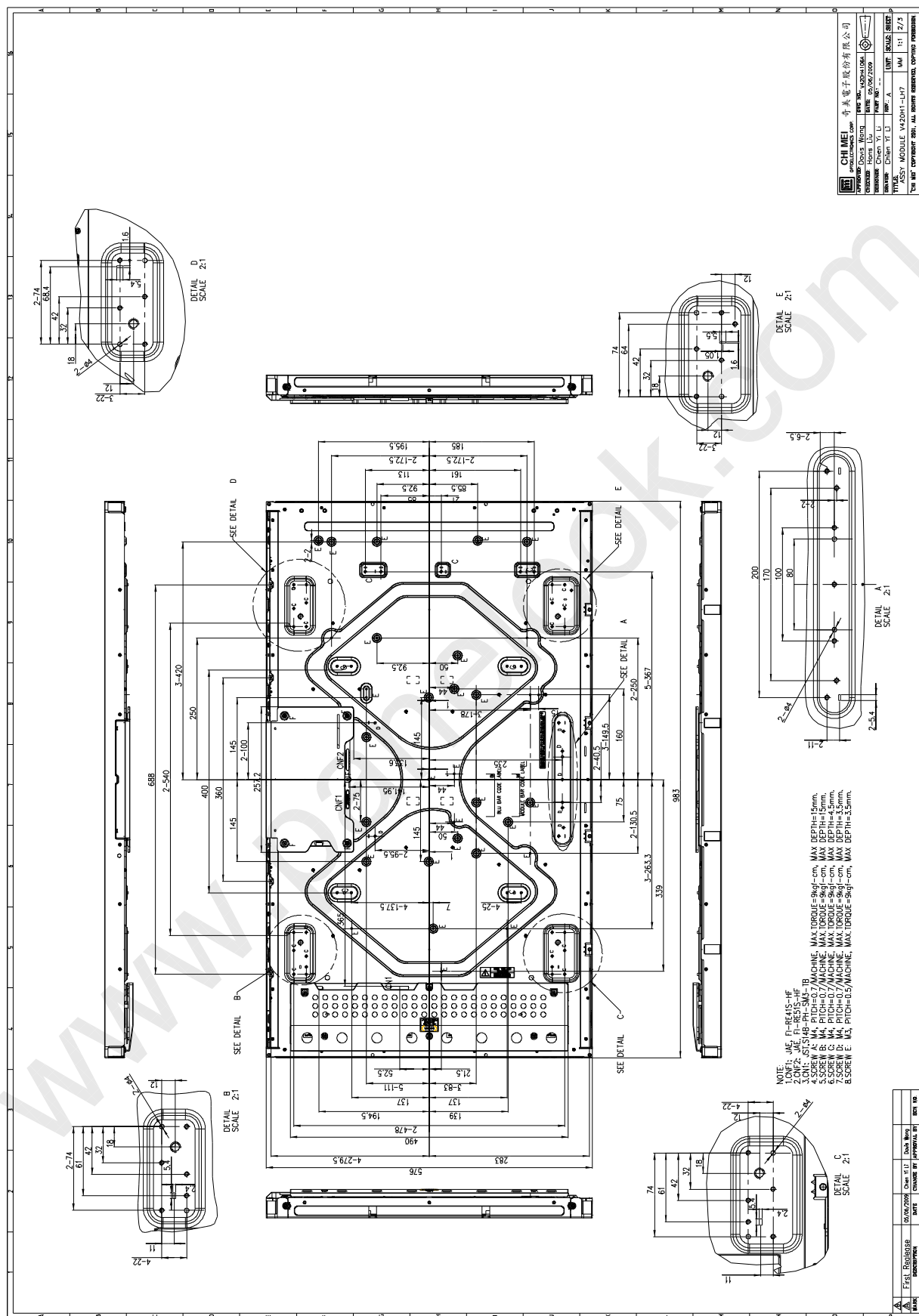
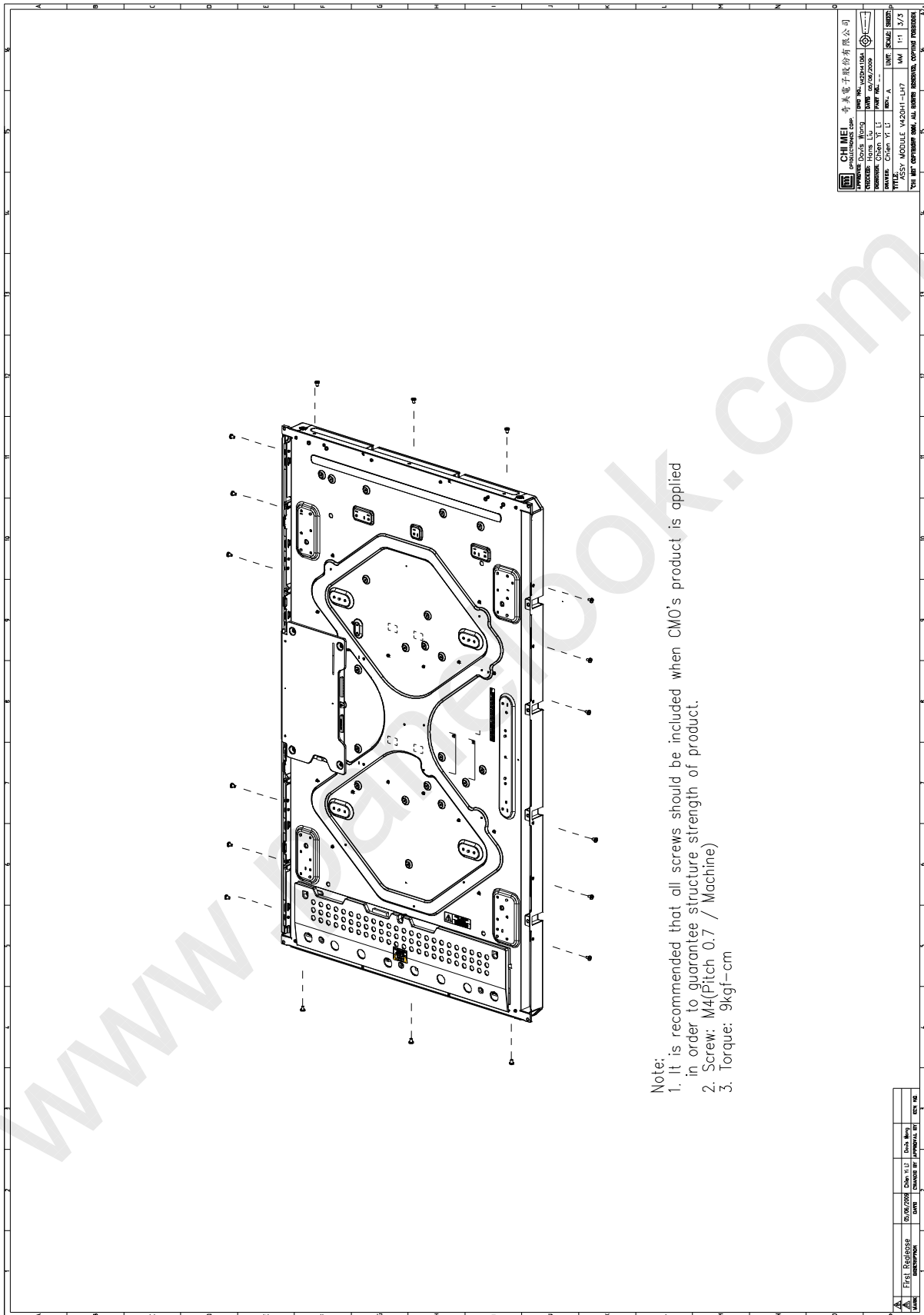


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTICS







CHI MEI OPTOELECTRONICS CORP.		奇美电子股份有限公司	
MODEL NO.	V420H1-LH7	REV.	1.1
DATE	2009.06.01	DATE	2009.06.01
DESIGNER	CHEN, Y. L.	UNIT	MODULE DESIGN
CHECKER	CHEN, Y. L.	DATE	2009.06.01
THIS IS A PRELIMINARY DRAWING. ALL DIMENSIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.			

Note:
1. It is recommended that all screws should be included when CMO's product is applied in order to guarantee structure strength of product.
2. Screw: M4(Pitch 0.7 / Machine)
3. Torque: 9kgf-cm

DATE	2009.06.01	BY	Y. L. CHEN
DATE	2009.06.01	BY	Y. L. CHEN
DATE	2009.06.01	BY	Y. L. CHEN