CHI MEI OPTOELECTRONICS CORP.

Issue Date:Aug.24.2009
Model No.: V420H1-PH5
Preliminary

TFT LCD Approval Specification

MODEL NO.: V420H1 – PH5

Customer: _____

Approved by:_____

Note:

Approved By	TV Head Division
	Chao-Chun Chung

Reviewed By	QA Dept.	Product Development Div.
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Prepared By	LCD TV Marketing and Product Management Div.	
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CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 0.0	Oct. 15, 2008	All	All	The tentative specification was first issued.
Ver. 1.0	Dec. 19, 2008	5 6 9 11 11-12 13 16-17 18-19 24 26 29 34-35 36-38	1.2 1.5 3.1 3.2.1 3.2.2 3.2.3 5.1 5.3 6.1 6.2 7.2 10 11	Revised fast response time Revised weight Updated TFT LCD module parameter Updated Lamp specification Updated BL electrical specification Updated inverter interface characteristics Updated TFT LCD module input Updated inverter unit Updated input signal timing specifications Updated Power ON/OFF sequence Updated optical specifications Updated packing Updated mechanical characteristics
Ver. 1.0	Dec. 23, 2008	18	5.3	Updated inverter pin 12 define
Ver. 1.0	Dec. 24, 2008	5 29-31	1.1 7.2	Modified “8-bit + FRC” to “10-bit” Updated Center Luminance of White spec
Ver. 1.1	Dec. 31, 2008	13 14 17	3.2.3 3.2.3 5.1	Add note(4) Updated power sequence and control signal timing fig. Updated pin define
Ver. 2.0	Feb. 12. 2009	11 16 17-19 29 30 35 35 37-39	3.2.1 3.2.2 5.1 5.1 7.1 7.2 10.1 10.2 11	Updated BLU connector pin configure. Updated BLU connector pin configure. Updated TFT LCD Module Input Updated LVDS pin assignment. Updated optical measurement condition. Updated optical specification. Updated package specification. Updated package specification. Updated ME specification.
Ver. 2.1	Apr. 8, 2009	13 13 14 15 26 38	3.2.3 3.2.3 3.2.3 4.1 6.1 11	Modified Internal PWM Control Voltage Max. value Deleted Note 4 Modified the V_{IPWM} value Modified the Block Diagram of the BLU Modified Vertical Active Display Term and Horizontal Active Display Term Modified Mechanical Characteristics (Removed FFC)
Ver. 2.2	Apr. 18, 2009	11 13 14	3.2.2 3.2.3 3.2.3	Updated Max Values of Power Consumption Deleted Max Values of VBL Rising/Falling Time, PWM Delay Time, BLON Delay Time, and BLON Off Time Modified the V_{IPWM} value
Ver. 2.3	Apr. 23, 2009	13 25	3.2.3 6.1	Modified BLON Delay Time and BLON Off Time Updated Frame Rate
Ver. 2.4	Jun. 4, 2009	30	7.1	Modified Oscillating Frequency
Ver. 2.5	Aug. 6,2009	9-11 16 17-19 28 40-47 35-36	3.1 4.1 5.1 6.2 Appendix 10	TFT LCD MODULE TFT LCD MODULE TFT LCD Module Input POWER ON/OFF SEQUENCE Add Appendix PACKAGING

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420H1-PH5 is a 42" TFT Liquid Crystal Display module with driver ICs and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 1.07G colors (10-bit/color). The backlight unit is not built-in.

1.2 FEATURES

- High contrast ratio (4000:1)
- Fast response time (Gray to gray average 4.0 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate with MEMC
- Ultra wide viewing angle : Super MVA technology
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.24(H) x 523.26 (V) (42.02" diagonal)	mm	(1)
Bezel Opening Area	937.24 (H) x 530.26 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 11%) Hard coating (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

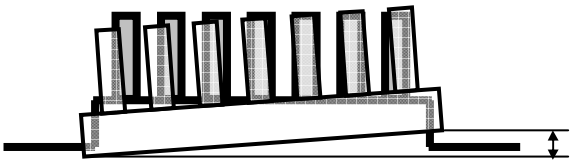
Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	2100	2150	2200	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT(BASE ON CMO MODULE V420H1-LH5)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

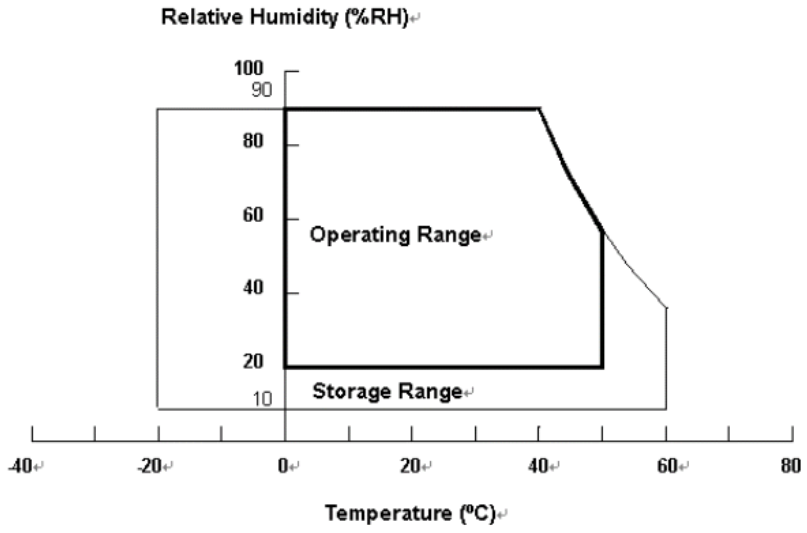
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Storage condition: With shipping package.

Storage temperature rang: 25±5℃

Storage humidity range: 50±10%RH

Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{AA}	-0.5	+18	V	(1)
Power Supply Voltage	V_{GH}	-0.3	+32.3	V	
Power Supply Voltage	V_{GL}	-5.7	-0.3	V	
Logic Input Voltage	V_{DD}	-0.3	3.4	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{GH}	31	32	33	V	
		V_{GL}	-5.8	-5.5	-5.2	V	
		V_{AA}	15.9	16.2	16.5	V	
		V_{DD}	3.2	3.3	3.4	V	
		V_{REF}	15.17	15.47	15.77	V	
Power Supply Current		I_{GH}	-	31.49	40.3	mA	
		I_{GL}	-	7.73	10.79	mA	
		I_{AA}	-	627	890.5	mA	
		I_{DD}		1.41	1.84	A	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

3.2 RSDS CHARACTERISTICS

VDDD=3.0 to 3.6V, VDDA=13.5 to 18.0V, VSSD=VSSA=0V, Ta = -20~+85 ºC

Item	Symbol	Condition	Value			Unit
			Min	Typ	Max	
RSDS high input Voltage	$V_{DIFFRSDS}$	V_{CMRSDS} = +1.2 V (1)	100	200	600	mV
RSDS low input Voltage	$V_{DIFFRSDS}$	V_{CMRSDS} = +1.2 V (1)	-600	-200	-100	
RSDS common mode input voltage range	V_{CMRSDS}	$V_{DIFFRSDS}$ = 200 mV (2)	VSSD+0.5	Note(3)	VDDD-1.2	V
RSDS Input leakage current	I_{DL}	A/BDxxP, A/BDxxN, A/BCLKP, A/BCLKN	-10	-	10	μA

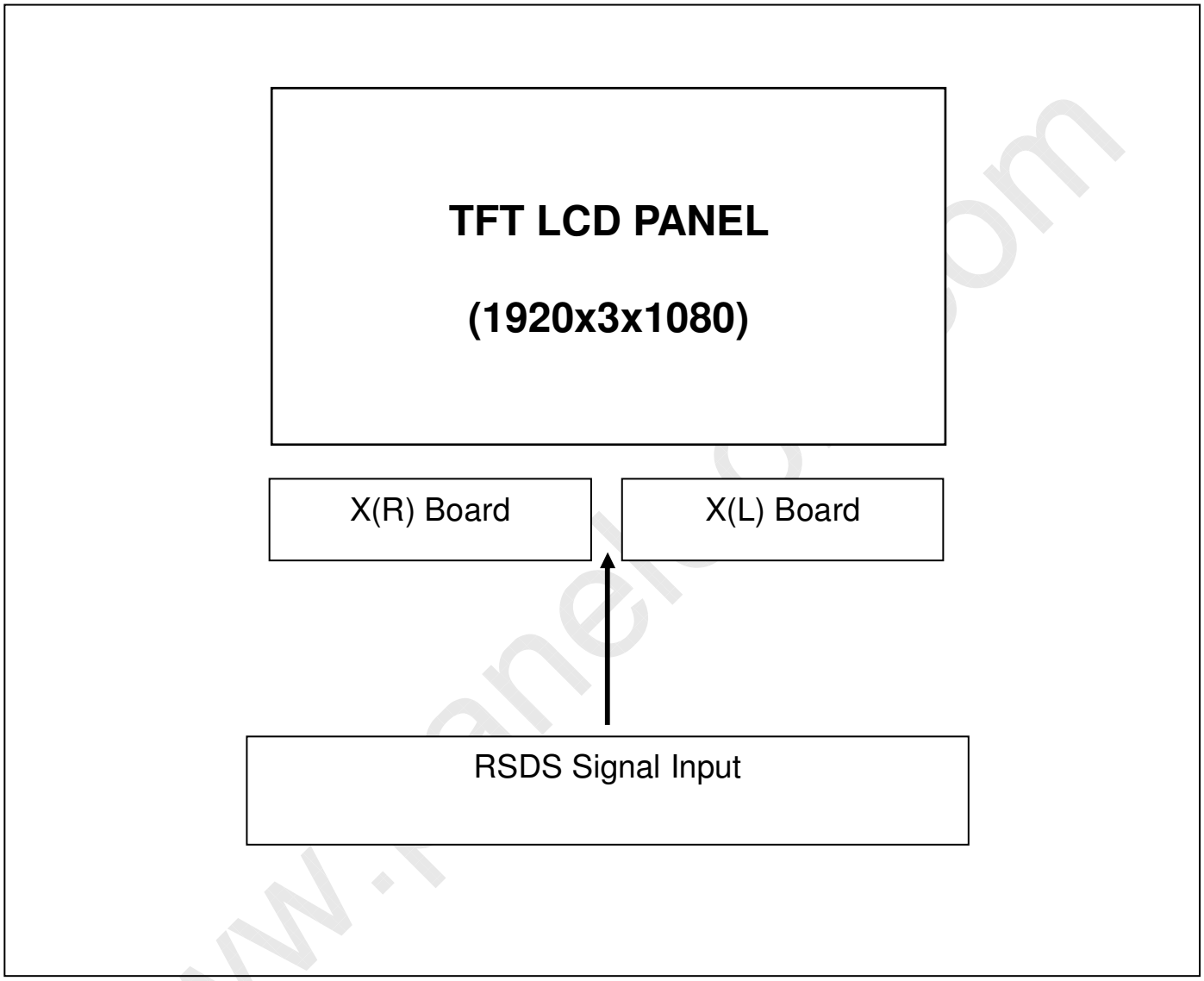
Note (1) V_{CMRSDS} = (VCLKP + VCLKN)/2 or V_{CMRSDS} = ($VD_{XX}P$ + $VD_{XX}N$)/2

Note (2) $V_{DIFFRSDS}$ = VCLKP - VCLKN or $V_{DIFFRSDS}$ = $VD_{XX}P$ - $VD_{XX}N$

Note (3) V_{CMRSDS} = 1.2V(VDDD = 3.3V)

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD OPEN CELL



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNX1(XL) Connector Pin Assignment

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	41	GM6	Gamma Power supply
2	NC	No connection	42	GM5	Gamma Power supply
3	NC	No connection	43	GM4	Gamma Power supply
4	NC	No connection	44	GM3	Gamma Power supply
5	NC	No connection	45	GM2	Gamma Power supply
6	TP1	RSDS data latch	46	GM1	Gamma Power supply
7	NC	No connection	47	GND	Ground
8	CKV	Scan driver clock	48	VCM	VCM Power supply
9	STV	Scan driver start pulse	49	VCM	VCM Power supply
10	OE1	Scan driver output1 enable	50	VAA	Driver Power supply
11	OE2	Scan driver output2 enable	51	VAA	Driver Power supply
12	NC	No connection	52	VGL	Driver Power supply
13	V33L	Logic Power supply	53	NC	No connection
14	V33L	Logic Power supply	54	VGH	Driver Power supply
15	NC	No connection	55	GND	Ground
16	NC	No connection			
17	NC	No connection			
18	NC	No connection			
19	GND	Ground			
20	VCS	Charge sharing trace			
21	VCS	Charge sharing trace			
22	VCS	Charge sharing trace			
23	VCS	Charge sharing trace			
24	VCS	Charge sharing trace			
25	VCS	Charge sharing trace			
26	GND	Ground			
27	GM20	Gamma Power supply			
28	GM19	Gamma Power supply			
29	GM18	Gamma Power supply			
30	GM17	Gamma Power supply			
31	GM16	Gamma Power supply			
32	GM15	Gamma Power supply			
33	GM14	Gamma Power supply			
34	GM13	Gamma Power supply			
35	GM12	Gamma Power supply			
36	GM11	Gamma Power supply			
37	GM10	Gamma Power supply			
38	GM9	Gamma Power supply			
39	GM8	Gamma Power supply			
40	GM7	Gamma Power supply			

CNX2(XL) Connector Pin Assignment

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	41	A_CLKP	A-Path Data driver clock
2	BD1P_6	B-Path RSDS data signal	42	A_CLKM	A-Path Data driver clock
3	BD1M_6	B-Path RSDS data signal	43	AD1P_2	A-Path RSDS data signal
4	BD0P_6	B-Path RSDS data signal	44	AD1M_2	A-Path RSDS data signal
5	BD0M_6	B-Path RSDS data signal	45	AD0P_2	A-Path RSDS data signal
6	AD1P_6	A-Path RSDS data signal	46	AD0M_2	A-Path RSDS data signal
7	AD1M_6	A-Path RSDS data signal	47	BD1P_1	B-Path RSDS data signal
8	AD0P_6	A-Path RSDS data signal	48	BD1M_1	B-Path RSDS data signal
9	AD0M_6	A-Path RSDS data signal	49	BD0P_1	B-Path RSDS data signal
10	BD1P_5	B-Path RSDS data signal	50	BD0M_1	B-Path RSDS data signal
11	BD1M_5	B-Path RSDS data signal	51	AD1P_1	A-Path RSDS data signal
12	BD0P_5	B-Path RSDS data signal	52	AD1M_1	A-Path RSDS data signal
13	BD0M_5	B-Path RSDS data signal	53	AD0P_1	A-Path RSDS data signal
14	AD1P_5	A-Path RSDS data signal	54	AD0M_1	A-Path RSDS data signal
15	AD1M_5	A-Path RSDS data signal	55	GND	Ground
16	AD0P_5	A-Path RSDS data signal			
17	AD0M_5	A-Path RSDS data signal			
18	BD1P_4	B-Path RSDS data signal			
19	BD1M_4	B-Path RSDS data signal			
20	BD1P_4	B-Path RSDS data signal			
21	BD0M_4	B-Path RSDS data signal			
22	BD0P_4	B-Path RSDS data signal			
23	AD1P_4	A-Path RSDS data signal			
24	AD1M_4	A-Path RSDS data signal			
25	AD0P_4	A-Path RSDS data signal			
26	AD0M_4	A-Path RSDS data signal			
27	BD1P_3	B-Path RSDS data signal			
28	BD1M_3	B-Path RSDS data signal			
29	BD0P_3	B-Path RSDS data signal			
30	BD0M_3	B-Path RSDS data signal			
31	AD1P_3	A-Path RSDS data signal			
32	AD1M_3	A-Path RSDS data signal			
33	AD0P_3	A-Path RSDS data signal			
34	GND	Ground			
35	B_CLKP	B-Path Data driver clock			
36	B_CLKM	B-Path Data driver clock			
37	BD1P_2	B-Path RSDS data signal			
38	BD1M_2	B-Path RSDS data signal			
39	BD0P_2	B-Path RSDS data signal			
40	BD0M_2	B-Path RSDS data signal			

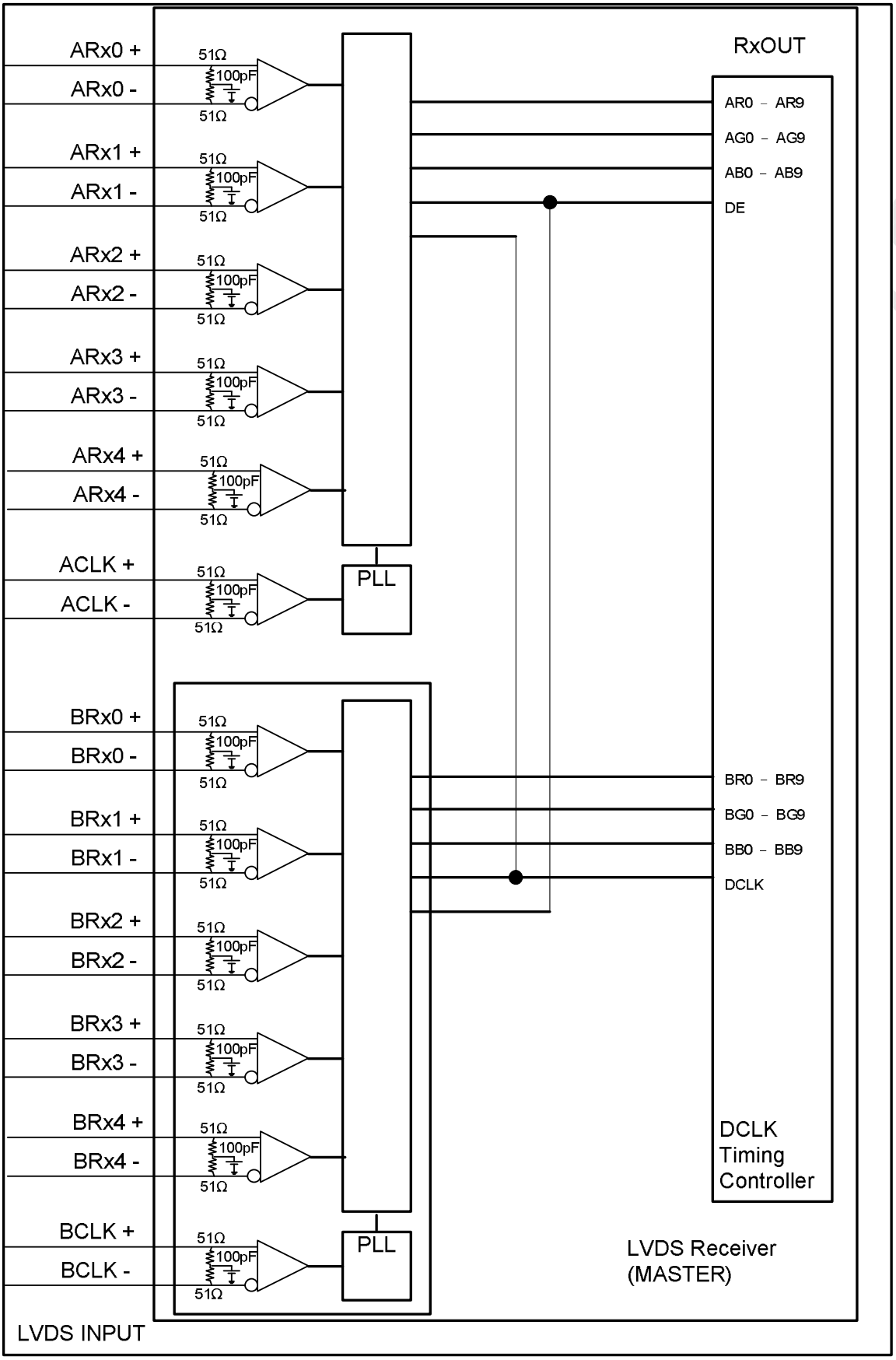
CNX3(XR) Connector Pin Assignment

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	41	C_CLKP	C-Path Data driver clock
2	BD1P_12	B-Path RSDS data signal	42	C_CLKM	C-Path Data driver clock
3	BD1M_12	B-Path RSDS data signal	43	AD1P_8	A-Path RSDS data signal
4	BD0P_12	B-Path RSDS data signal	44	AD1M_8	A-Path RSDS data signal
5	BD0M_12	B-Path RSDS data signal	45	AD0P_8	A-Path RSDS data signal
6	AD1P_12	A-Path RSDS data signal	46	AD0M_8	A-Path RSDS data signal
7	AD1M_12	A-Path RSDS data signal	47	BD1P_7	B-Path RSDS data signal
8	AD0P_12	A-Path RSDS data signal	48	BD1M_7	B-Path RSDS data signal
9	AD0M_12	A-Path RSDS data signal	49	BD0P_7	B-Path RSDS data signal
10	BD1P_11	B-Path RSDS data signal	50	BD0M_7	B-Path RSDS data signal
11	BD1M_11	B-Path RSDS data signal	51	AD1P_7	A-Path RSDS data signal
12	BD0P_11	B-Path RSDS data signal	52	AD1M_7	A-Path RSDS data signal
13	BD0M_11	B-Path RSDS data signal	53	AD0P_7	A-Path RSDS data signal
14	AD1P_11	A-Path RSDS data signal	54	AD0M_7	A-Path RSDS data signal
15	AD1M_11	A-Path RSDS data signal	55	GND	Ground
16	AD0P_11	A-Path RSDS data signal			
17	AD0M_11	A-Path RSDS data signal			
18	BD1P_11	B-Path RSDS data signal			
19	BD1M_11	B-Path RSDS data signal			
20	BD0P_10	B-Path RSDS data signal			
21	BD0M_10	B-Path RSDS data signal			
22	AD1P_10	A-Path RSDS data signal			
23	AD1M_10	A-Path RSDS data signal			
24	AD0P_10	A-Path RSDS data signal			
25	AD1M_10	A-Path RSDS data signal			
26	BD1P_9	B-Path RSDS data signal			
27	BD1M_9	B-Path RSDS data signal			
28	BD0P_9	B-Path RSDS data signal			
29	BD0M_9	B-Path RSDS data signal			
30	AD1P_9	A-Path RSDS data signal			
31	AD1M_9	A-Path RSDS data signal			
32	AD0P_9	A-Path RSDS data signal			
33	AD0M_9	A-Path RSDS data signal			
34	GND	Ground			
35	D_CLKP	D-Path Data driver clock			
36	D_CLKM	D-Path Data driver clock			
37	BD1P_8	B-Path RSDS data signal			
38	BD1M_8	B-Path RSDS data signal			
39	BD0P_8	B-Path RSDS data signal			
40	BD0M_8	B-Path RSDS data signal			

CNX4(XR) Connector Pin Assignment

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	41	NC	No connection
2	VSCM	VSCM Power supply	42	NC	No connection
3	VGH	Driver Power supply	43	NC	No connection
4	NC	No connection	44	NC	No connection
5	VGL	Driver Power supply	45	NC	No connection
6	VAA	Driver Power supply	46	NC	No connection
7	VAA	Driver Power supply	47	NC	No connection
8	VCM	VCM Power supply	48	NC	No connection
9	VCM	VCM Power supply	49	OE2_R	Scan driver output2 enable
10	GND	Ground	50	OE1R	Scan driver output1 enable
11	GM1	Gamma Power supply	51	STV	Scan driver start pulse
12	GM2	Gamma Power supply	52	CKV	Scan driver clock
13	GM3	Gamma Power supply	53	NC	No connection
14	GM4	Gamma Power supply	54	TP1	RSDS data latch
15	GM5	Gamma Power supply	55	GND	Ground
16	GM6	Gamma Power supply			
17	GM7	Gamma Power supply			
18	GM8	Gamma Power supply			
19	GM9	Gamma Power supply			
20	GM10	Gamma Power supply			
21	GM11	Gamma Power supply			
22	GM12	Gamma Power supply			
23	GM13	Gamma Power supply			
24	GM14	Gamma Power supply			
25	GM15	Gamma Power supply			
26	GM16	Gamma Power supply			
27	GM17	Gamma Power supply			
28	GM18	Gamma Power supply			
29	GM19	Gamma Power supply			
30	GM20	Gamma Power supply			
31	GND	Ground			
32	VCS	Charge sharing trace			
33	VCS	Charge sharing trace			
34	VCS	Charge sharing trace			
35	VCS	Charge sharing trace			
36	VCS	Charge sharing trace			
37	VCS	Charge sharing trace			
38	V33R	Logic Power supply			
39	V33R	Logic Power supply			
40	NC	No connection			

5.2 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

Notes (1) The system must have the transmitter to drive the module.

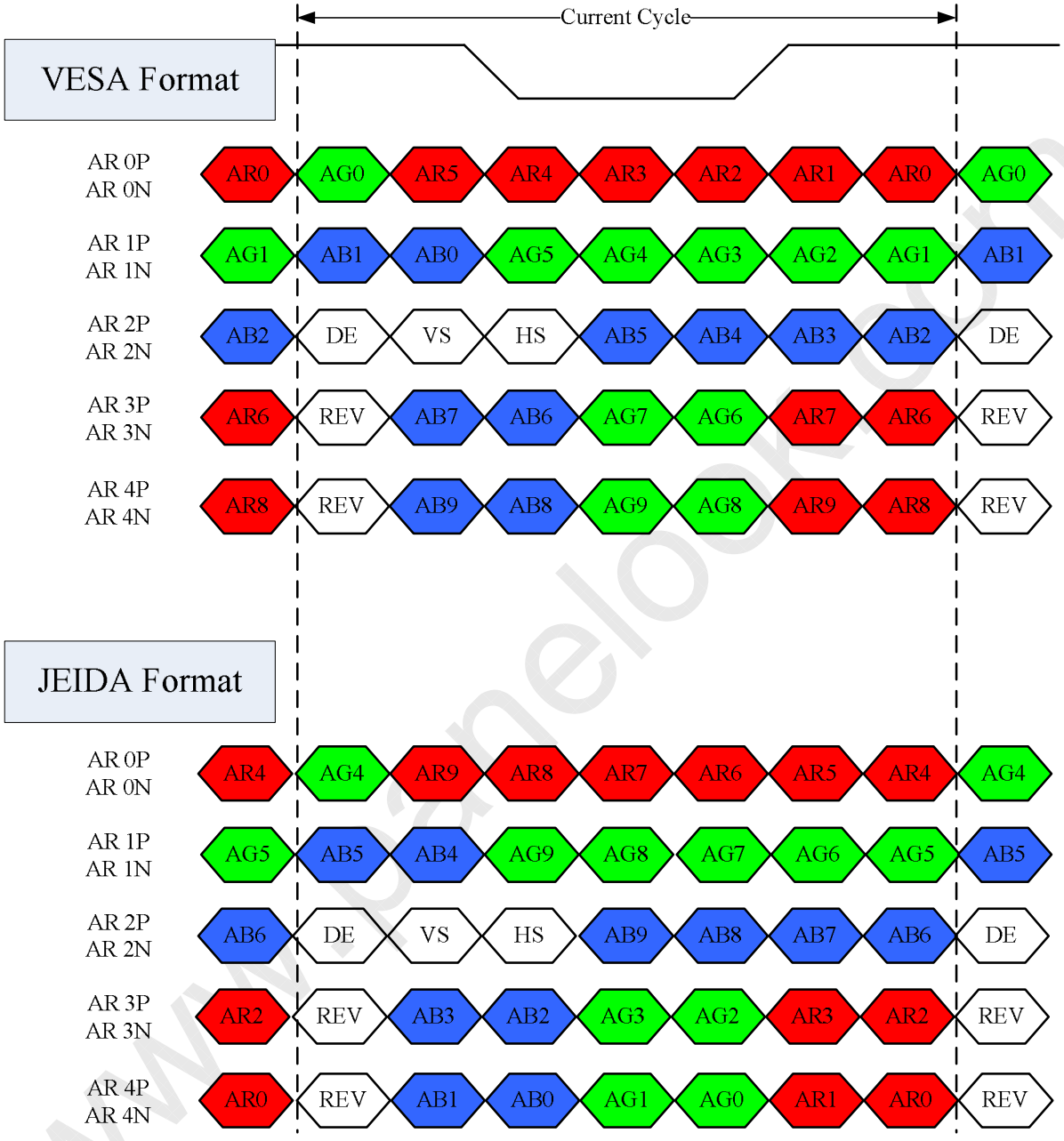
Notes (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Notes (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.3 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

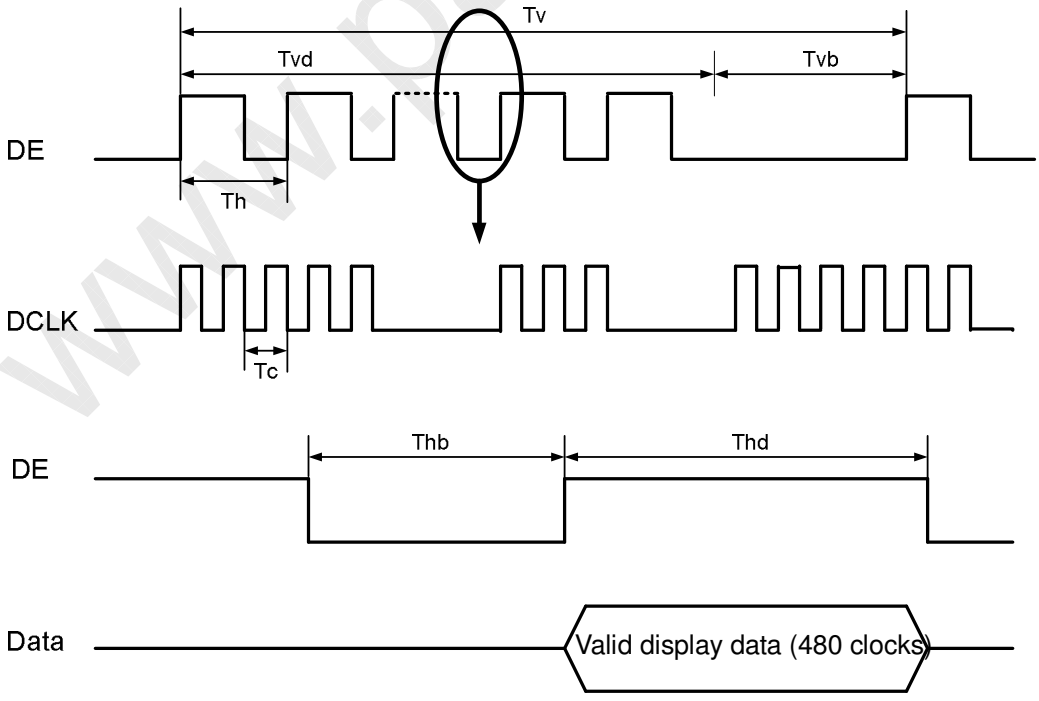
(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

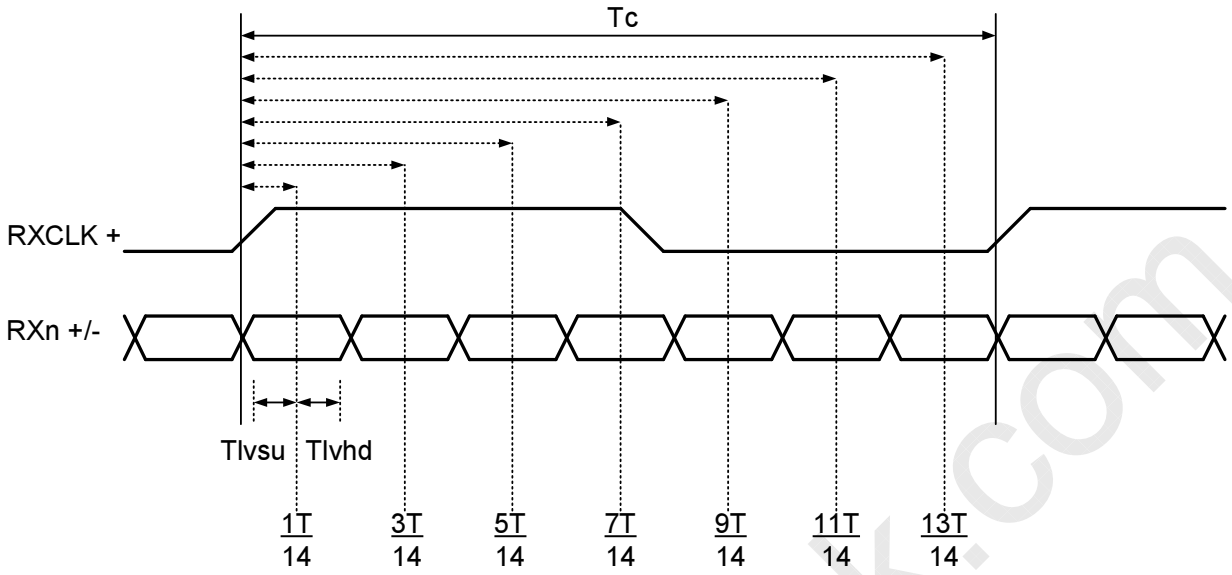
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	78	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate		-	120	-	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	525	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	45	70	95	Tc	-

Note : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



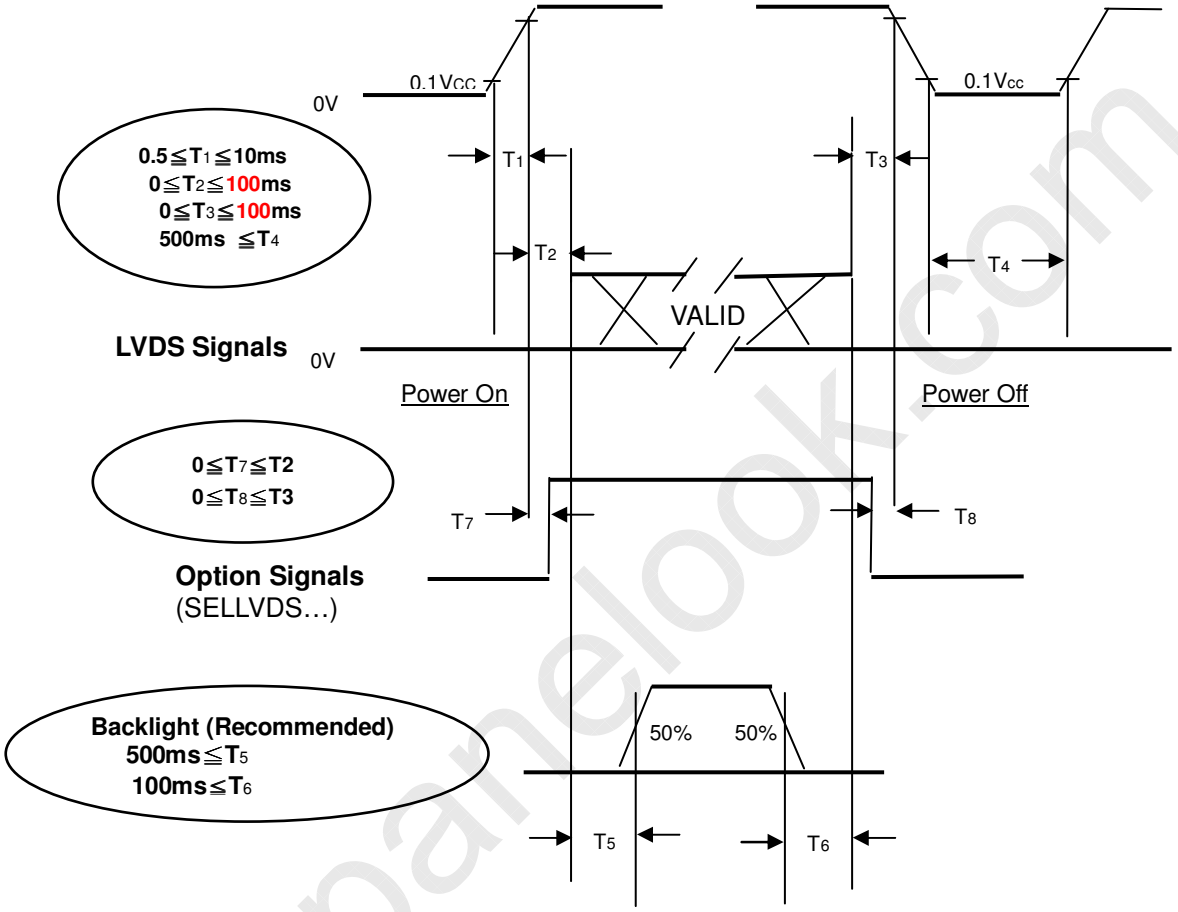
LVDS INPUT INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note.

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failures.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

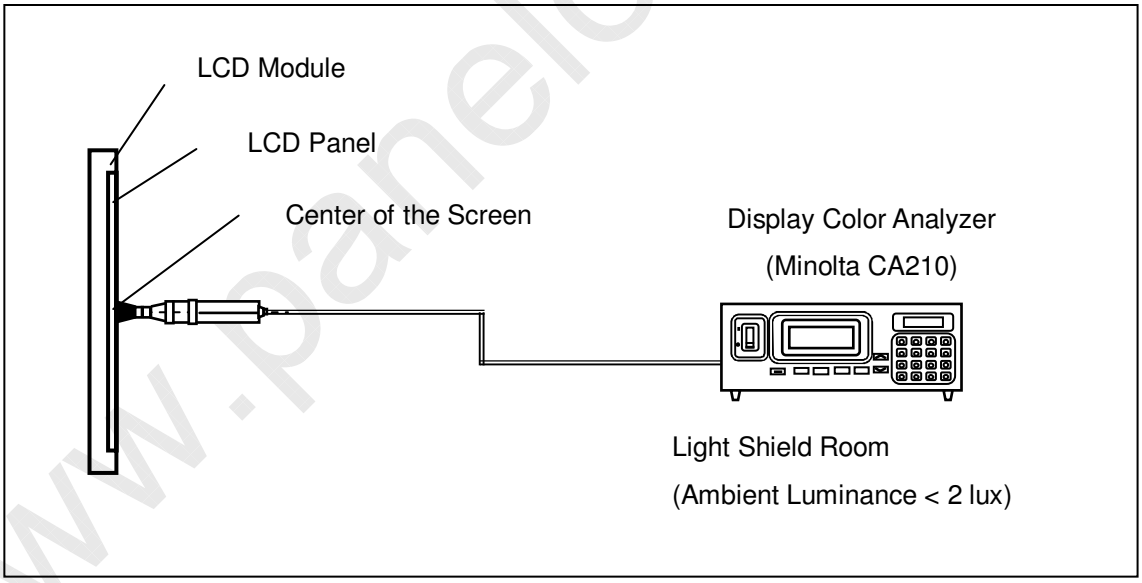
(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	8.7/10.2	mA
Oscillating Frequency (Inverter)	FW	42±3	KHz
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement (CS-1000 or CA-210 calibrated by CS-1000) should be executed after lighting backlight for 1 hour in a windless room.



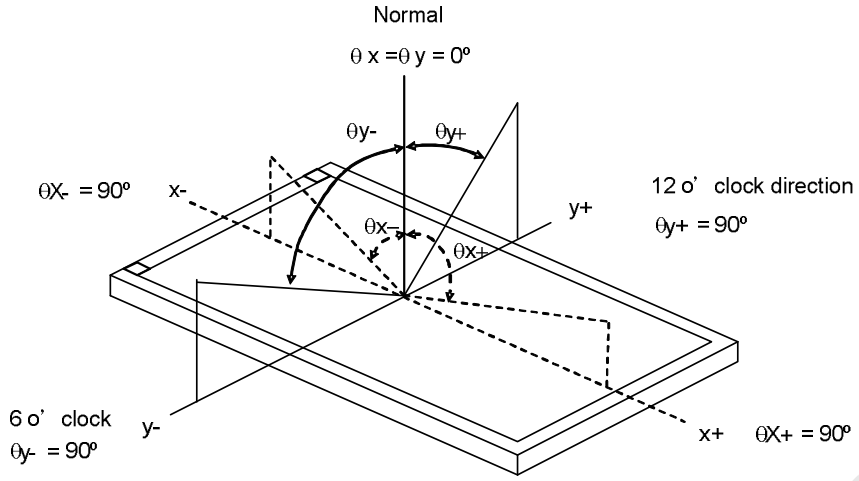
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	3000	4000	-	-	Note (2)
Response Time		Gray to gray		-	4.0	8.0	ms	Note (3)
Center Luminance of White	Noraml mode	LC		400	500	-	cd/m^2	Note (4)
	ECO mode	LC		350	450	-	cd/m^2	Note (4), (7)
White Variation		δW		-	-	1.3	-	Note (6)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.649	Typ. +0.03	-	-
		Ry			0.334		-	
	Green	Gx			0.267		-	
		Gy			0.610		-	
	Blue	Bx			0.149		-	
		By			0.060		-	
	White	Wx			0.280		-	
		Wy			0.285		-	
	Color Gamut	C.G		-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	Note (1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

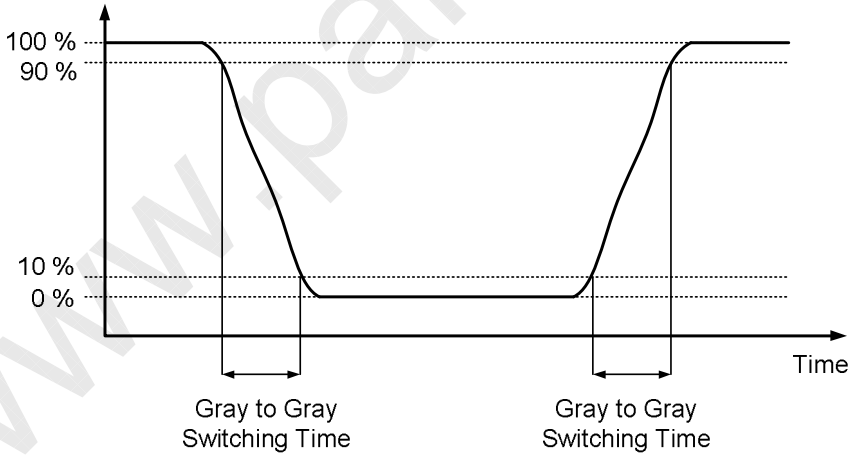
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:

Optical Response



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892, 1023 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 1023 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

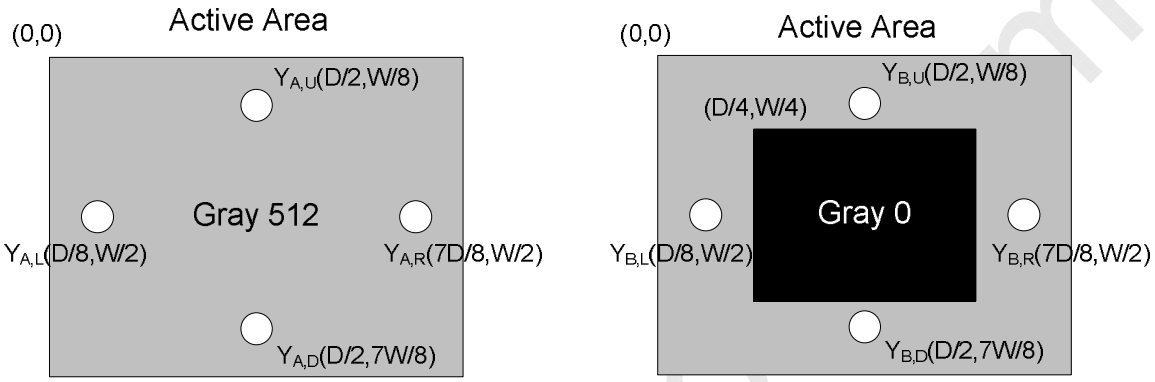
Note (5) Definition of Cross Talk (CT):

CT = | YB – YA | / YA × 100 (%)

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

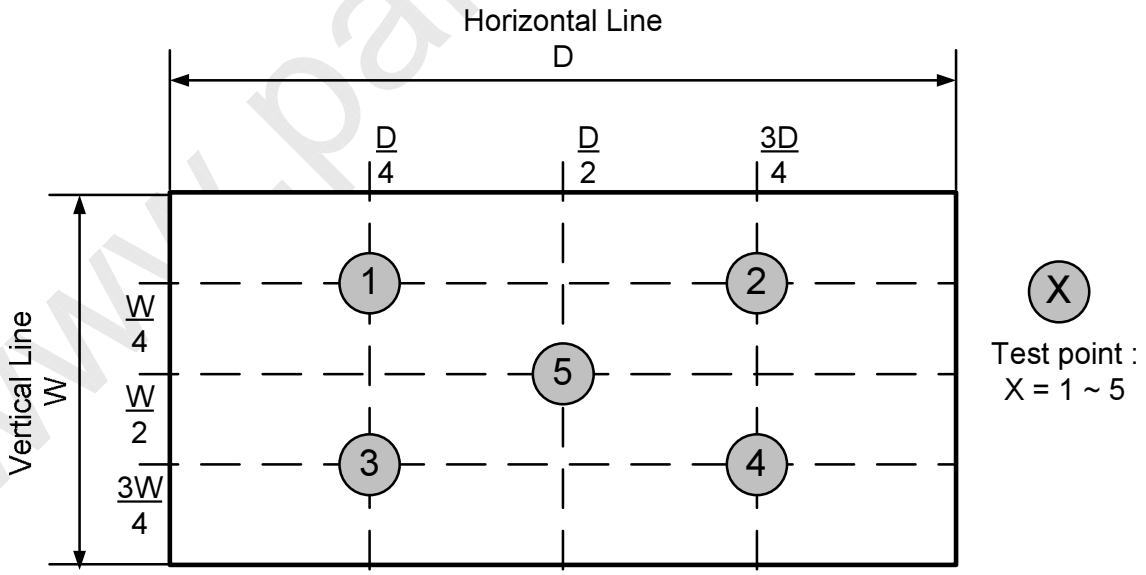
YB = Luminance of measured location with gray level 0 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



Note (7) ECO mode:

ECO mode was selected by inverter pin: A_DIM.

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

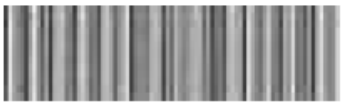
[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMO internal control.

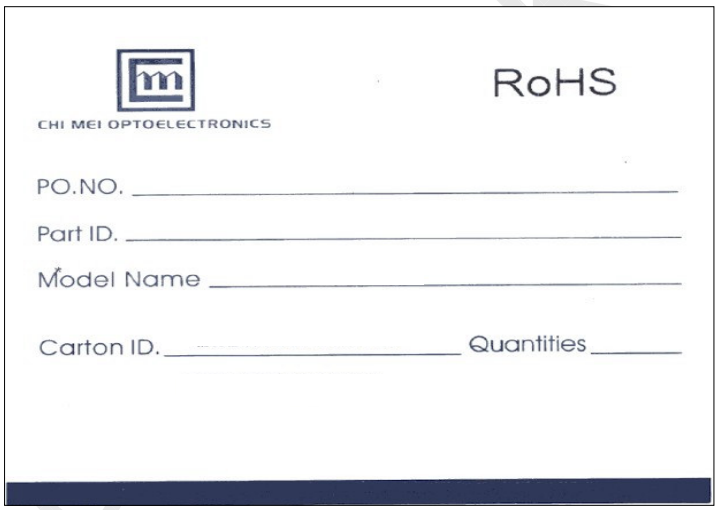
V420H1-PH5



XXXXXXXXXXXXX

9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.



(a) Model Name: V420H1-PH5

(b) Carton ID: CMO internal control

(c) Quantities: 9 pcs

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 9PCS LCD TV Panels / 1 Box

(2) Box dimensions : 1225 (L) X 801 (W) X 234 (H)

(3) Weight : approximately 32.2 Kg

10.2 PACKING METHOD

Figures 10-1 and 10-2 are the packing method

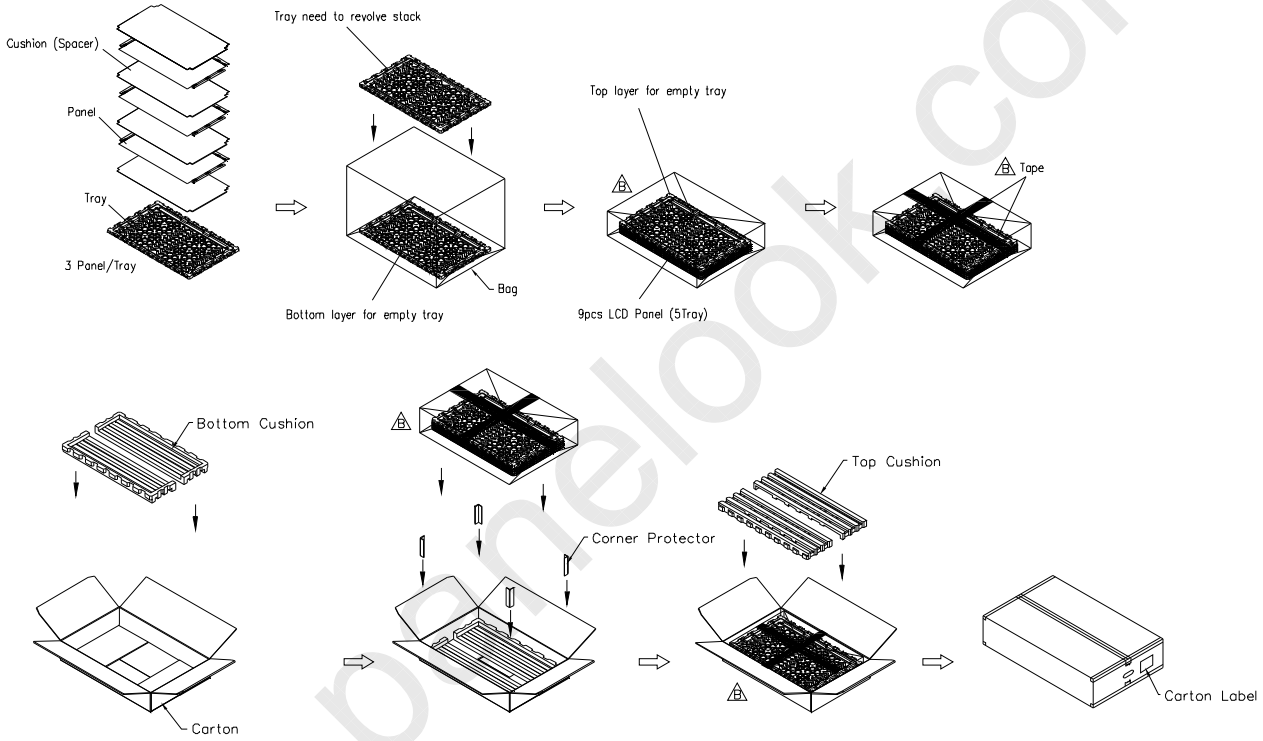
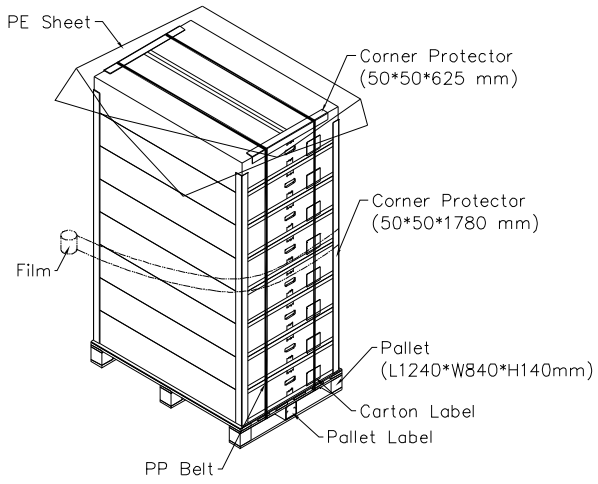


Figure.10-1 packing method

Sea & Land Transportation



Air Transportation

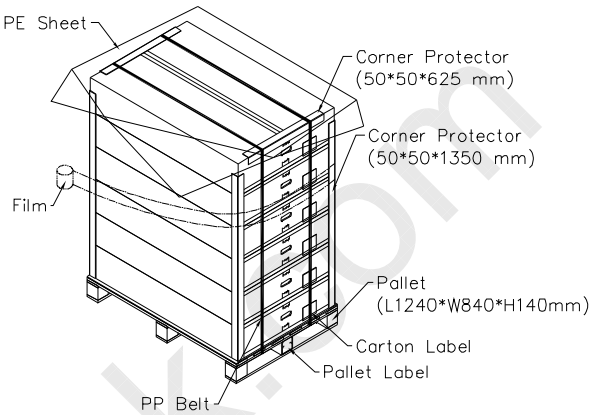
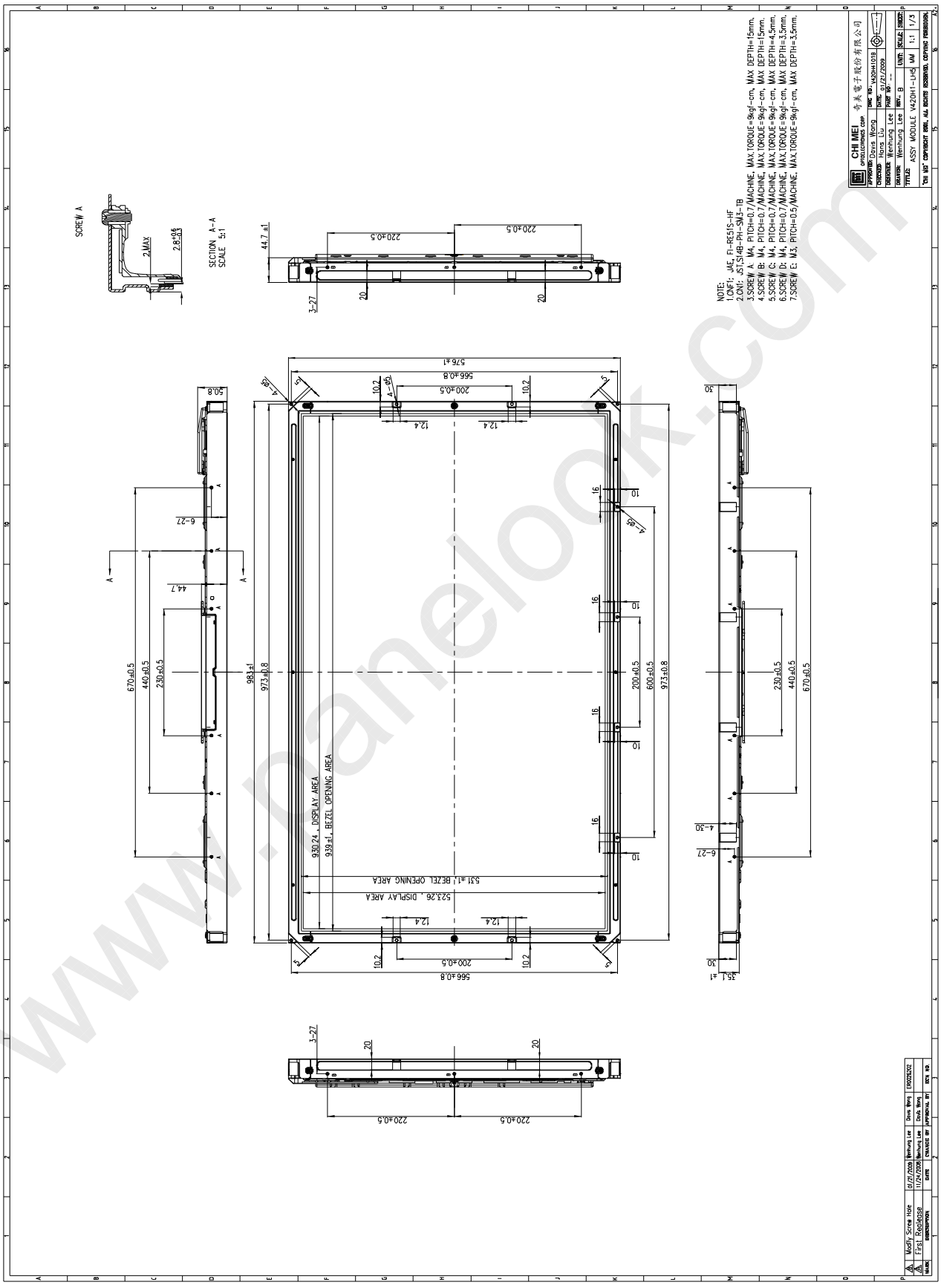
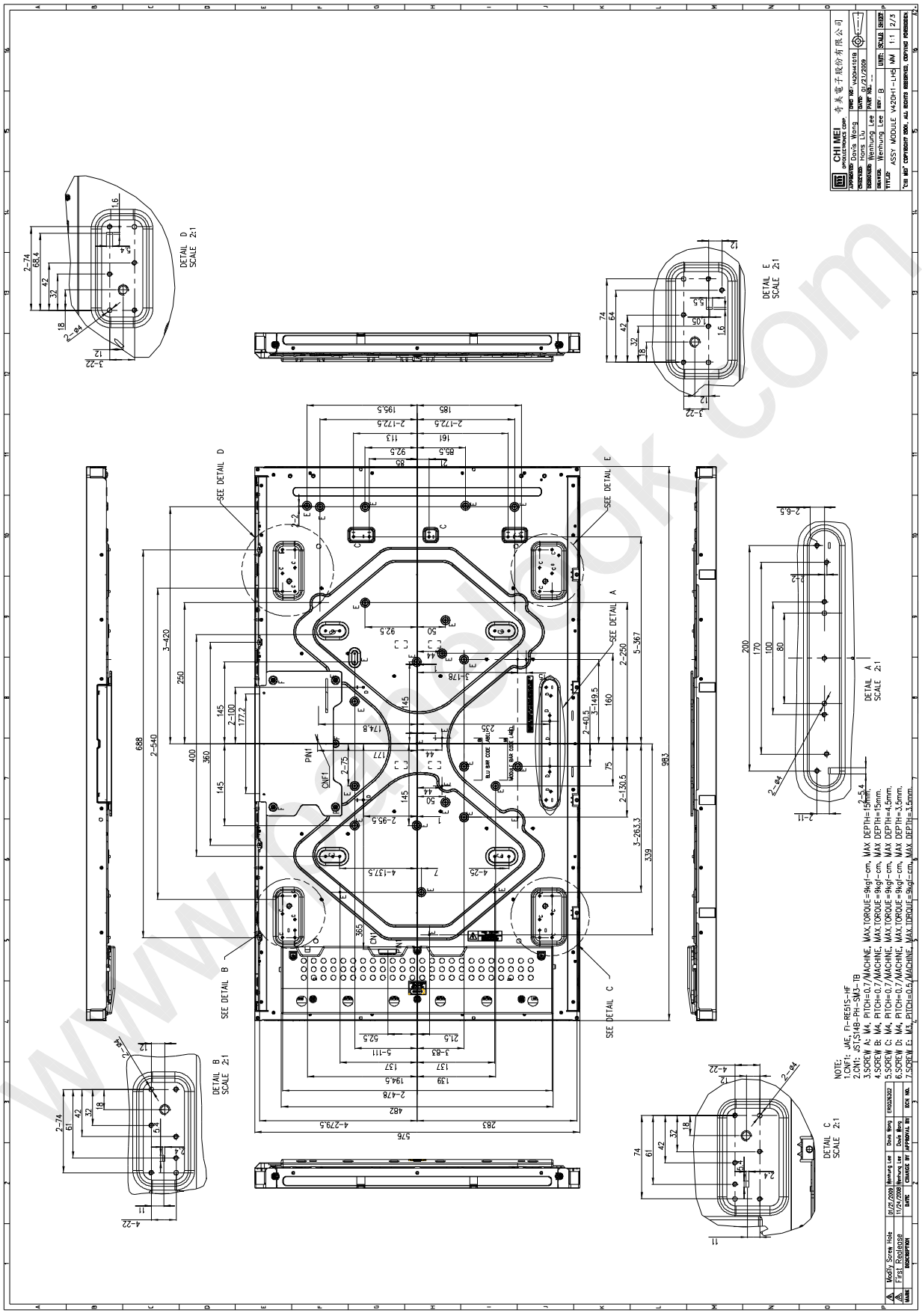
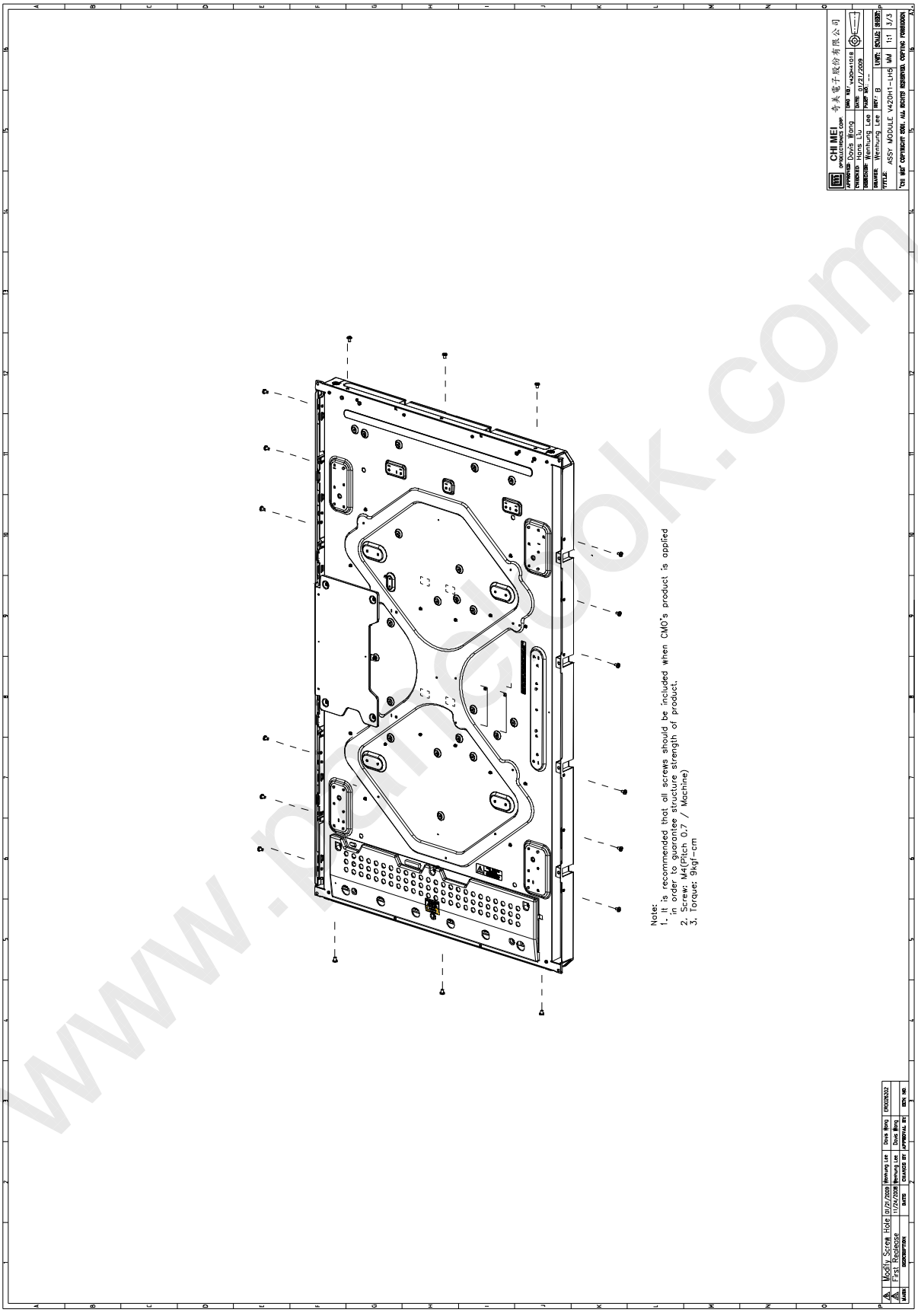


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTICS







Appendix – TWO Wire BUS INTRODUCTION

A.1 PIN ASSIGNMENT

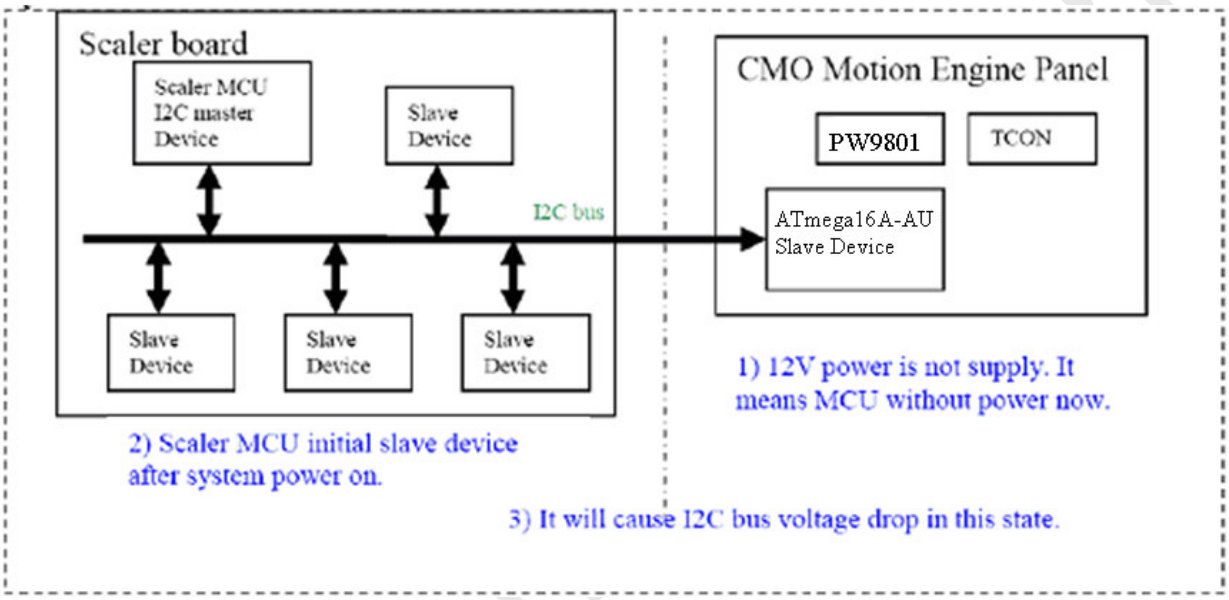
51pins LVDS connector

Pin8: SCL

Pin9: SDA

A.2 I2C BUS APPLICATION NOTE

I2C bus: (The I2C bus must for MEMC only or prevent the I2C bus voltage drop down in initial state)



A.3 TWO WIRE BUS DEVICE ADDRESS

Two wire device address: default is 0x40, 1 byte

Two wire command: the range is 0x00 to 0xFF, 1 byte, see the two wire command table.

Two wire bus format:

Device Address : 0x40 default							
D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	W/R

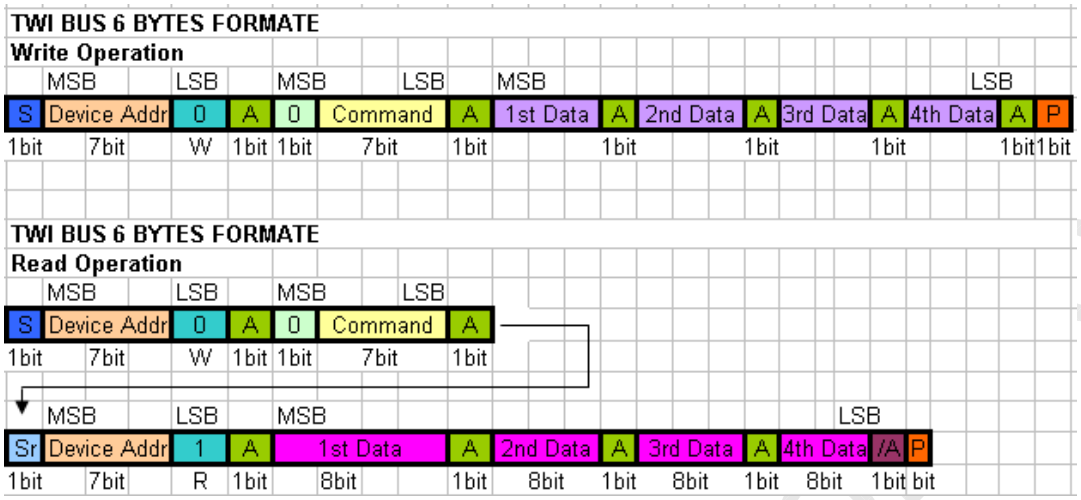
Command							
D7	D6	D5	D4	D3	D2	D1	D0
L	x	x	x	x	x	x	x

W/R	write : 0; Read : 1
L	1 : 1Byte Data Length; 0: 4Byte Data Length
S	TWI-Bus Start condition from master
Sr	TWI-Bus Start condition from master
A	TWI-Bus Acknowledge bit from master
/A	TWI-Bus Not Acknowledge bit from salve
P	TWI-Bus Stop condition from master
Data	TWI Bus Data from master
Data	TWI Bus Data from salve

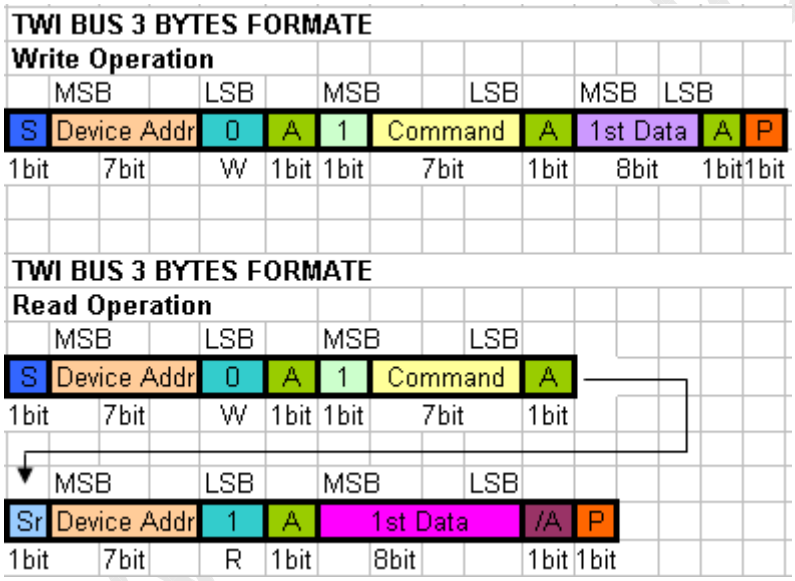
A.4 TWO WAY TO CONTROL THE TWO WIRE BUS

There are two options to control the two wires bus command.

Two wire bus 6 bytes format



Two wire bus 3 bytes format



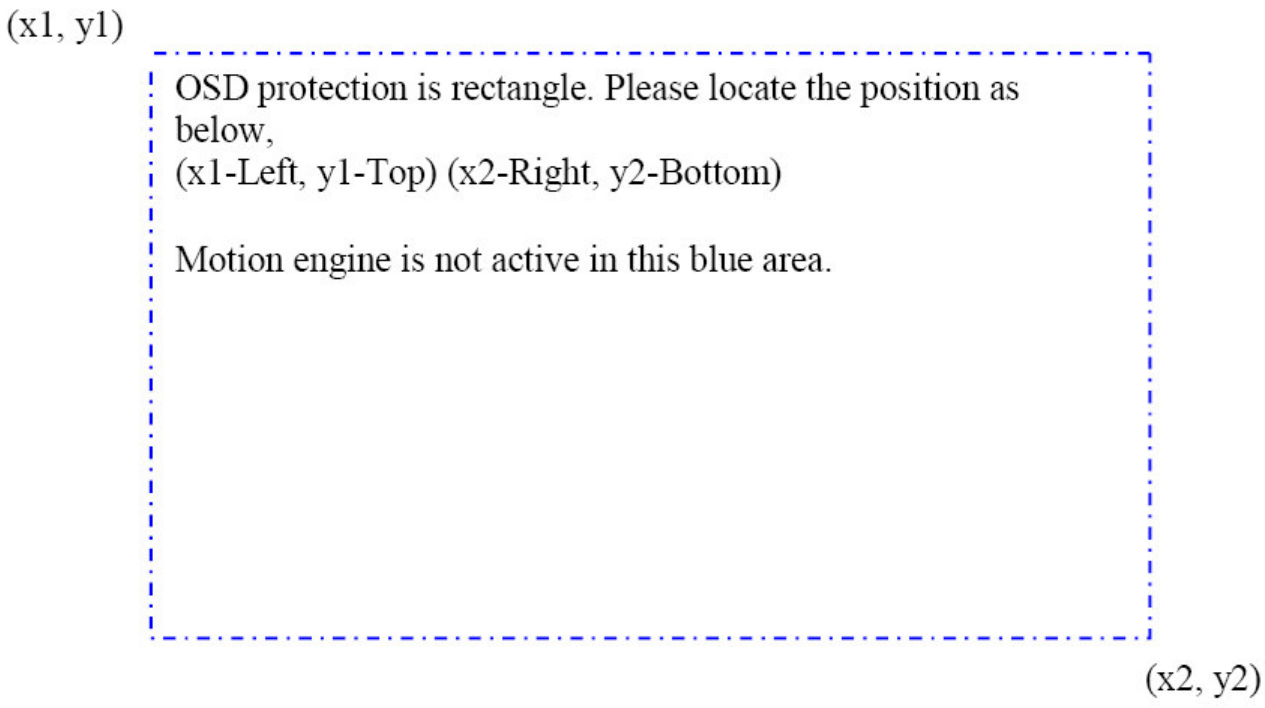
Note:

A transmission basically consists of a START condition, a SLA+R/W, one or more data packets and a STOP condition. An empty message, consisting of a START followed by a STOP condition, is illegal. Note that the wired-ANDing of the SCL line can be used to implement handshaking between the master and the slave. The slave can extend the SCL low period by pulling the SCL line low. This is useful if the clock speed set up by the master is too fast for the slave, or the slave needs extra time for processing between the data transmissions. The slave extending the SCL low period will not affect the SCL high period, which is determined by the master. As a consequence, the slave can reduce the TWI data transfer speed by prolonging the SCL duty cycle.

A.5 TWO WIRE BUS COMMAND TABLE

There is two wire bus command table.

Command Name		Access Mode	Description
All OSD Protection	0x00	R/W	OSDx Enable Flag Contorl
OSD1_Start_Protection	0x01	R/W	OSD1 Protection Start Position
OSD2_Start_Protection	0x02	R/W	OSD2 Protection Start Position
OSD3_Start_Protection	0x03	R/W	OSD3 Protection Start Position
OSD4_Start_Protection	0x04	R/W	OSD4 Protection Start Position
OSD1_End_Protection	0x05	R/W	OSD1 Protection End Position
OSD2_End_Protection	0x06	R/W	OSD2 Protection End Position
OSD3_End_Protection	0x07	R/W	OSD3 Protection End Position
OSD4_End_Protection	0x08	R/W	OSD4 Protection End Position
Demo Window	0x09	R/W	ME Performance Demo
MEMC Level	0x0A	R/W	ME Performance
GV Mode	0x0B	R/W	ME Operation
Blanking	0x0C	R/W	Blinking the screen



Enable All OSD Protection

AllOSD Protection : 0x00										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D28	Unused
	Unused				OSDx				D27	OSD4 flag 1 : On ; 0 : Off
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D26	OSD3 flag 1 : On ; 0 : Off
	Unused								D25	OSD2 flag 1 : On ; 0 : Off
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8	D24	OSD1 flag 1 : On ; 0 : Off
	Unused								D23~D0	Unused
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused									

AllOSD Protection : 0x80										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D4	Unused
	Unused				OSDx				D3	OSD4 flag 1 : On ; 0 : Off
									D2	OSD3 flag 1 : On ; 0 : Off
									D1	OSD2 flag 1 : On ; 0 : Off
									D0	OSD1 flag 1 : On ; 0 : Off

OSD # 1~4 Start Protection

OSD1_Start_Protection : 0x01 OSD2_Start_Protection : 0x02 OSD3_Start_Protection : 0x03 OSD4_Start_Protection : 0x04										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31	OSDx flag 1 : On ; 0 : Off
		Unused							D30~D27	Unused
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D26~D16	OSDx Left position
	OSD Left								D15~D11	Unused
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8	D10~D0	OSDx Top position
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	OSDx Top								Left position Max : 1919 Top position Max : 1079	

OSD # 1~4 End Protection

OSD1_End_Protection : 0x05 OSD2_End_Protection : 0x06 OSD3_End_Protection : 0x07 OSD4_End_Protection : 0x08										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D27	Unused
	Unused								D26~D16	OSDx Right position
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D15~D11	Unused
	OSD Right								D10~D0	OSDx Bottom position
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	OSD Bottom								Right position Max : 1919 Bootom position Max : 1079	

Demo Window

Demo Window : 0x09										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D25	Unused
	Unused								D24	Demo Window 1 : On ; 0 : Off
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0	Unused
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused									
Demo Window : 0x89										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused
	Unused								D0	Demo Window 1 : On ; 0 : Off

MEMC Level

ME Level : 0x0A										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D29	Unused
	Unused			ME Level					D28~24	ME Level 0~16
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16		
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		0 : Strong 1 : Normal 2 : Weak 3 : Off
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused								D23~D0	Unused
ME Level : 0x8A										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D5	Unused
	Unused			ME Level					D4~D0	ME Level 0~16
										0 : Strong 1 : Normal 2 : Weak 3 : Off

GV Mode

GV Mode : 0x0B										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D25	Unused
	Unused								D24	1 : Graphic ; 0 : Video
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0	Unused
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused									
GV Mode : 0x8B										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused
	Unused								D0	1 : Graphic ; 0 : Video

Blanking (Enable/Disable)

Blanking : 0x0C										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D26	Unused
	Unused								D24	Blanking; 1 : On ; 0 : Off
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0	Unused
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	When the input signal is unstable, the screen should be blanked.	
	Unused									

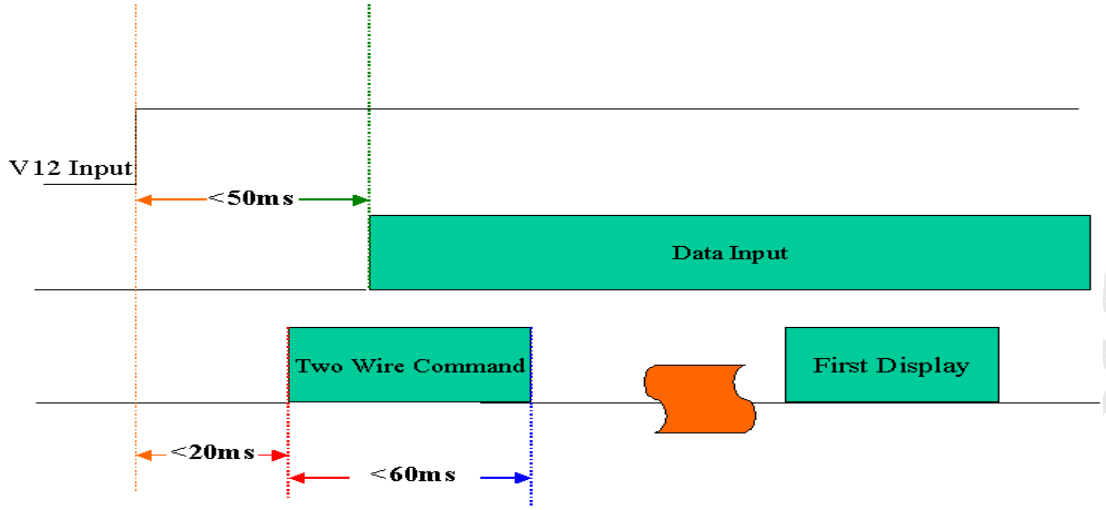
Blanking : 0x8C										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused
	Unused								D0	Blanking; 1 : On ; 0 : Off

A.6 TWO WIRE BUS REQUIREMENT

Symbol	Parameter	Condition	Min	Max	Unite
V_{IL}	Input Low-voltage		0	0.7	V
V_{IH}	Input High-voltage		2.7	3.3	V
V_{hys}(1)	Hysteresis of Schmitt Trigger Inputs		0.16	–	V
V_{OL}(1)	Output Low-voltage	3 mA sink current	0	0.4	V
t_r(1)	Rise Time for both SDA and SCL		20 + 0.1C_b(3)(2)	300	ns
t_{of}(1)	Output Fall Time from V_{IHmin} to V_{ILmax}	10 pF < C_b < 400 pF(1)	20 + 0.1C_b(3)(2)	250	ns
t_{SP}(1)	Spikes Suppressed by Input Filter		0	50(2)	ns
I_i	Input Current each I/O Pin	0.1V_{CC} < V_i < 0.9V_{CC}	-10	10	µA
C_i(1)	Capacitance for each I/O Pin		–	10	pF
f_{SCL}	SCL Clock Frequency	f_{CK}(4) > max(16f_{SCL}, 250kHz)(5)	0	400	kHz
Rp	Value of Pull-up resistor	f_{SCL} ≤ 100 kHz	3000	$\frac{1000ns}{C_b}$	Ω
		f_{SCL} > 100 kHz	3000	$\frac{300ns}{C_b}$	Ω
$t_{HD;STA}$	Hold Time (repeated) START Condition	f_{SCL} ≤ 100 kHz	4.0	–	µs
		f_{SCL} > 100 kHz	0.6	–	µs
t_{LOW}	Low Period of the SCL Clock	f_{SCL} ≤ 100 kHz(6)	4.7	–	µs
		f_{SCL} > 100 kHz(7)	1.3	–	µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0	–	µs
		f_{SCL} > 100 kHz	0.6	–	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	f_{SCL} ≤ 100 kHz	4.7	–	µs
		f_{SCL} > 100 kHz	0.6	–	µs
$t_{HD;DAT}$	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
		f_{SCL} > 100 kHz	0	0.9	µs
$t_{SU;DAT}$	Data setup time	f_{SCL} ≤ 100 kHz	250	–	ns
		f_{SCL} > 100 kHz	100	–	ns
$t_{SU;STO}$	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0	–	µs
		f_{SCL} > 100 kHz	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	f_{SCL} ≤ 100 kHz	4.7	–	µs
		f_{SCL} > 100 kHz	1.3	–	µs

A.7 THE TWO WIRE BUS SEQUENCE

Two Wire command can be initialized during 20ms to 60ms.



Example:

The previous state is strong mode, and the power is reset. The two wire command (strong mode command) must be initialized during 20ms to 60ms.