□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V420HF1
SUFFIX: PE1

Customer:

APPROVED BY **SIGNATURE**

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
KJ Cheng	Pam Liang	S C.Wang

CONTENTS

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 1.0	Aug. 23, 2012	All	All	Approval specification was first issued. (Tentative specification)
Ver. 1.1	Sep. 07,2012	13	5.1.2	Modify CN501 Connector Pin Assignment
		20	6.1.1	Modify Timing spec for frame rate 50Hz
		21	6.1.2	Modify Timing spec for frame rate 60Hz
		29	8.2	Modify Carton Label
		All		Change module to open cell

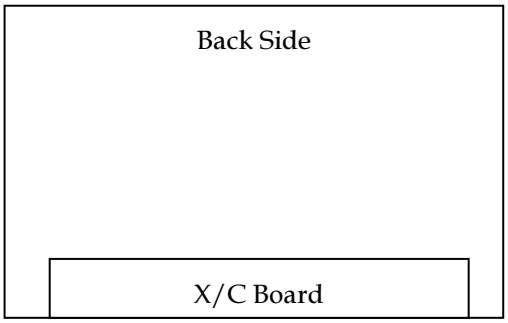
1. GENERAL DESCRIPTION

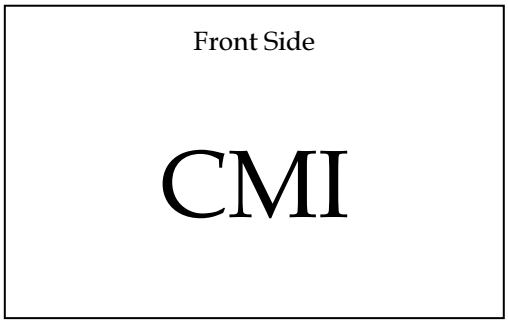
1.1 OVERVIEW

V420HF1-PE1 is a 42” TFT Liquid Crystal Display product with driver IC and 2ch-LVDS interface. This product supports 1920 x 1080 FHDTV format and can display 1.07G colors (10-bit/color).

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	42
Pixels [lines]	1920 × 1080
Active Area [mm]	930.24 (H) ×523.26 (V)
Sub-Pixel Pitch [mm]	0.1615(H) ×0.4845 (V)
Pixel Arrangement	RGB Vertical Stripe
Weight [g]	2000 Typ. (g)
Physical Size [mm]	961.14(with g-cof)*511.01(with s-cof & s-pcb)
Display Mode	Normallly black mode
Contrast Ratio	Typ. 1000:1 (Typical value measure by CMI’s Module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>10)	+88/-88(H), +88/-88(V) Typ. (CR≧10) (Typical value measure at CMI’s module)
Color Chromaticity	Rc = (0.662, 0.322) Gc = (0.275, 0.597) Bc = (0.134, 0.148) Wc= (0.301, 0.3371) * Please refer to “color chromaticity” on p.26
Cell Transparency [%]	4.7%
Polarizer Surface Treatment	Anti-Glare coating (Haze 1%), Hardness 3H & Glare coating,Hardness 3H
Rotation Function	Unachievable
Display Orientation	Signal input with “CMI”





1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight		2000		g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position 2. ABSOLUTE MAXIMUM RATINGS

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2)

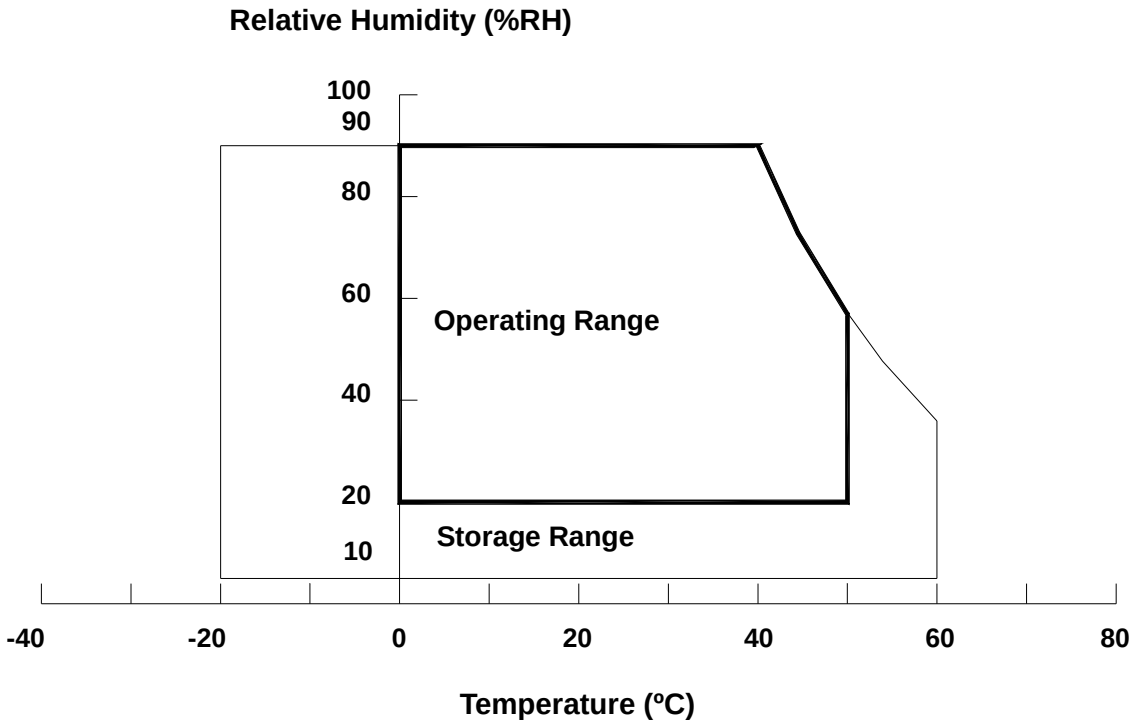
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD open cell alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.



When storing open cell as spares for a long time, the following precaution is necessary.

(a) Do not leave the open cell in high temperature, and high humidity for a long time. It is highly recommended to store the open cell with temperature from 0 to 35℃at normal humidity without condensation.

(b) The open cell shall be stored in dark place. Do not store the TFT-LCD open cell in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD OPEN CELL

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VDD	0	13.2	V	
Logic Input Voltage	V1	-0.3	4.0	V	

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD OPEN CELL

(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{DD}	11.4	12.0	12.6	V	(1)
Rush Current		I_{RUSH}	—	—	3.5	A	
Power Supply Current	White Pattern	—	—	1.23	1.72	A	(2)
	Horizontal Stripe	—	—	1.753	2.45	A	
	Black Pattern	—	—	1.19	1.66	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(3)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	100	—	600	mV	
	Terminating Resistor	R_T	87	110	133	Ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	3.0	3.3	3.6	V	
	Input Low Threshold Voltage	V_{IL}	0	0	0.6	V	

Note (1) The open cell should be always operated within the above ranges.

Note (2) The specified power supply current is under the conditions at VDD = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, fCLK=74.25MHz , whereas a power dissipation check pattern below is displayed.

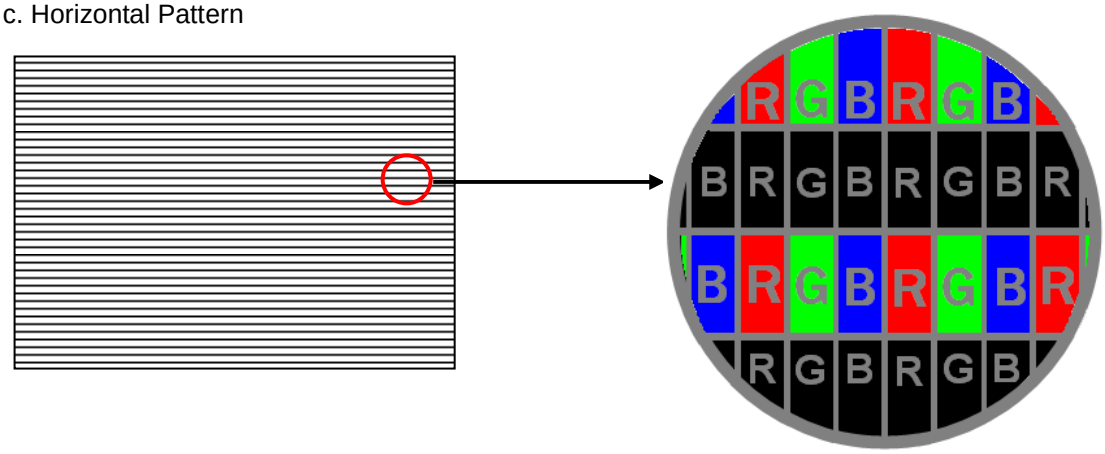
a. White Pattern

Active Area

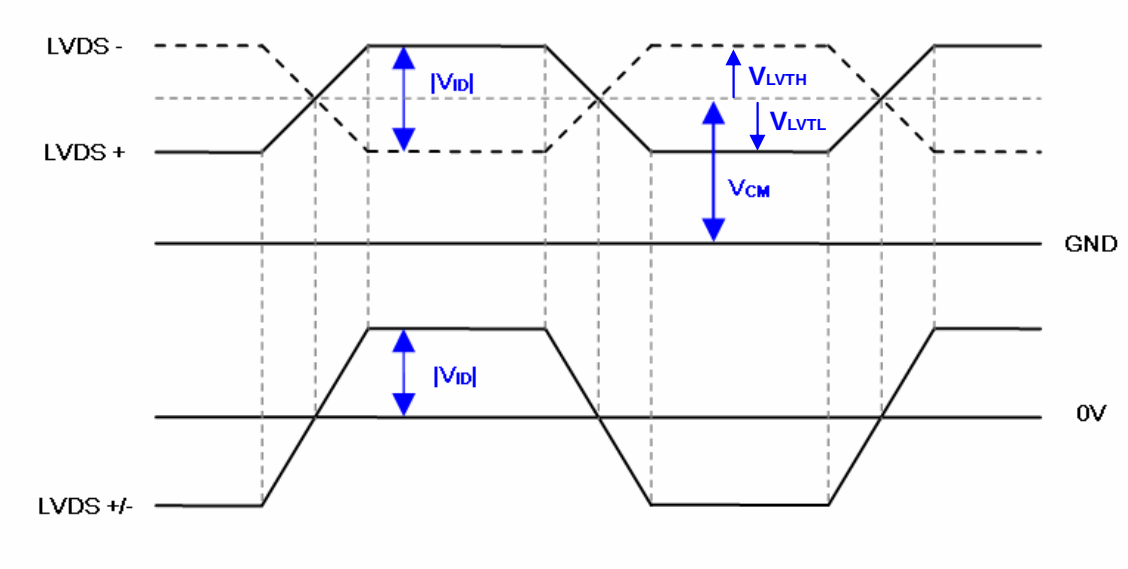
b. Black Pattern

Active Area

c. Horizontal Pattern

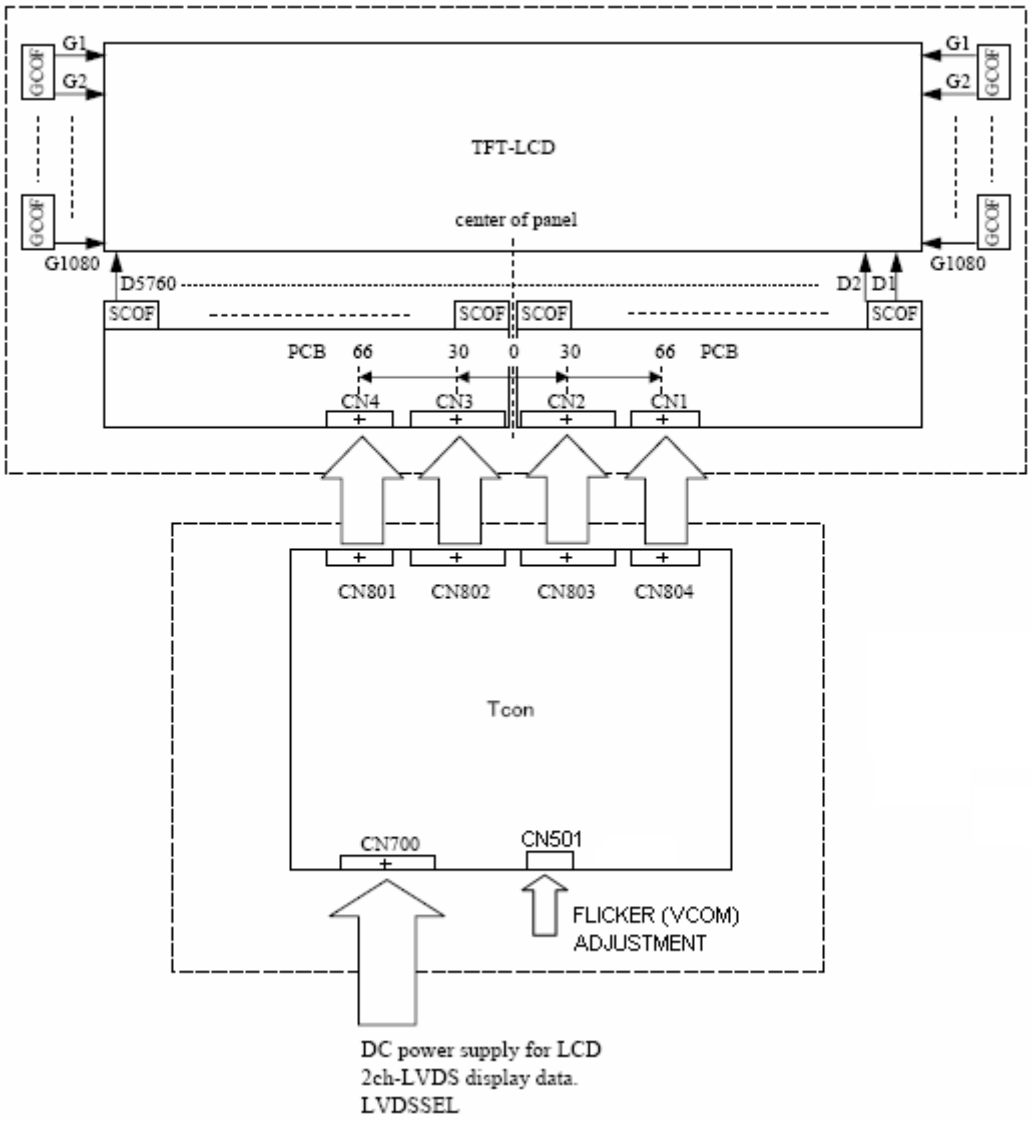


Note (3) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD OPEN CELL



Note

1) CN1 relays FFC(40pin) and must connect it with TCON's CN804.

2) CN2 relays FFC(60pin) and must connect it with TCON's CN803.

3) CN3 relays FFC(60pin) and must connect it with TCON's CN802.

4) CN4 relays FFC(40pin) and must connect it with TCON's CN801.

5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD OPEN CELL INPUT

5.1.1:CN700 Connector Pin Assignment: (JAE FM8S060HA2)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	LVDSSEL	Select LVDS Data Format	(2)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	
11	N.C.	No Connection	
12	N.C.	No Connection	
13	VSS	Ground (0V)	(3)
14	Rx0AN	Odd pixel Negative LVDS differential data input. Channel 1	(4)
15	Rx0AP	Odd pixel Positive LVDS differential data input. Channel 1	
16	Rx0BN	Odd pixel Negative LVDS differential data input. Channel 2	
17	Rx0BP	Odd pixel Positive LVDS differential data input. Channel 2	
18	Rx0CN	Odd pixel Negative LVDS differential data input. Channel 3	
19	Rx0CP	Odd pixel Positive LVDS differential data input. Channel 3	
20	VSS	Ground (0V)	(3)
21	Rx0CKN	Odd pixel Negative LVDS differential clock input.	(4)
22	Rx0CKP	Odd pixel Positive LVDS differential clock input.	
23	VSS	Ground (0V)	(3)
24	Rx0DN	Odd pixel Negative LVDS differential data input. Channel 4	(4)
25	Rx0DP	Odd pixel Positive LVDS differential data input. Channel 4	
26	Rx0EN	Odd pixel Negative LVDS differential data input. Channel 5	
27	Rx0EP	Odd pixel Positive LVDS differential data input. Channel 5	
28	VSS	Ground (0V)	(3)

29	Rx1AN	Even pixel Negative LVDS differential data input. Channel 1	(4)
30	Rx1AP	Even pixel Positive LVDS differential data input. Channel 1	
31	Rx1BN	Even pixel Negative LVDS differential data input. Channel 2	
32	Rx1BP	Even pixel Positive LVDS differential data input. Channel 2	
33	Rx1CN	Even pixel Negative LVDS differential data input. Channel 3	
34	Rx1CP	Even pixel Positive LVDS differential data input. Channel 3	
35	VSS	Ground (0V)	(3)
36	Rx1CKN	Even pixel Negative LVDS differential clock input.	(4)
37	Rx1CKP	Even pixel Positive LVDS differential clock input.	
38	VSS	Ground (0V)	(3)
39	Rx1DN	Even pixel Negative LVDS differential data input. Channel 4	(4)
40	Rx1DP	Even pixel Positive LVDS differential data input. Channel 4	
41	Rx1EN	Even pixel Negative LVDS differential data input. Channel 5	
42	Rx1EP	Even pixel Positive LVDS differential data input. Channel 5	
43	VSS	Ground (0V)	(3)
44	VSS	Ground (0V)	
45	VSS	Ground (0V)	
46	VSS	Ground (0V)	
47	VSS	Ground (0V)	
48	VSS	Ground (0V)	
49	VSS	Ground (0V)	
50	VSS	Ground (0V)	
51	VSS	Ground (0V)	
52	VDD	Power Supply (typ.+12V)	(5)
53	VDD	Power Supply (typ.+12V)	
54	VDD	Power Supply (typ.+12V)	
55	VDD	Power Supply (typ.+12V)	
56	VDD	Power Supply (typ.+12V)	
57	VDD	Power Supply (typ.+12V)	
58	VDD	Power Supply (typ.+12V)	
59	VDD	Power Supply (typ.+12V)	
60	VDD	Power Supply (typ.+12V)	

5.1.2: CN501 Connector Pin Assignment: (JST SM12B-SRSS-TB (LF))

Pin	120Hz operation mode	VCOM adjust mode	Note
1	No Connection	High	(7)
2	No Connection	High	
3	No Connection	Low	
4	No Connection	Low	
5	No Connection	Low	
6	No Connection	High	
7	No Connection	I2CPOW	(6)
8	No Connection	I2CCLK	
9	No Connection	I2CDAT	
10	No Connection	Ground (0V)	(3)
11	No Connection	No Connection	(1)
12	No Connection	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND or open, H=Connect to +3.3V

SELLVDS	Note
L or open	JEIDA Format
H	VESA Format

Note (3) All V_{SS} pins shall be grounded.

Note (4) Two pixel data send into the open cell for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

Note (5) All V_{DD} pins shall be connected to +12.0V (Typ.).

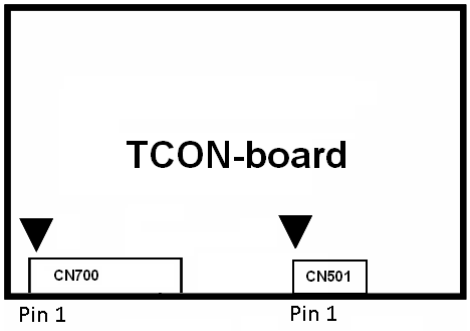
Note (6) I2CPOW is defined as I2C Power for E2PROM Write

I2CCLK is defined as I2C CLOCK

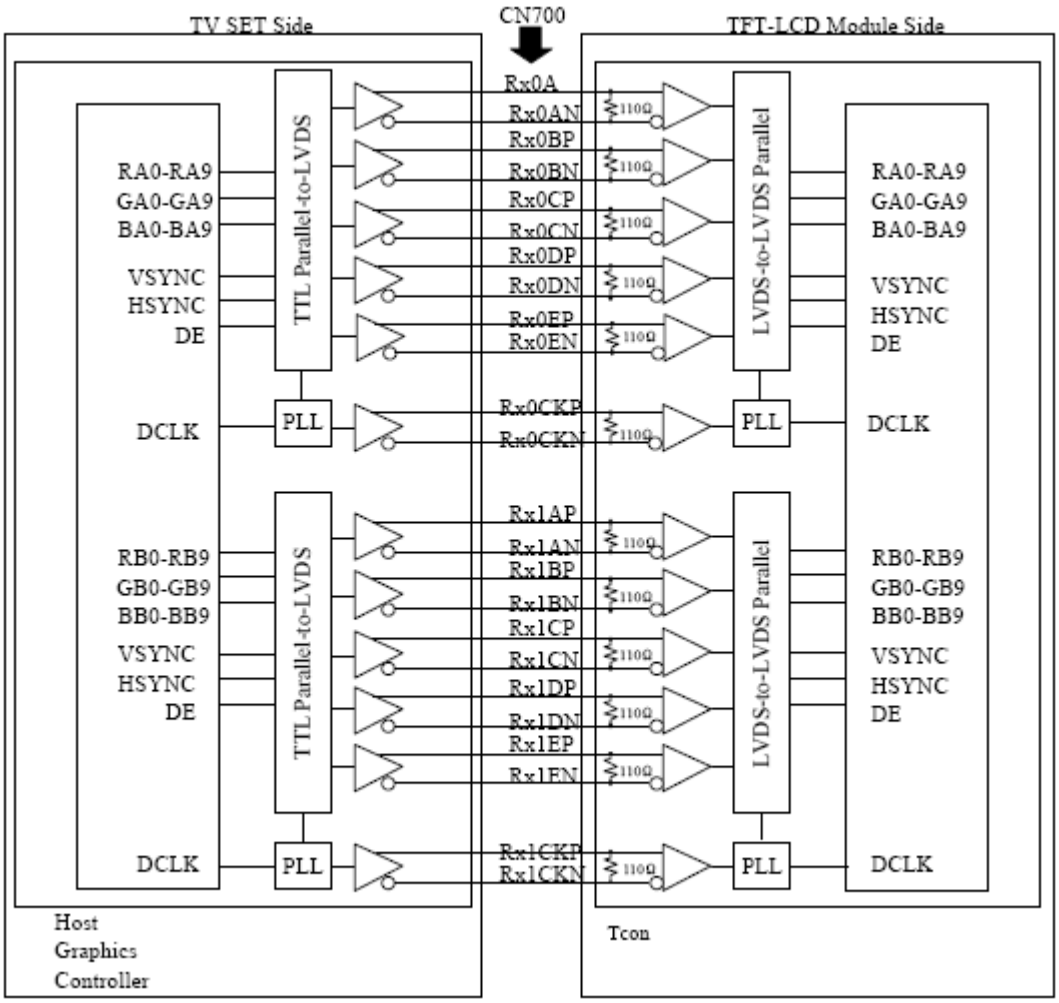
I2CDAT is defined as I2C DATA

Note (7) Low= Connect to GND, High=Connect to +3.3V

Note (8) CN700 & CN501 connector pin orderdefined as follows



5.2 BLOCK DIAGRAM OF INTERFACE



RA0～RA9, RB0～RB9 : Pixel R Data (9; MSB, 0; LSB)

GA0～GA9, GB0～GB9 : Pixel G Data (9; MSB, 0; LSB)

BA0～BA9, BB0～BB9 : Pixel B Data (9; MSB, 0; LSB)

VSYNC : Vertical Sync

HSYNC : Horizontal Sync

DE : Data Enable

Note 1) The system must have the transmitter to drive the open cell.

2) LVDS cable impedance shall be 55 ohms per signal line or about 110 ohms per twist-pair line when it is used differentially.

5.3 LVDS INTERFACE

JEIDA Format : SELLVDS = L or Open

VESA Format : SELLVDS = H

VESA LVDS format

The LVDSSEL signal of CN700 pin No.8 specification is “H” 【LVDSSEL = H】

	SIGNAL	INTERFACE CONNECTOR		TFT CONTROL
		TV Set	TFT-LCD	INPUT
30bit	RA0/RB0	Tx0AP/Tx1AP	Rx0AP/Rx1AP	RA0/RB0
	RA1/RB1			RA1/RB1
	RA2/RB2			RA2/RB2
	RA3/RB3			RA3/RB3
	RA4/RB4	Tx0AN/Tx1AN	Rx0AN/Rx1AN	RA4/RB4
	RA5/RB5			RA5/RB5
	GA0/GB0			GA0/GB0
	GA1/GB1	Tx0BP/Tx1BP	Rx0BP/Rx1BP	GA1/GB1
	GA2/GB2			GA2/GB2
	GA3/GB3			GA3/GB3
	GA4/GB4	Tx0BN/Tx1BN	Rx0BN/Rx1BN	GA4/GB4
	GA5/GB5			GA5/GB5
	BA0/BB0			BA0/BB0
	BA1/BB1			BA1/BB1
	BA2/BB2	Tx0CP/Tx1CP	Rx0CP/Rx1CP	BA2/BB2
	BA3/BB3			BA3/BB3
	BA4/BB4			BA4/BB4
	BA5/BB5	Tx0CN/Tx1CN	Rx0CN/Rx1CN	BA5/BB5
	HSYNC			HSYNC
	VSYNC			VSYNC
	YS			YS
	RA6/RB6	Tx0DP/Tx1DP	Rx0DP/Rx1DP	RA6/RB6
	RA7/RB7			RA7/RB7
	GA6/GB6			GA6/GB6
	GA7/GB7	Tx0DN/Tx1DN	Rx0DN/Rx1DN	GA7/GB7
	BA6/BB6			BA6/BB6
	BA7/BB7			BA7/BB7
	RSVD 1)			RSVD 1)
	RA8/RB8	Tx0EP/Tx1EP	Rx0EP/Rx1EP	RA8/RB8
	RA9/RB9			RA9/RB9
	GA8/GB8			GA8/GB8
	GA9/GB9	Tx0EN/Tx1EN	Rx0EN/Rx1EN	GA9/GB9
	BA8/BB8			BA8/BB8
	BA9/BB9			BA9/BB9
	LRID			LRID
	DCLK	Tx0CKP/Tx1CKP Tx0CKN/Tx1CKN	Rx0CKP/Rx1CKP Rx0CKN/Rx1CKN	DCLK

RA0～RA9, RB0～RB9 : Pixel R Data (9; MSB, 0; LSB)

GA0～GA9, GB0～GB9 : Pixel G Data (9; MSB, 0; LSB)

BA0～BA9, BB0～BB9 : Pixel B Data (9; MSB, 0; LSB)

VSYNC : Vertical Sync

HSYNC : Horizontal Sync

Note 1) RSVD(reserved) pins on the transmitter shall be tied to"H"or"L".

JEDIA LVDS format

The LVDSSEL signal of CN700 pin No.8 specification is “L” or open.【LVDSSEL = L or Open】

	SIGNAL	INTERFACE CONNECTOR		TFT CONTROL
		TV Set	TFT-LCD	INPUT
30bit	RA4/RB4	Tx0AP/Tx1AP	Rx0AP/Rx1AP	RA4/RB4
	RA5/RB5			RA5/RB5
	RA6/RB6			RA6/RB6
	RA7/RB7			RA7/RB7
	RA8/RB8	Tx0AN/Tx1AN	Rx0AN/Rx1AN	RA8/RB8
	RA9/RB9			RA9/RB9
	GA4/GB4			GA4/GB4
	GA5/GB5	Tx0BP/Tx1BP	Rx0BP/Rx1BP	GA5/GB5
	GA6/GB6			GA6/GB6
	GA7/GB7			GA7/GB7
	GA8/GB8	Tx0BN/Tx1BN	Rx0BN/Rx1BN	GA8/GB8
	GA9/GB9			GA9/GB9
	BA4/BB4			BA4/BB4
	BA5/BB5			BA5/BB5
	BA6/BB6	Tx0CP/Tx1CP	Rx0CP/Rx1CP	BA6/BB6
	BA7/BB7			BA7/BB7
	BA8/BB8			BA8/BB8
	BA9/BB9	Tx0CN/Tx1CN	Rx0CN/Rx1CN	BA9/BB9
	HYSNC			HSYNC
	VSYNC			VSYNC
	YS			YS
	RA2/RB2	Tx0DP/Tx1DP	Rx0DP/Rx1DP	RA2/RB2
	RA3/RB3			RA3/RB3
	GA2/GB2			GA2/GB2
	GA3/GB3	Tx0DN/Tx1DN	Rx0DN/Rx1DN	GA3/GB3
	BA2/BB2			BA2/BB2
	BA3/BB3			BA3/BB3
	RSVD 1)			RSVD 1)
	RA0/RB0	Tx0EP/Tx1EP	Rx0EP/Rx1EP	RA0/RB0
	RA1/RB1			RA1/RB1
	GA0/GB0			GA0/GB0
	GA1/GB1	Tx0EN/Tx1EN	Rx0EN/Rx1EN	GA1/GB1
	BA0/BB0			BA0/BB0
	BA1/BB1			BA1/BB1
	LRID			LRID
	DCLK	Tx0CKP/Tx1CKP Tx0CKN/Tx1CKN	Rx0CKP/Rx1CKP Rx0CKN/Rx1CKN	DCLK

RA0～RA9, RB0～RB9 : Pixel R Data (9; MSB, 0; LSB)

GA0～GA9, GB0～GB9 : Pixel G Data (9; MSB, 0; LSB)

BA0～BA9, BB0～BB9 : Pixel B Data (9; MSB, 0; LSB)

VSYNC : Vertical Sync

HSYNC : Horizontal Sync

Note 1) RSVD(reserved) pins on the transmitter shall be tied to"H"or"L".

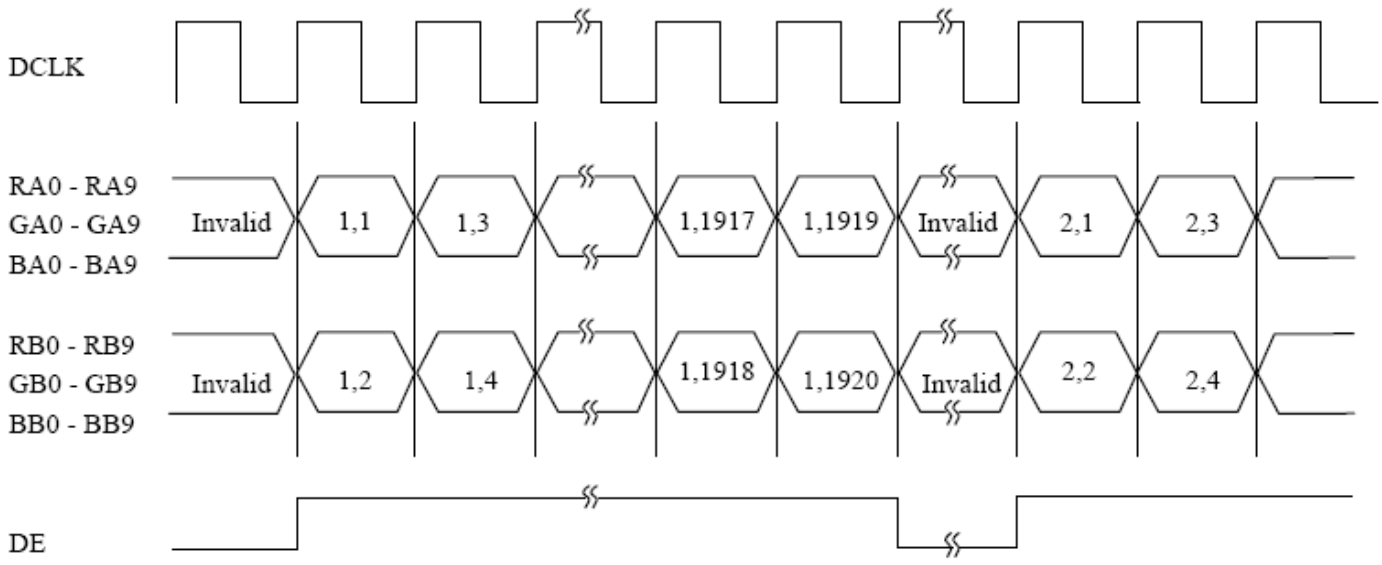
5.4 CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

Display data of adjacent one pixel is latched during one cycle of DCLK

	(1,1)			(1,2)	
BA	GA	RA	BB	GB	RB

ODD pixel : RA0 - RA9 : Red data
GA0 - GA9 : Green data
BA0 - BA9 : Blue data
EVEN pixel RB0 - RB9 : Red data
GB0 - GB9 : Green data
BB0 - BB9 : Blue data

1 , 1	1 , 2	1 , 3	- -	1 , 1920
2 , 1	2 , 2	2 , 3	- -	2 , 1920
3 , 1	3 , 2	3 , 3	- -	3 , 1920
1080 , 1	1080 , 2	1080 , 3		1080, 1920



5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color \ Input		Red Data										Green Data										Blue Data									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
		MSB									LSB	MSB									LSB	MSB									LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note 1) Definition of gray scale :

Color(n)・・・・Number in parenthesis indicates gray scale level.

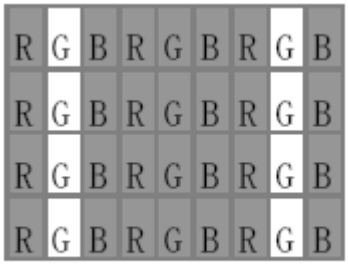
Larger n correspondsto brighter level

2) Data : 1 : High, 0 : Low

5.6 FLICKER (VCOM) ADJUSTMENT

(1) Adjustment Pattern:

Flick pattern was shown as below. If customer needs below pattern, please directly contact with CMI account FAE.



Display Pattern of Flicker

(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com.The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

a. USB Sensor Board.

b. Programmable software.

(3)CN501 setting must follow page.13 “5.1.2: CN501 Connector Pin Assignment_ V COM adjust mode”

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	73.6	74.25	75.4	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	150	ps	(2)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-3%	-	F_{clkin}+3%	MHz	(3)
	Spread spectrum modulation frequency	F_{SSM}	-	-	60	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-	-	-	ps	(4)

6.1.1 Timing spec for Frame Rate = 50Hz

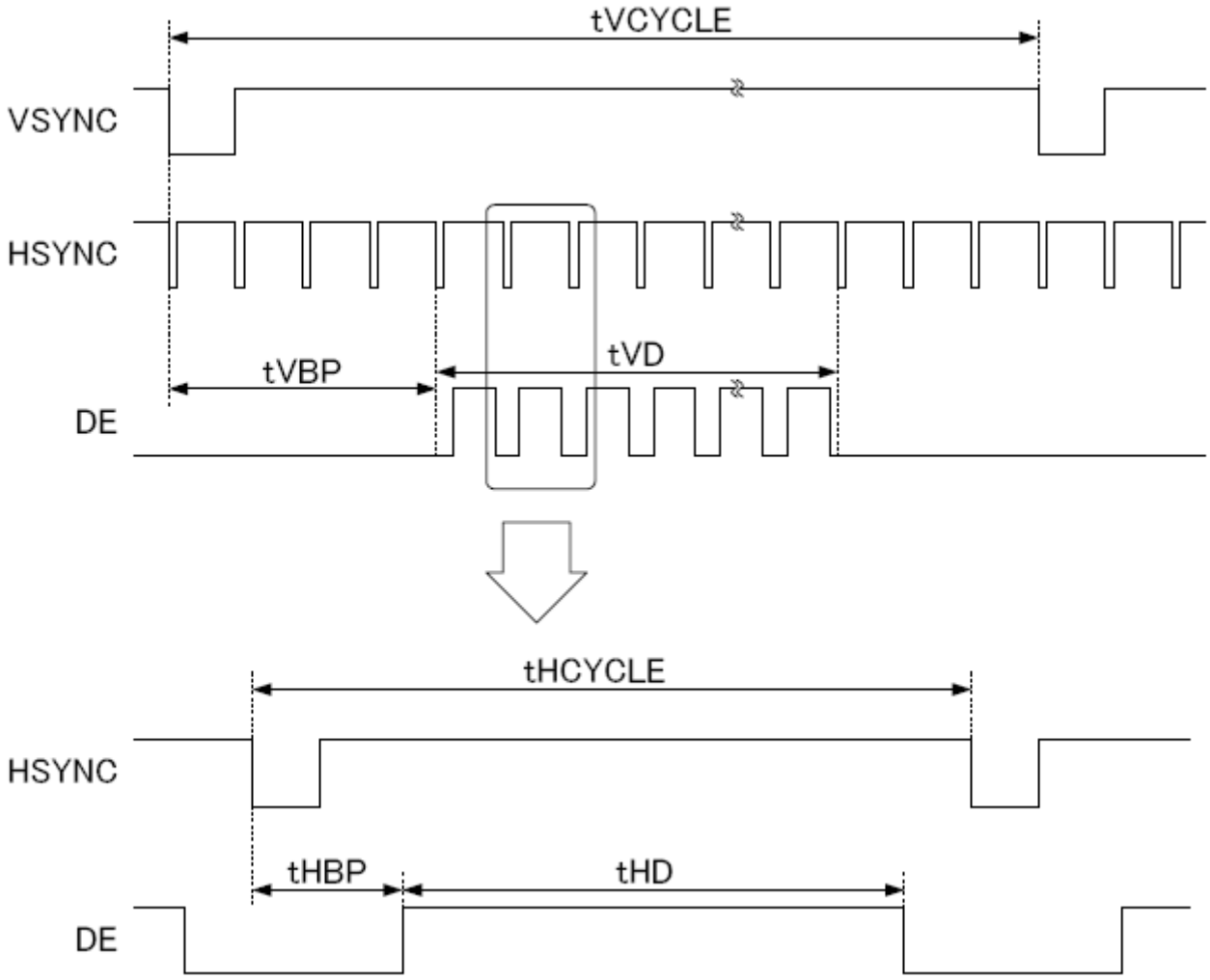
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	--	50	--	Hz	
Vertical Active Display Term	2D Mode	Total	tVCYCLE	--	1338	--	Th	tVCYCLE=tVD+Tvb
		Display	tVD	--	1080	--	Th	—
		Blank	Tvb	--	258	--	Th	—
		Vertical Back Porch	tVBP	--	20	--	Th	-
Horizontal Active Display Term	2D Mode	Total	tHCYCLE	--	1109	--	Tc	tHCYCLE=tHD+Thb
		Display	tHD	--	960	--	Tc	—
		Blank	Thb	--	149	--	Tc	—
		Horizontal Back Porch	tHBP	--	24	--	Tc	—

6.1.2 Timing spec for Frame Rate = 60Hz

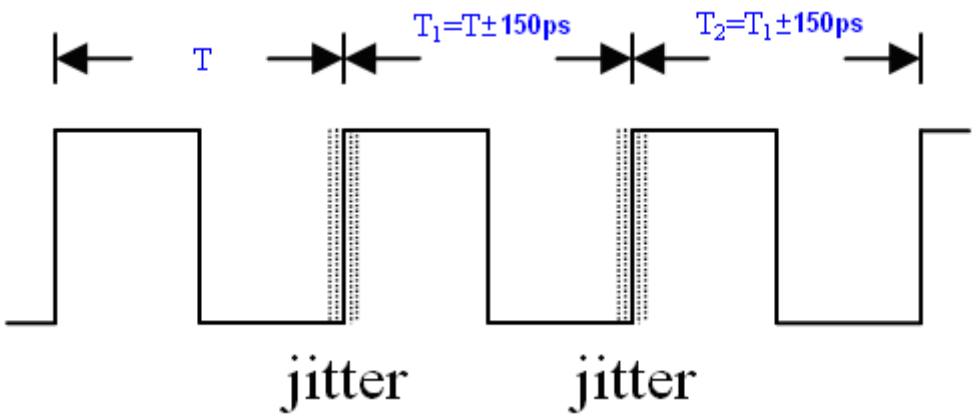
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	--	60	--	Hz	
Vertical Active Display Term	2D Mode	Total	tVCYCLE	--	1115	--	Th	tVCYCLE=tVD+Tvb
		Display	tVD	--	1080	--	Th	—
		Blank	Tvb	--	35	--	Th	—
		Vertical Back Porch	tVBP	--	20	--	Th	-
Horizontal Active Display Term	2D Mode	Total	tHCYCLE	--	1109	--	Tc	tHCYCLE=tHD+Thb
		Display	tHD	--	960	--	Tc	—
		Blank	Thb	--	149	--	Tc	—
		Horizontal Back Porch	tHBP	--	24	--	Tc	—

Note (1) Please make sure the value of tVBP and tHBP has followed the above-mentioned specification.If setting the wrong value, the display image can't be full screen.

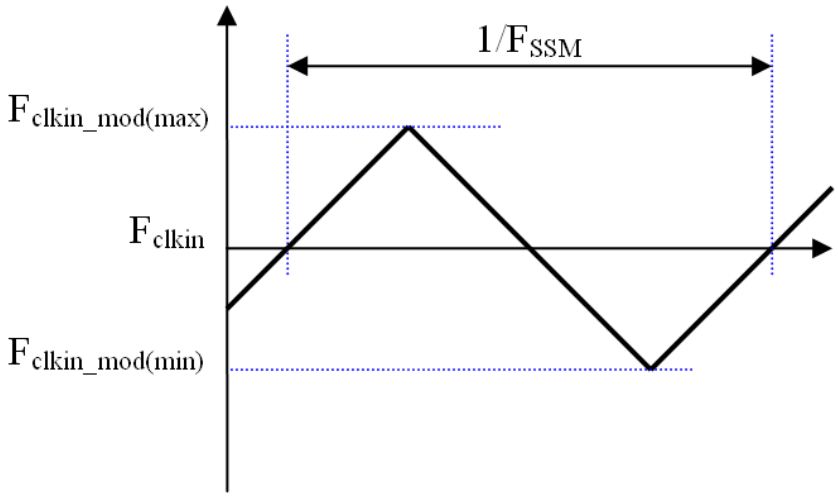
INPUT SIGNAL TIMING DIAGRAM



Note (2) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

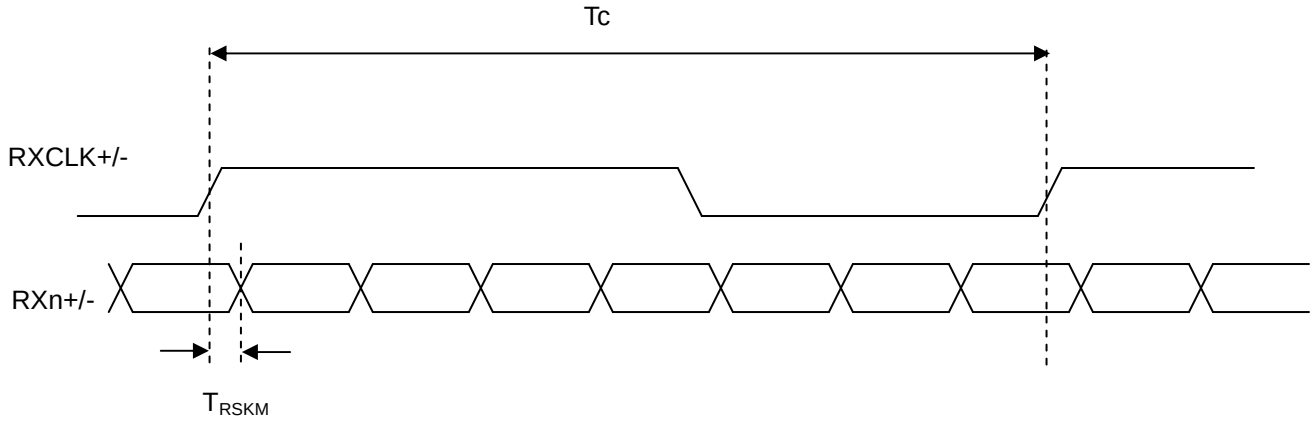


Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (4) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

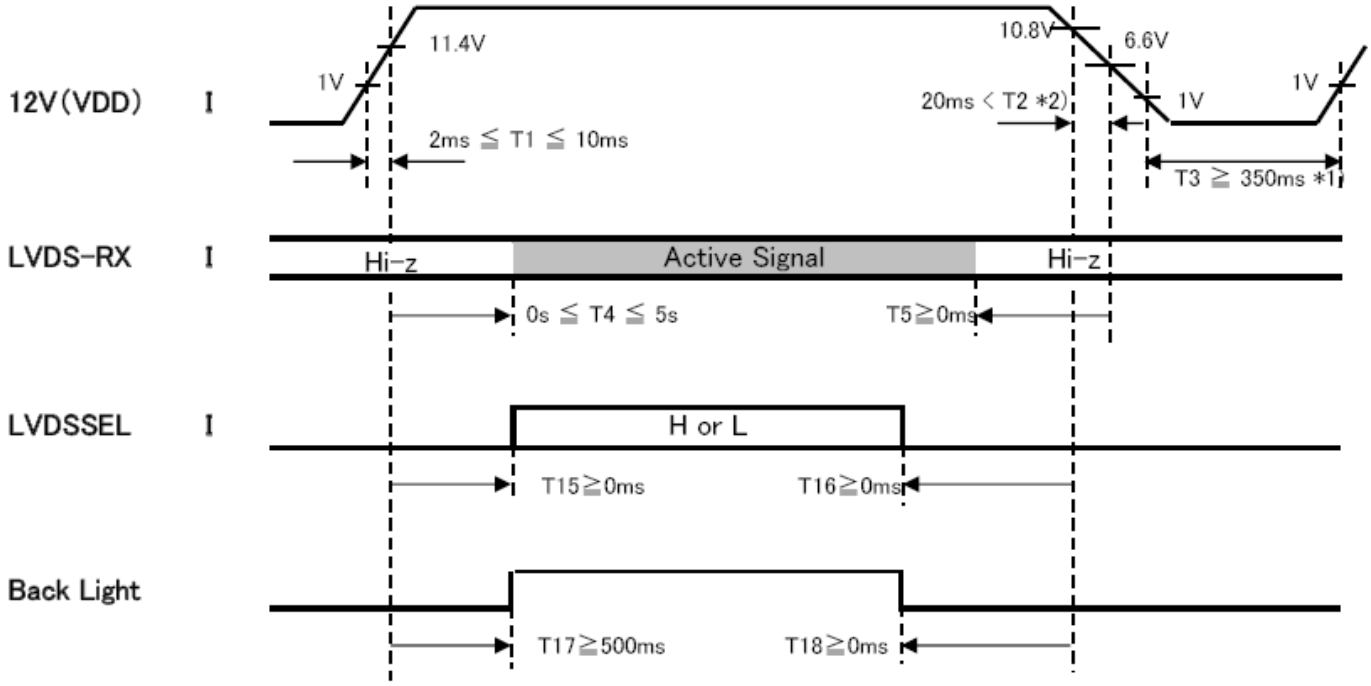


6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

6.2.1 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD open cell, the power on/off sequence should be as the diagram below.



*1) There is a case that afterimage can be seen if this specification is not followed.
However, as long as the afterimage can be allowed, it is tolerated.

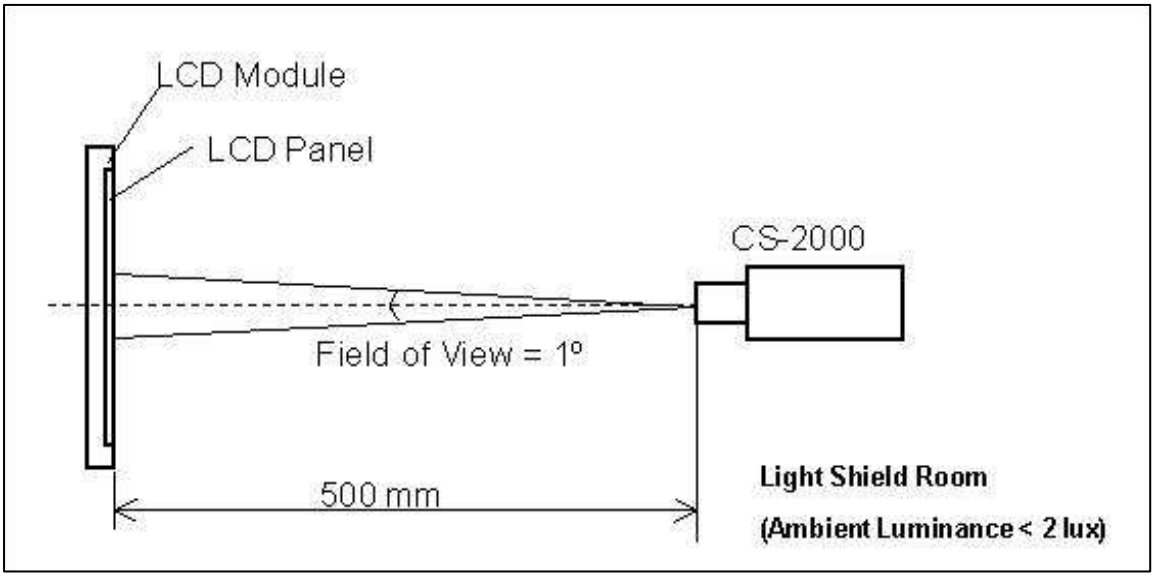
*2) The T2 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Vertical Frame Rate	Fr	60	Hz
LED Current (LED Model)	I_L	60	mA

The LCD open cell should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction Standard light source "C"	-0.03	0.662	+0.03	-	(0)
		Rcy			0.322		-	
	Green	Gcx			0.275		-	
		Gcy			0.597		-	
	Blue	Bcx			0.134		-	
		Bcy			0.148		-	
	White	Wcx			0.301		-	
		Wcy			0.371		-	
Center Transmittance		T%	θ_x=0°, θ_Y =0°		4.7		%	(1),(5)
Transmittance Variation		δT				1.3		(1),(6)
Contrast Ratio		CR		700	1000		-	(1),(3)
Response Time		Gray to gray	θ_x=0°, θ_Y =0°		6.5		ms	(1),(4)
Viewing Angle	Horizontal	θ_x+	CR≥10		88		Deg.	(1),(2)
		θ_x-			88			
	Vertical	θ_Y+			88			
		θ_Y-			88			

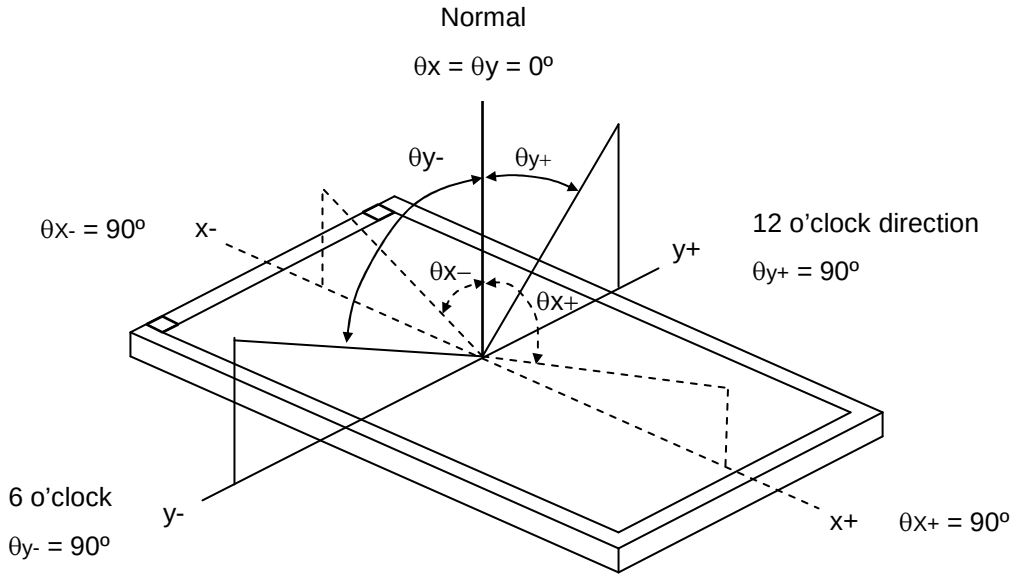
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following :

1. Measure open cell's and BLU's spectrum at center point. W, R,G, B are with signal input. BLU is supplied by CMI .
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

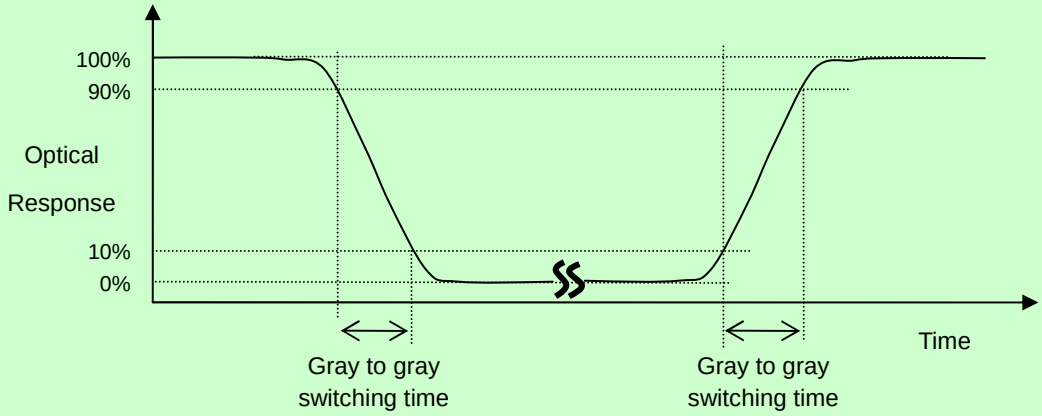
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (5).

Note (4) Definition of Response Time (T_R, T_F):



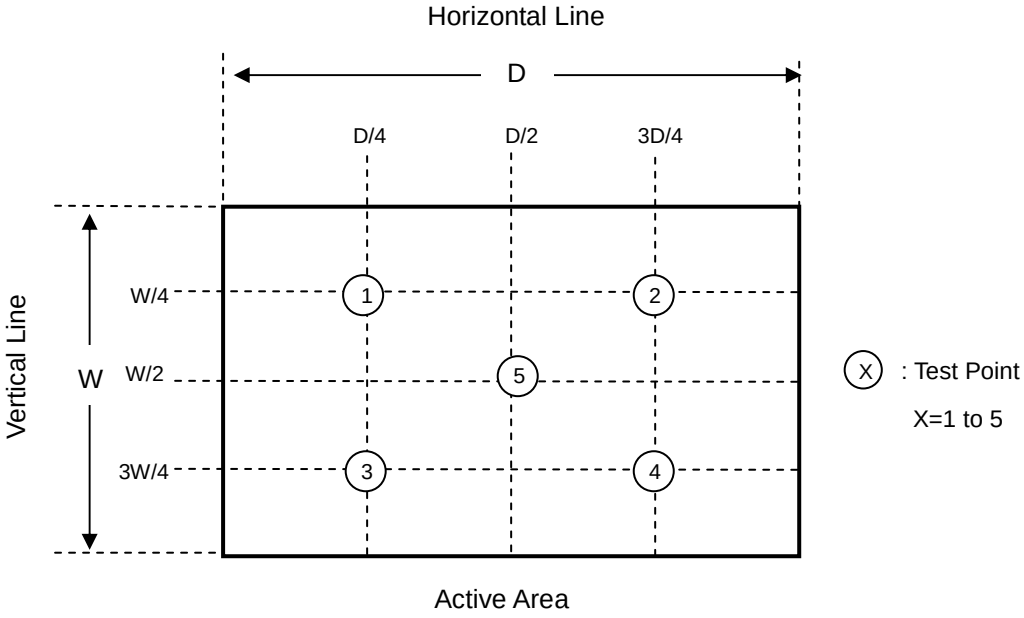
The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



Note (6) Definition of Transmittance (T%) :

Measure the luminance of gray level 1023 at center point of LCD open cell.

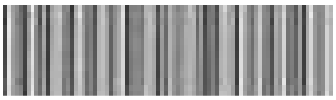
$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD open cell}}{\text{Luminance of backligh unit}} \times 100\%$$

8. DEFINITION OF LABELS

8.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.

V420HF1-PE1



XXXXXXXXXXXXX

V420HF1-PE1 Rev.

XXXXXXXXXXXXX

8.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation

P.O. NO._____Made in Taiwan

Part ID._____Quantities _____

Model Name._____

Carton ID.___XXXXXXXXXXXXX___ RoHS

P.O. NO._____Made in China

Part ID._____Quantities _____

Model Name._____

Carton ID.___XXXXXXXXXXXXX___ RoHS

(a) Model Name: V420HF1– PE1

(b) Carton ID: CMI internal control

(c) Quantities:

9. PACKAGING

9.1 PACKING SPECIFICATIONS

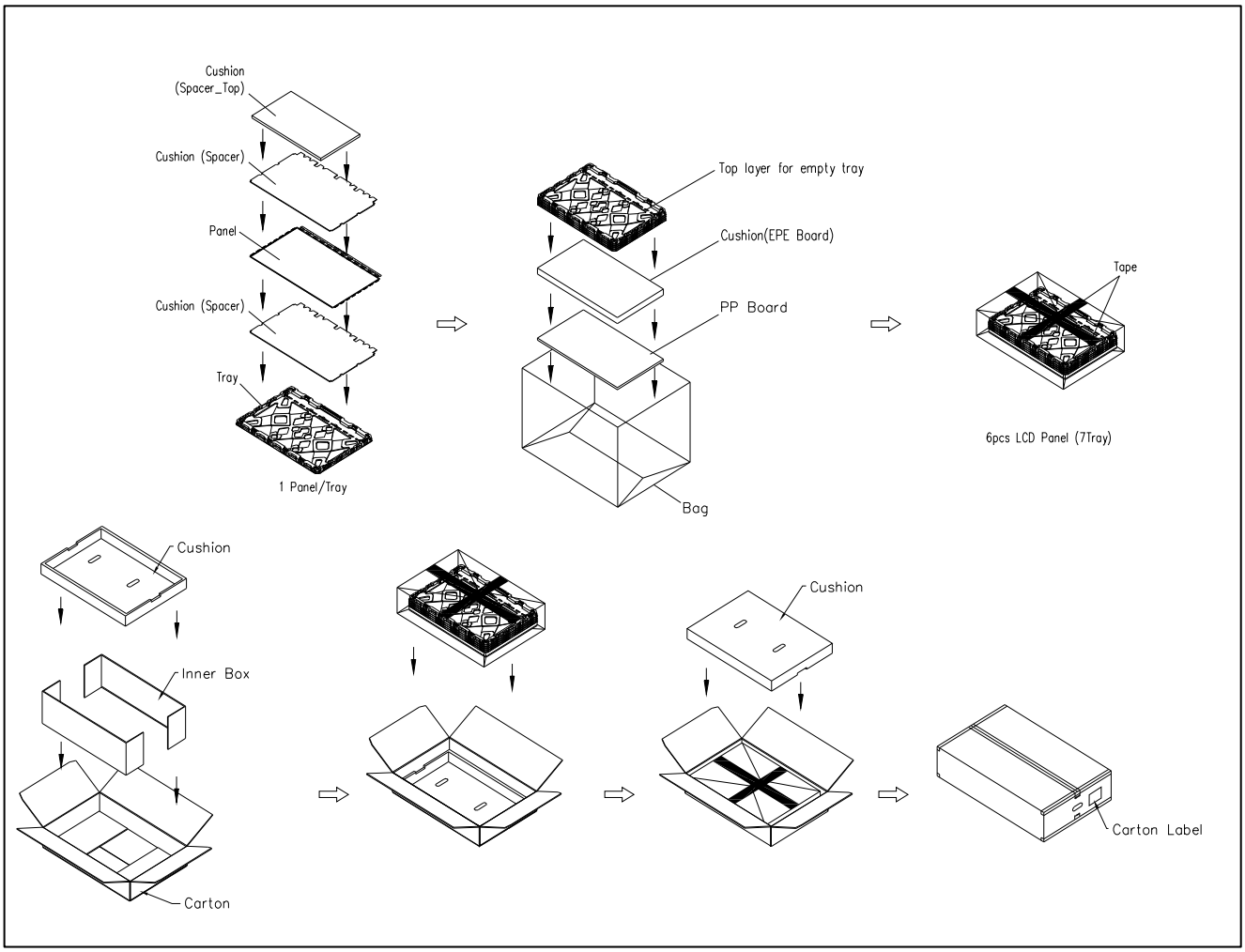
(1) 6 LCD TV Panels / 1 Carton

(2) Box dimensions : 1123 (L) X 818 (W) X245 (H)mm

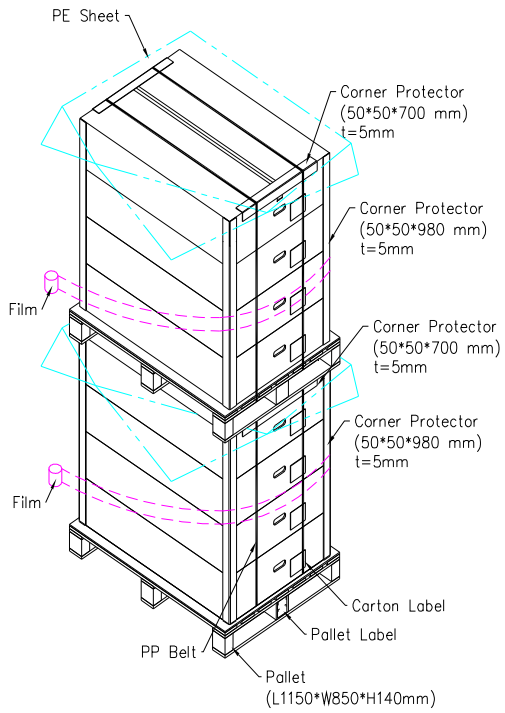
(3) Weight :approximately 16Kg (6 panels per box)

9.2 PACKING METHOD

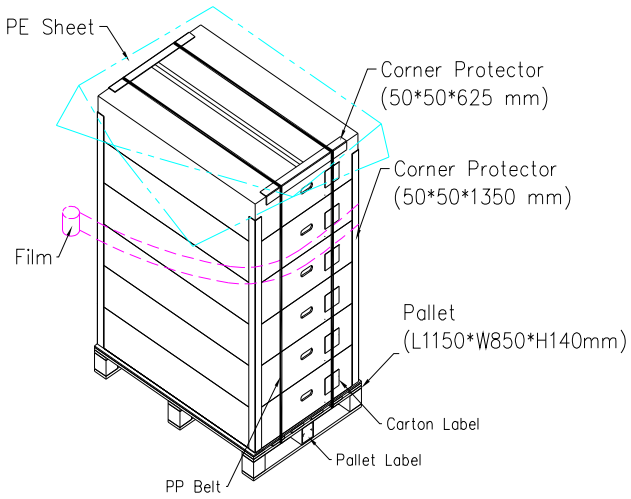
Figures 9-1 and 9-2 are the packing method



Sea & Land Transportation



Air Transportation



10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the product during assembly.

(2) To assemble backlight or install open cell into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the open cell because the LCD panel will be damaged.

(4) Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the open cell is operating.

(6) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(7) It is dangerous that moisture come into or contacted the product, because moisture may damage the product when it is operating.

(8) High temperature or humidity may reduce the performance of open cell. Please store this product within the specified storage conditions.

(9) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

10.2 SAFETY PRECAUTIONS

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the product's end of life, it is not harmful in case of normal operation and storage.

11. MECHANICAL CHARACTERISTIC