

- ☐ Tentative Specification
- ☐ Preliminary Specification
- ☒ Approval Specification

MODEL NO.: V420HJ1
SUFFIX: P02

Customer:	
APPROVED BY	SIGNATURE
Name / Title _____	_____
Note	
Please return 1 copy for your confirmation with your signature and comments.	

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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 1.0	Mar 20, 2012	All	All	The Preliminary specification was first issued.
Ver. 2.0	Apr 12, 2012	All	All	The Approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420HJ1-P02 is a 42" TFT Liquid Crystal Display product with driver ICs and 2ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit/color).

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	42.02
Pixels [lines]	1920 × 1080
Active Area [mm]	930.24(H) × 523.26(V) (42.02" diagonal)
Sub-Pixel Pitch [mm]	0.1615(H) × 0.4845(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 2107g
Physical Size [mm]	957.72 (W) × 564.61 (H) × 1.75 (D) Typ.
Display Mode	Transmissive mode / Normally black
Contrast Ratio	5000:1 Typ. (Typical value measure at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H), +88/-88(V) Typ. (CR ≥ 20) (Typical value measure at CMI's module)
Color Chromaticity	R = (0.653, 0.325) G = (0.301, 0.597) B = (0.134, 0.110) W = (0.318, 0.360) * Please refer to "color chromaticity" on p.23
Cell Transparency [%]	5.7 %
Polarizer Surface Treatment	Anti-Glare coating (Haze 3.5%), Hard coating (3H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight		2107		g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position

2. ABSOLUTE MAXIMUM RATINGS

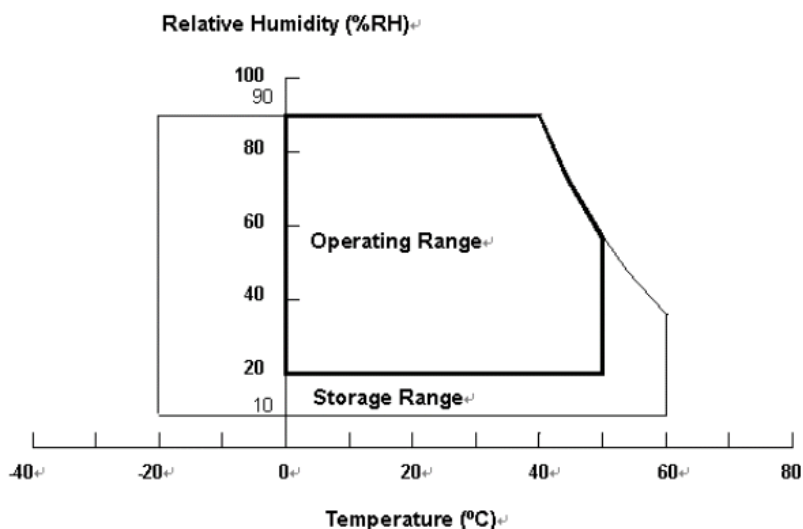
2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ($T_a \leq 40$ °C).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stroed in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

3. ELECTRICAL CHARACTERISTICS

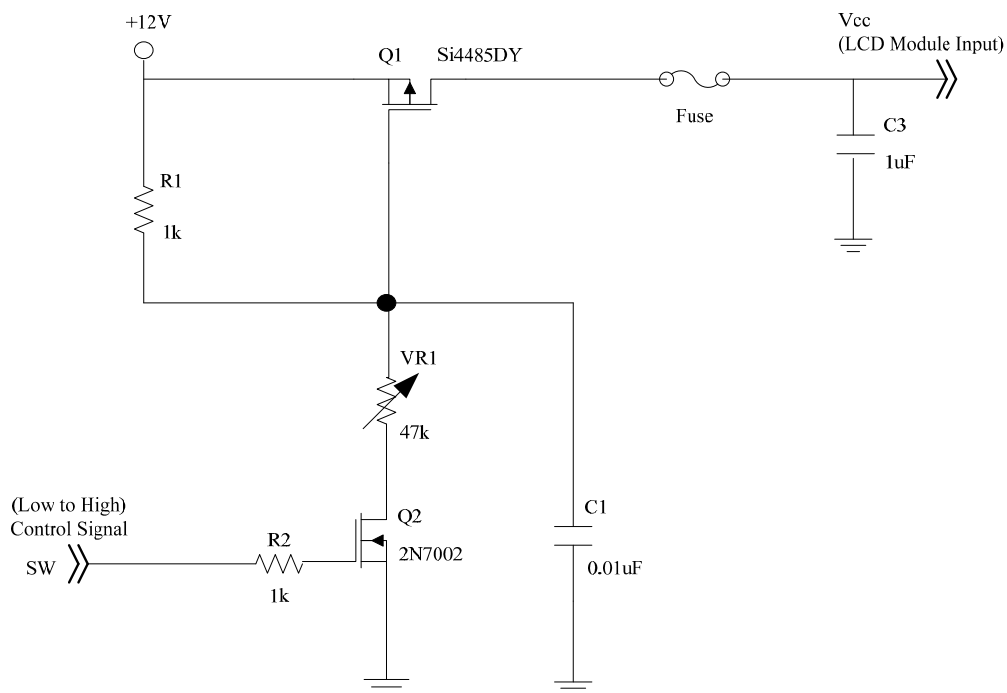
3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

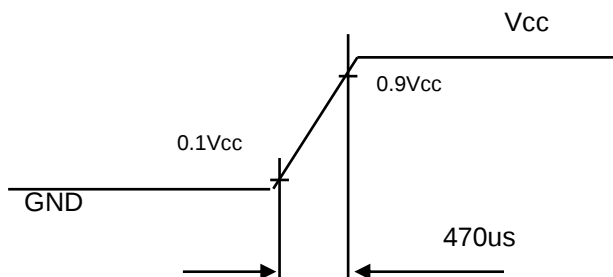
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	3.5	A	(2)
Power Supply Current	White Pattern	—	—	0.336	—	A	(3)
	Horizontal Stripe	—	—	0.576	0.663	A	
	Black Pattern	—	—	0.324	—	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

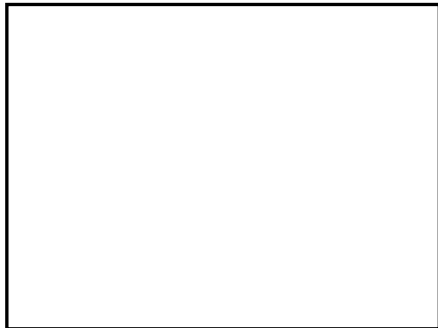


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at $V_{CC} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern

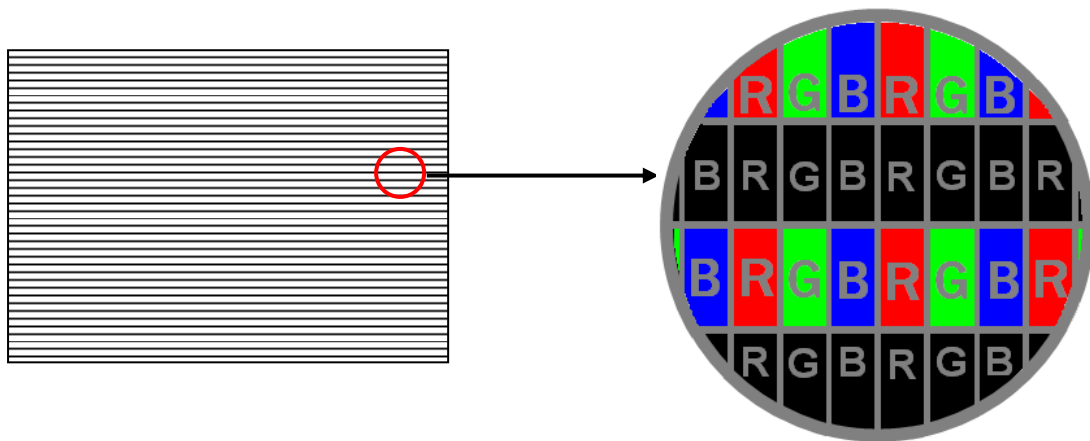


Active Area

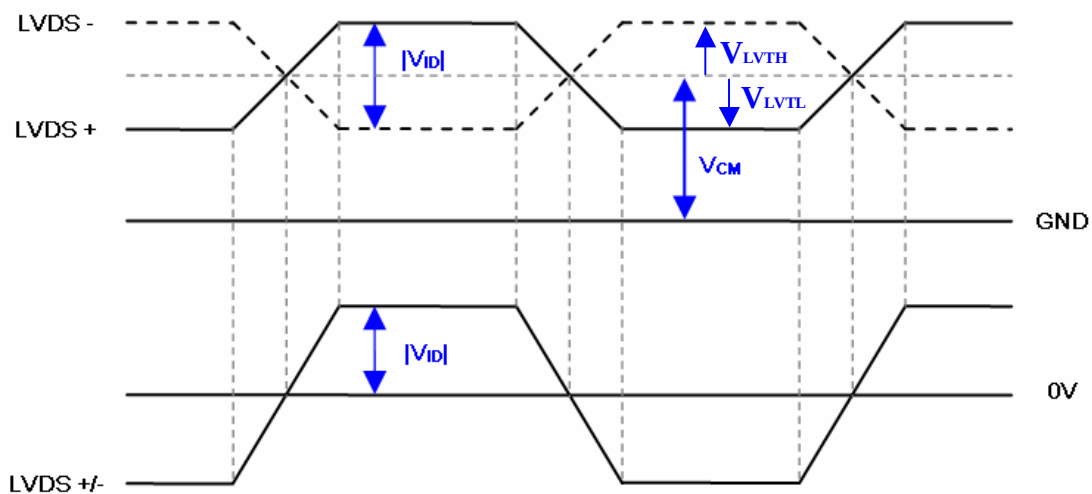
b. Black Pattern



Active Area

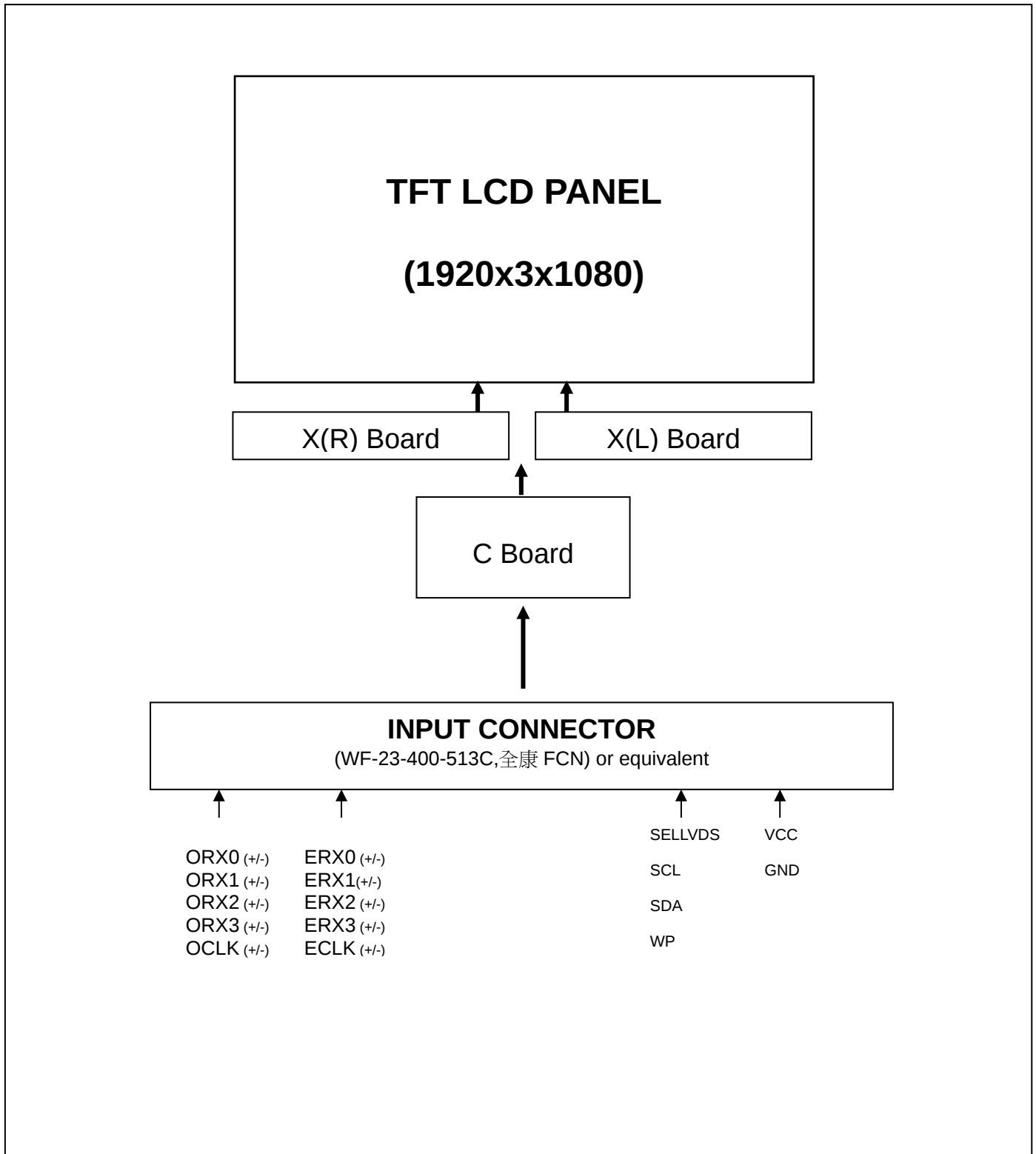


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 CNF1 Connector Part No.:

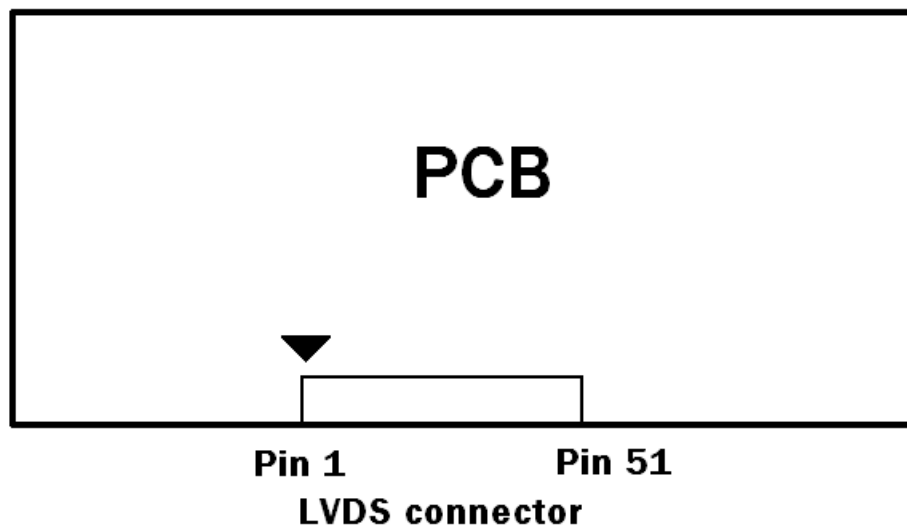
CNF1 Connector Part No.:全康(FCN) WF23-400-513C or equivalent.

Pin	Name	Description	Note
1	GND	Ground	
2	SCL	I2C clock (for auto Vcom)	
3	SDA	I2C data (for auto Vcom)	
4	N.C.	No Connection	(3)
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection (0V~0.7V/OPEN→VESA, 2.7V~3.3V→JEIDA) 【禁止Floating】	(4)(5)
8	N.C.	No Connection	(3)
9	N.C.	No Connection	
10	W.P	Write protection (0V~0.7V/Open→Disable, 2.7V~3.3V→Enable, for auto Vcom)	(7)
11	GND	Ground	
12	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(1)
13	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	Even pixel Negative LVDS differential clock input.	(1)
20	ECLK+	Even pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(1)
23	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(3)
25	N.C.	No Connection	
26	GND	Ground	
27	GND	Ground	
28	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(1)
29	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	Odd pixel Negative LVDS differential clock input.	(1)
36	OCLK+	Odd pixel Positive LVDS differential clock input.	
37	GND	Ground	(3)
38	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(1)
39	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	

40	N.C.	No Connection	
41	N.C.	No Connection	(3)
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(3)
48	Vin	Power input (+12V)	
49	Vin	Power input (+12V)	
50	Vin	Power input (+12V)	
51	Vin	Power input (+12V)	

Note (1) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

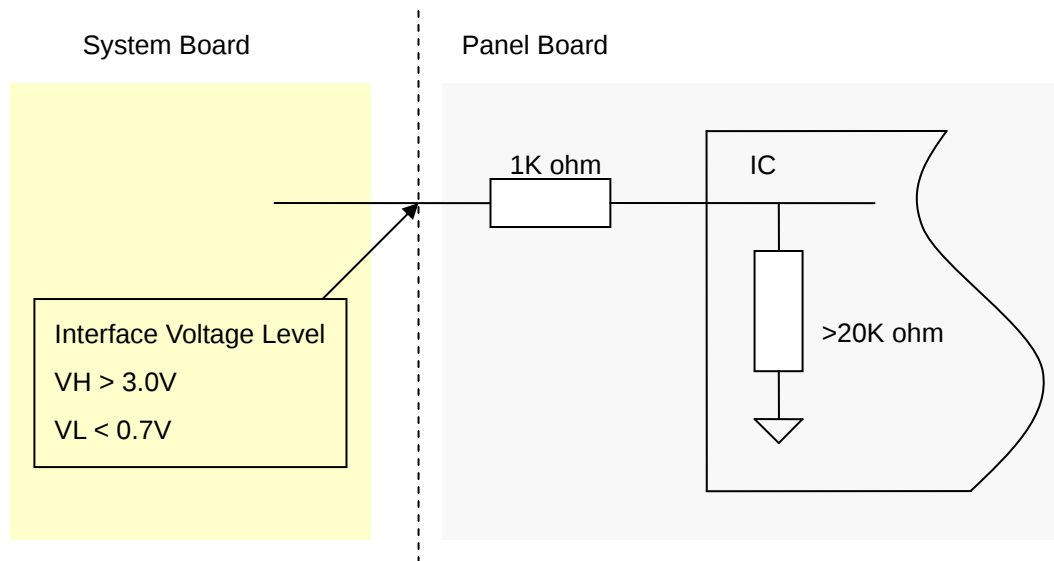
Note (2) LVDS connector pin order defined as follows



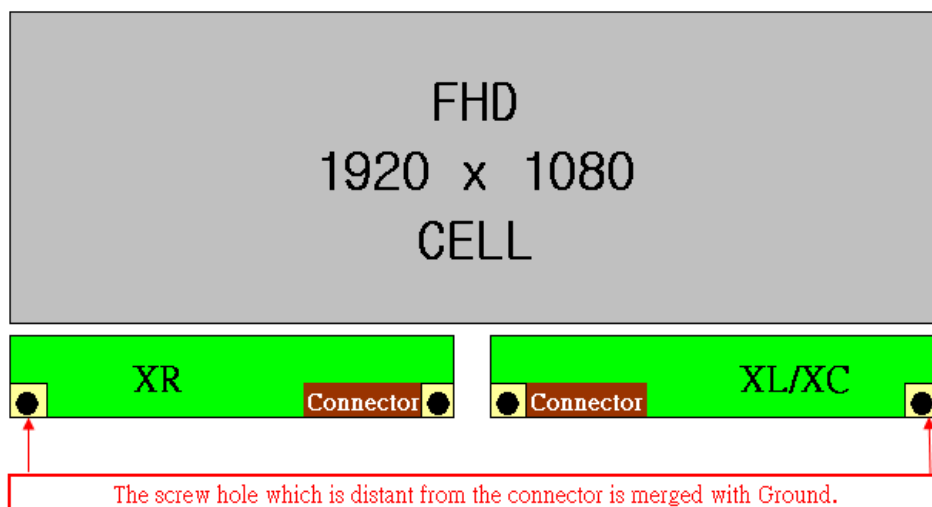
Note (3) Reserved for internal use. Please leave it open.

Note (4) Low = Open or connect to GND: VESA Format, High = Connect to +3.3V: JEIDA Format.

Note (5) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.

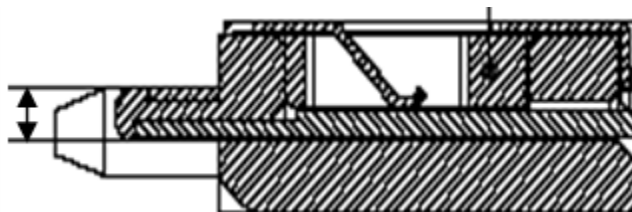


Note (6) The screw hole which is distant from the connector is merged with Ground.



Note (7) High=connect to +3.3V : Enable bus switch ; Low= connect to GND or Open : Disable bus switch for I2C bus isolation

Note (8) LVDS connector mating dimension range request is 0.93mm~1.0mm as follow:

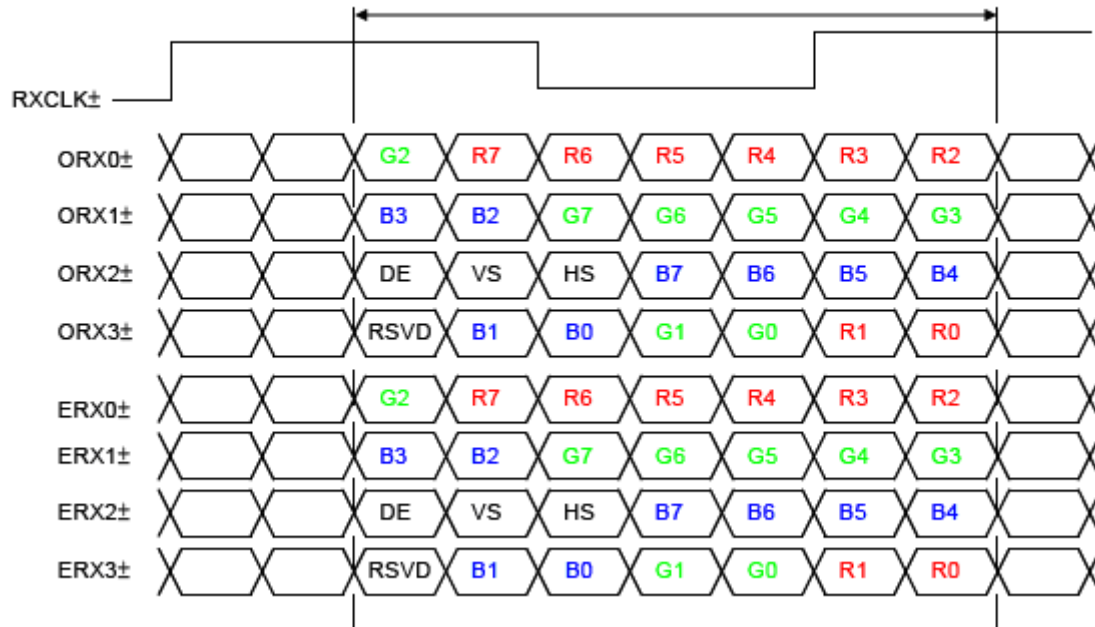


5.2 LVDS INTERFACE

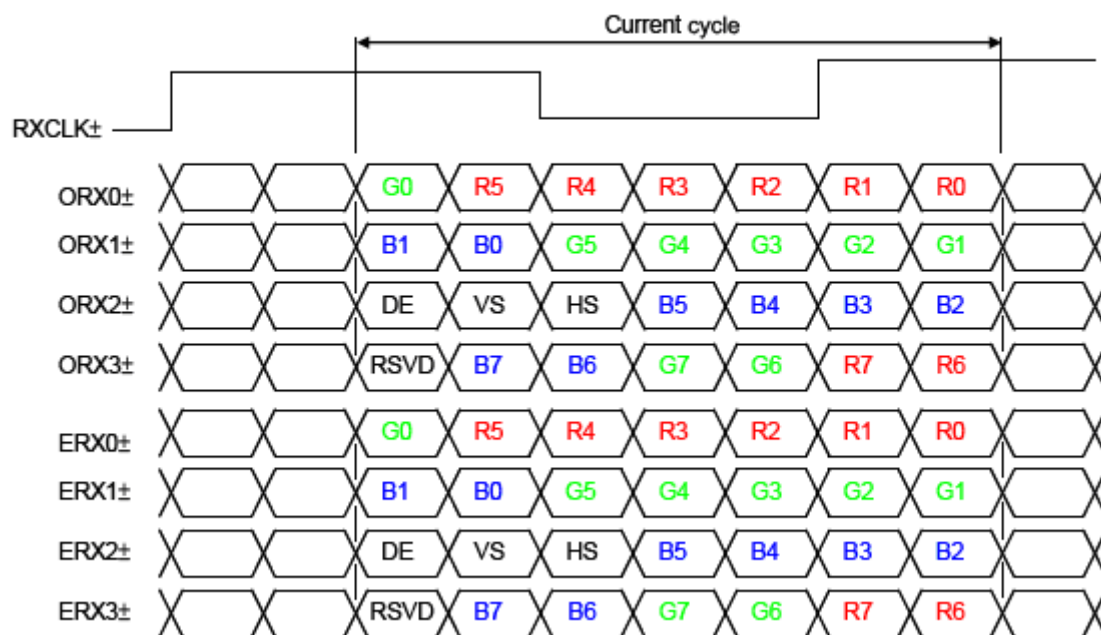
JEIDA Format : SELLVDS = H

VESA Format : SELLVDS = L or Open

JEDIA Format : SELLVDS=H



VESA Format : SELLVDS=L or Open



AR0~AR7: First Pixel R Data (7; MSB, 0; LSB)

AG0~AG7: First Pixel G Data (7; MSB, 0; LSB)

AB0~AB7: First Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSV : Reserved

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

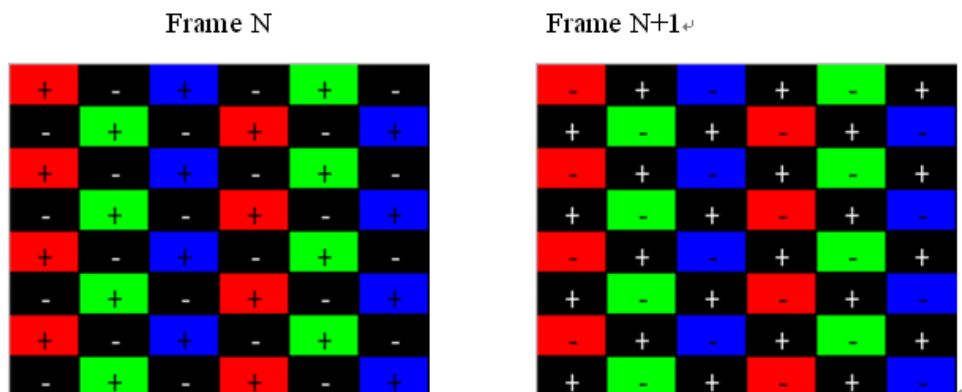
Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.4 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern:

Sub pixel on/off Pattern was shown as below. If customer need below pattern, please directly contact with Account FAE. (bright sub-pixel : G128 ; dark sub-pixel : G0)



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com. The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

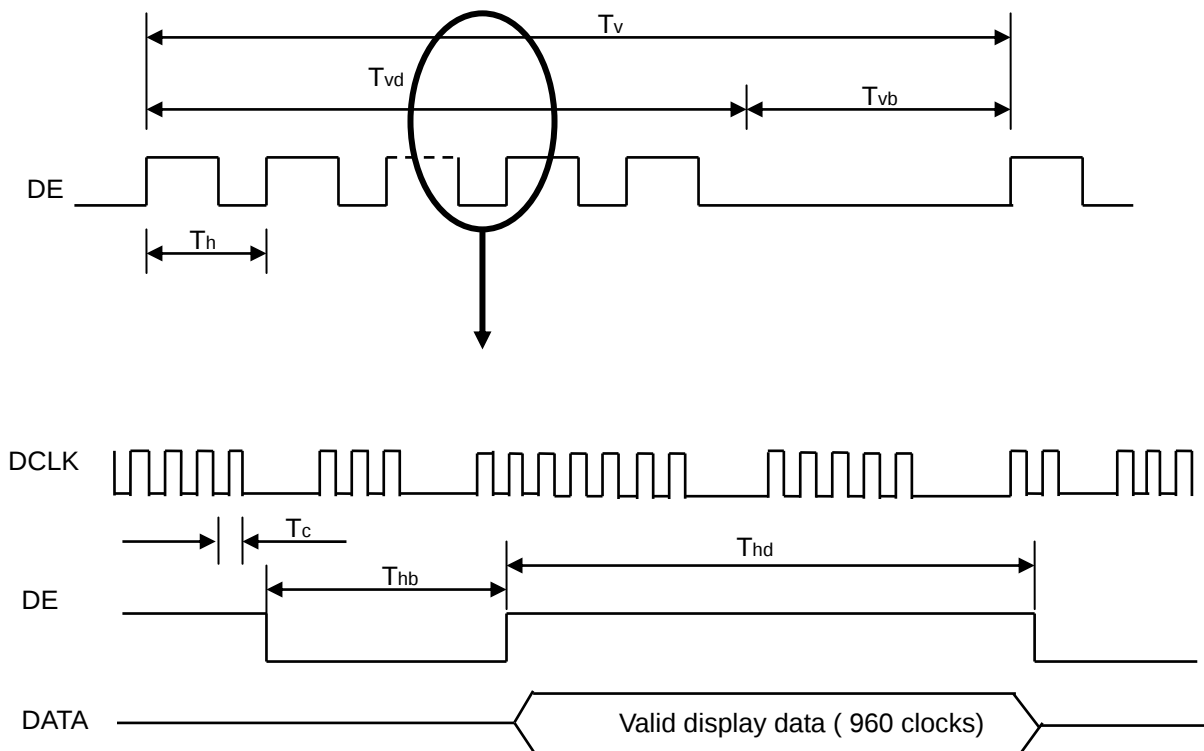
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{clk_{in}}$ (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{clk_{in_mod}}$	$F_{clk_{in}}-2\%$	—	$F_{clk_{in}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	-	400	ps	(5)
	Frame Rate	F_{r5}	—	50	—	Hz	
		F_{r6}	—	60	—	Hz	
	Total	T_v	1115	1125	1135	Th	$T_v=T_{vd}+T_{vb}$
	Display	T_{vd}	1080	1080	1080	Th	—
	Blank	T_{vb}	35	45	55	Th	—
Horizontal Active Display Term	Total	T_h	1030	1100	1325	Tc	$T_h=T_{hd}+T_{hb}$
	Display	T_{hd}	960	960	960	Tc	—
	Blank	T_{hb}	70	140	365	Tc	—

Note (1) Please make sure the range of pixel clock has follow the below equation :

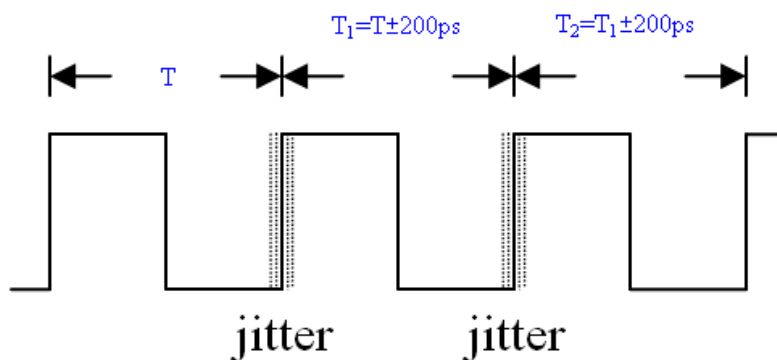
$$F_{clk_{in}(max)} \geq F_{r6} \times T_v \times T_h$$

$$F_{r5} \times T_v \times T_h \geq F_{clk_{in}(min)}$$

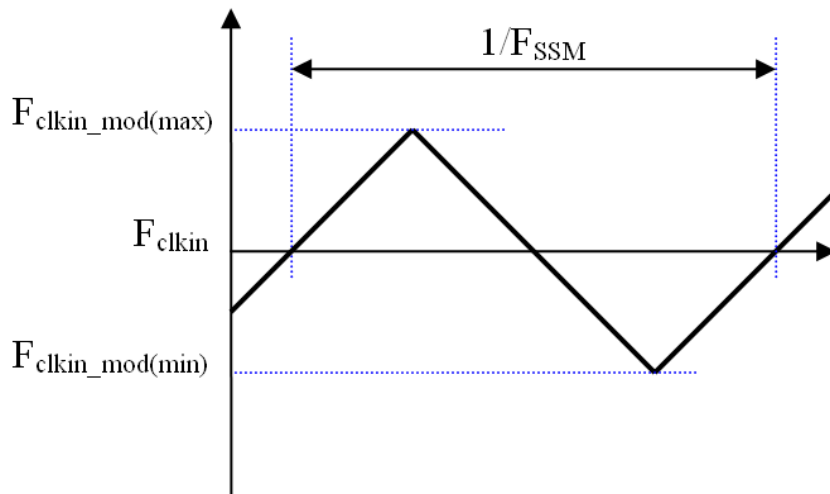
Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$

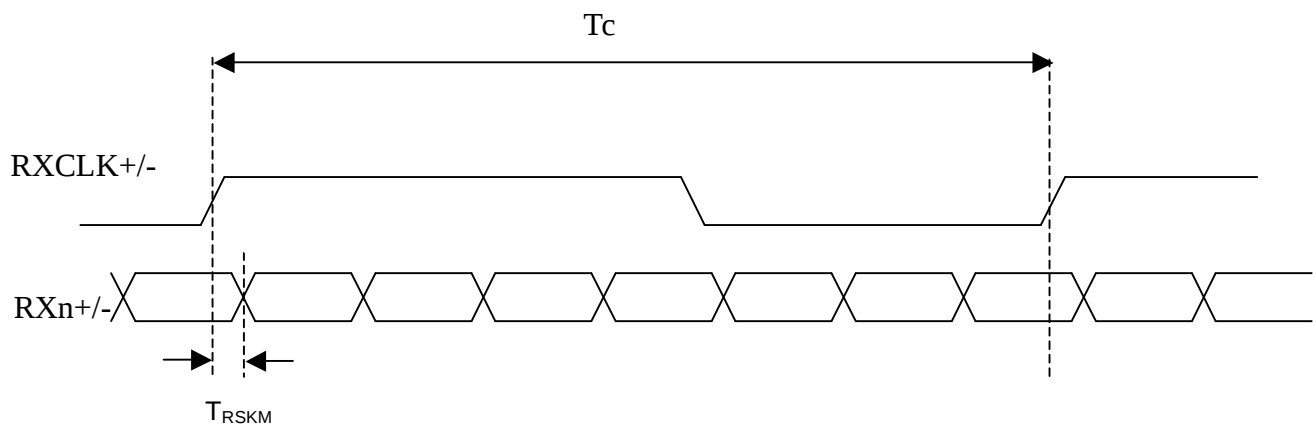


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

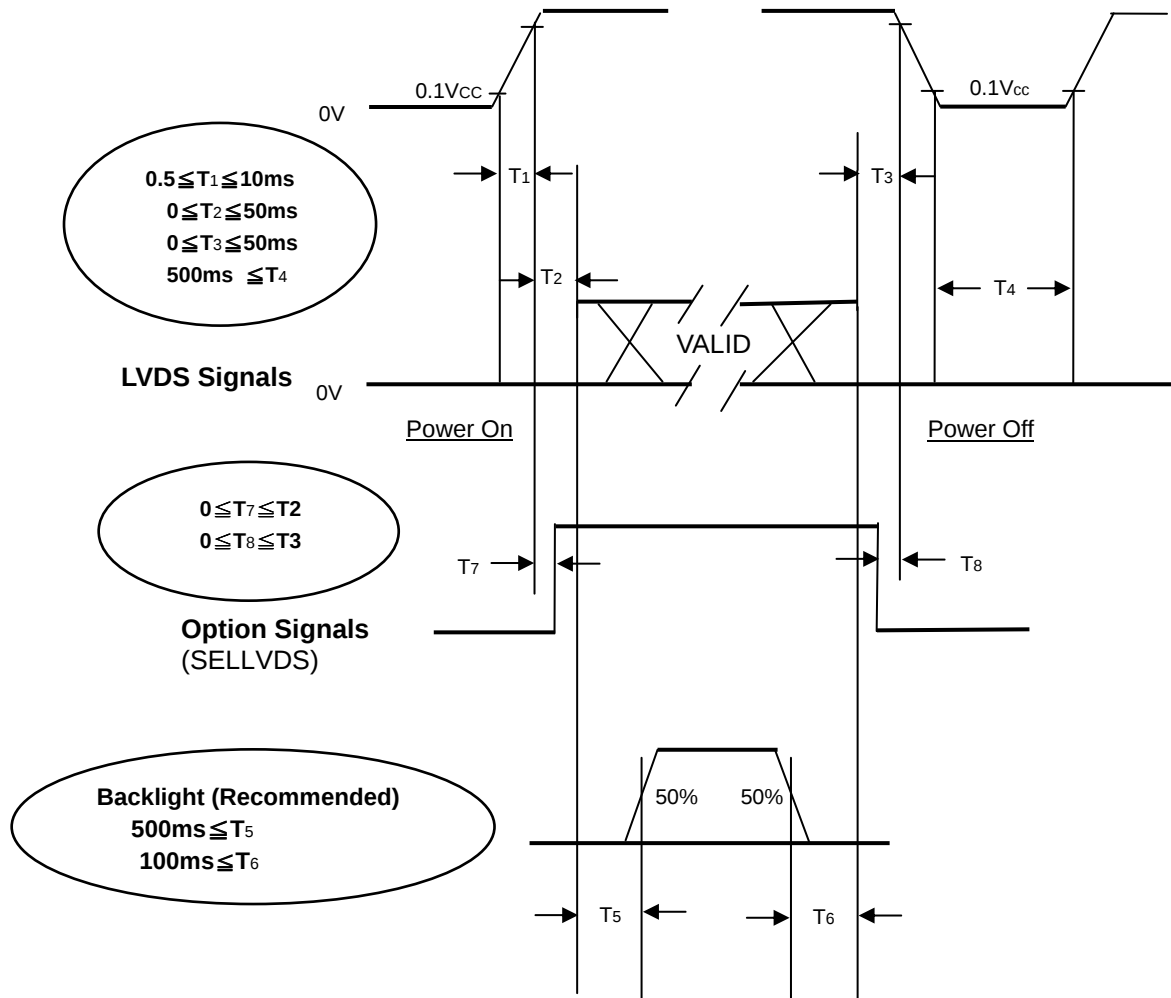
LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

($T_a = 25 \pm 2^\circ\text{C}$)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of V_{CC}.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of V_{CC} is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.

Note (4) T₄ should be measured after the module has been fully discharged between power off and on period.

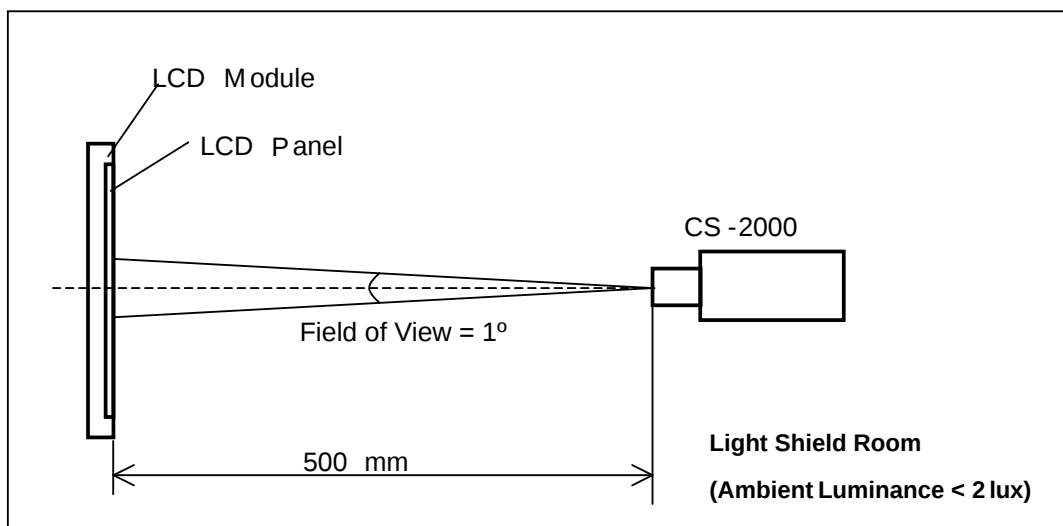
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I _L	16.5 ± 0.5	mA
Oscillating Frequency (Inverter)	F _w	40 ± 3	KHz
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Angle at Normal Direction Standard light source “C”	Typ. – 0.03	0.653	Typ+ 0.03	-	(0)
		Rcy			0.325		-	
	Green	Gcx			0.301		-	
		Gcy			0.597		-	
	Blue	Bcx			0.134		-	
		Bcy			0.110		-	
	White	Wcx			0.318		-	
		Wcy			0.360		-	
Center Transmittance		T%	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI module		5.7		%	(1),(6)
Contrast Ratio		CR		3500	5000	-	-	(1),(3)
Response Time		Gray to gray	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI Module@60Hz	-	9.5	19	ms	(1),(4)
White Variation		δW	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI module	-	-	1.3	-	(1),(5)
Viewing Angle	Horizontal	θ_{x+}	CR $\geq$ 20 with CMI module		88	-	Deg.	(1),(2)
		θ_{x-}			88	-		
	Vertical	θ_{Y+}			88	-		
		θ_{Y-}			88	-		

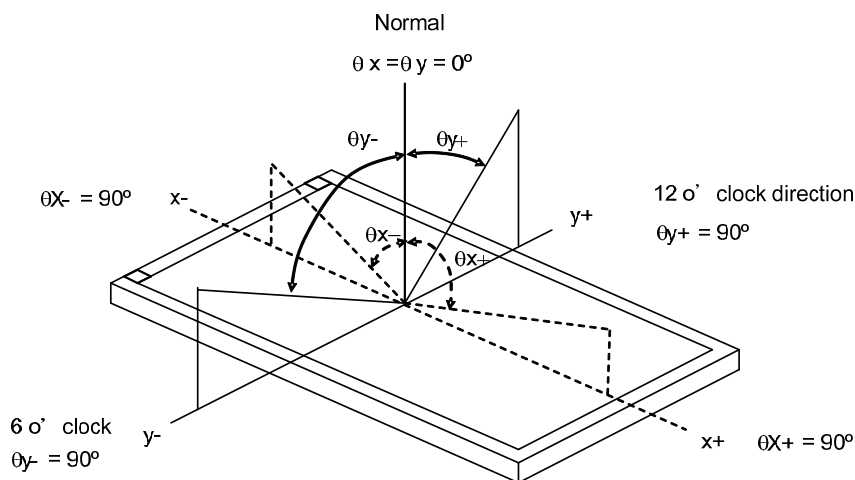
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's and BLU's spectrum at center point. White is without signal input and R,G,B are with signal input. BLU (for V420H2-L06) is supplied by CMO.
2. Measure Module's and BLU's spectrum at center point. W, R,G, B are with signal input. BLU (for V420H2-L06) is supplied by CMO.
3. Calculate cell's spectrum.
4. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θ_x , θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80. (or Eldim EZ-Contrast 160R)



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

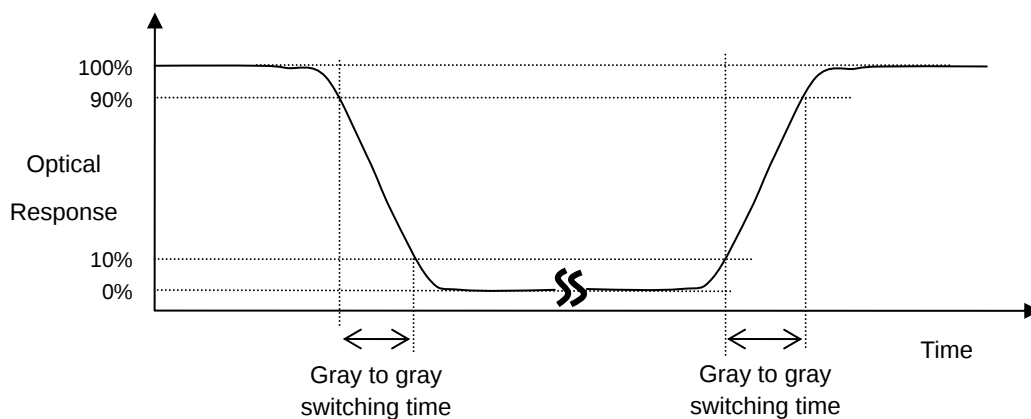
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (5).

Note (4) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

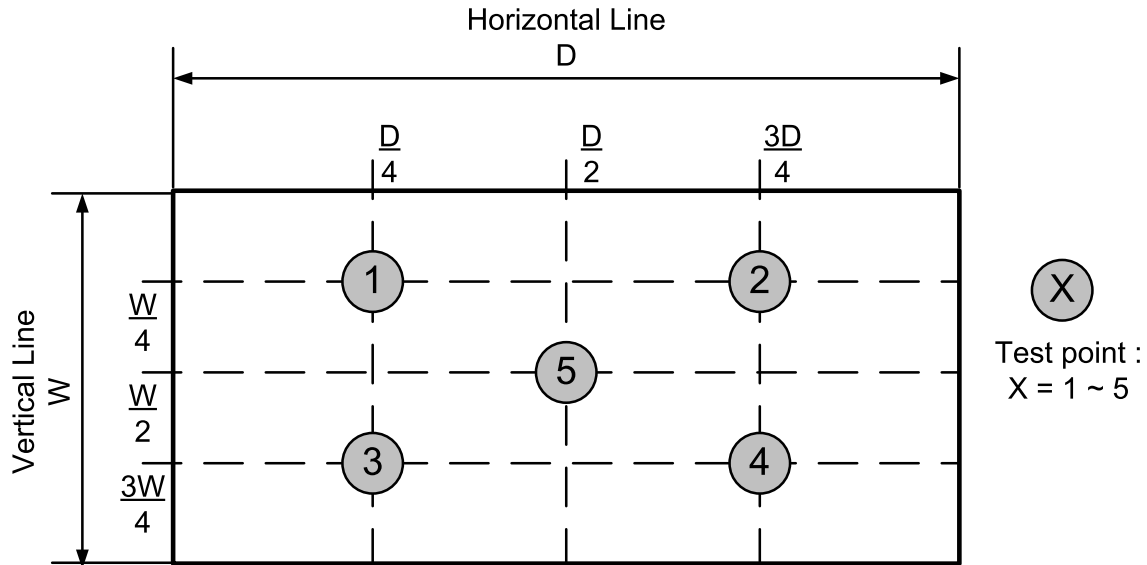
Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$

[Dino Hint: SEC and AUO are 9 points and the test point distance is $W/6$]



Note (6) Definition of Transmittance (T%) : (VA case)

Measure the luminance of gray level 255 at 5 points of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{average [L (1), L (2), L (3), L (4), L (5)] of LCD module}}{\text{average [L (1), L (2), L (3), L (4), L (5)] of backligh unit}} \times 100\%$$

The 5 point is corresponding of the point X at the figure in Note (5).

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [1] Do not apply rough force such as bending or twisting to the product during assembly.
- [2] To assemble backlight or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] It's not permitted to have pressure or impulse on the module because the LCD panel will be damaged.
- [4] Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- [5] Do not pull the I/F connector in or out while the module is operating.
- [6] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [7] It is dangerous that moisture come into or contacted the product, because moisture may damage the product when it is operating.
- [8] High temperature or humidity may reduce the performance of module. Please store this product within the specified storage conditions.
- [9] When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly.

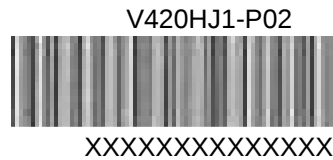
8.2 SAFETY PRECAUTIONS

- [1] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [2] After the product's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.



9.2 CARTON LABEL

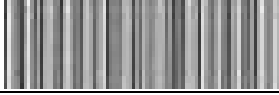
The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation

P.O. NO. _____

Parts ID. _____ Quantities _____

Model Name. _____

Carton ID. _____



XXXXXXXXXXXXXXXX

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

- (1) 12 LCD TV Panels / 1 Box
- (2) Box dimensions : 1110 (L) X 810 (W) X99 (H)mm
- (3) Weight : approximately 33Kg (12 panels per box)
- (4) 144 LCD TV Panels / 1 Group

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method.

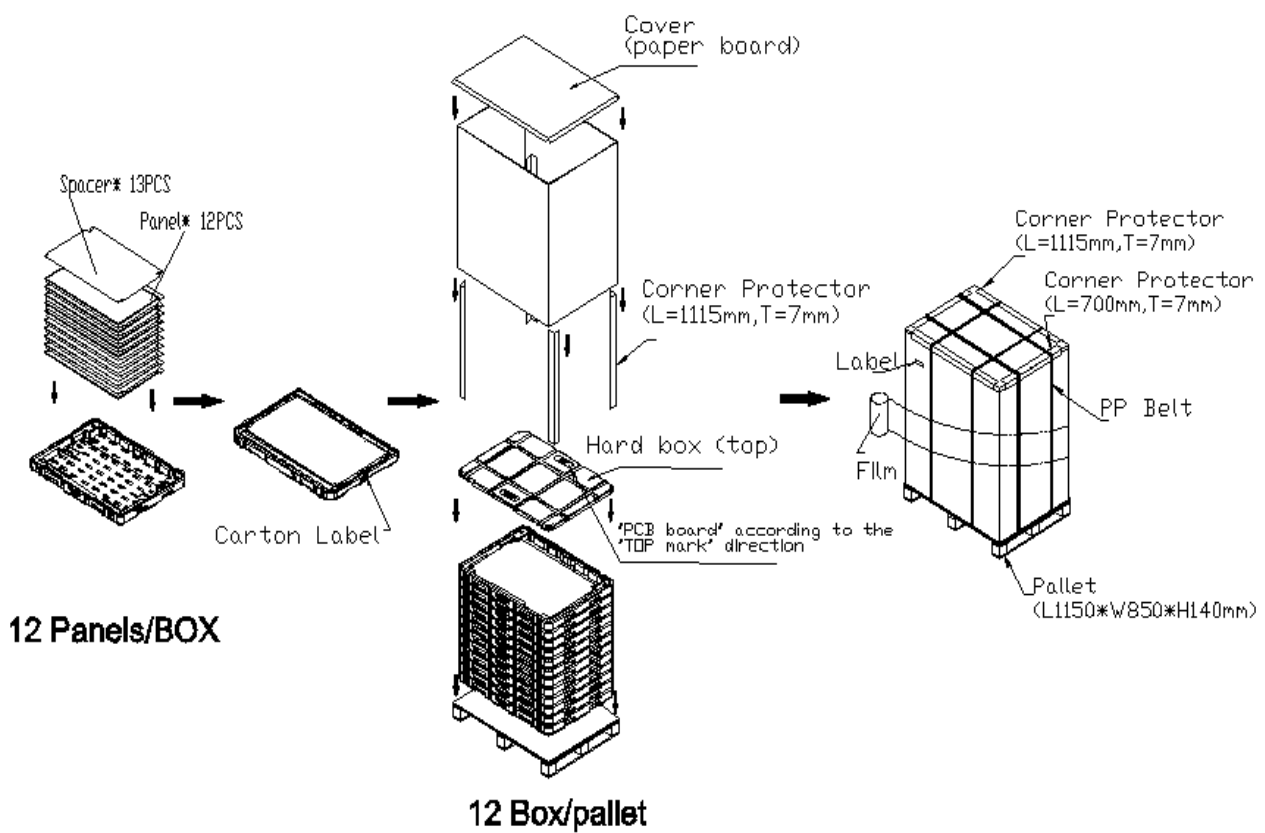


Figure.10-1 packing method

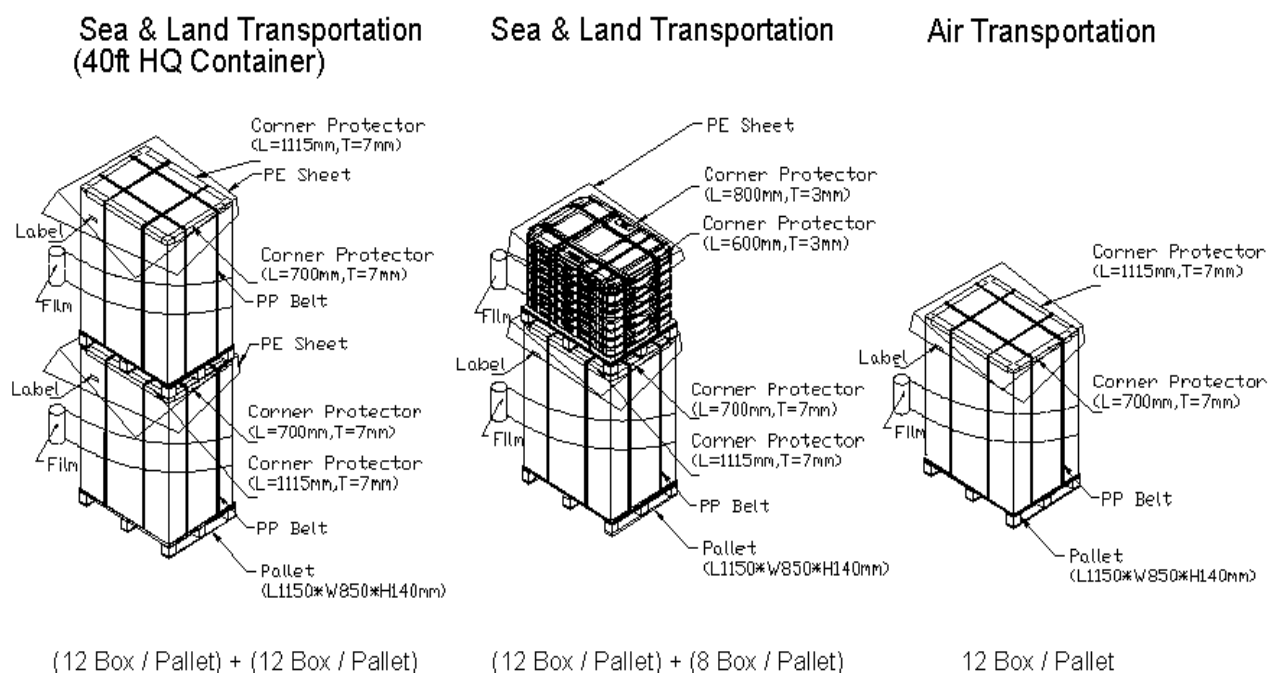


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTIC

