V43644R04V(C)TG-10PC
3.3 VOLT 4M x 64 HIGH PERFORMANCE PC100 UNBUFFERED SDRAM MODULE

Features

- 168 Pin Unbuffered 4,194,304 x 64 bit Oganization SDRAM Modules
- Utilizes High Performance 4M x 16 SDRAM in TSOPII-54 Packages
- Fully PC Board Layout Compatible to INTEL'S Rev 1.0 Module Specification
- Single +3.3V (± 0.3V) Power Supply
- Programmable $\overline{CAS}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All Inputs, Outputs are LVTTL Compatible
- 4096 Refresh Cycles every 64 ms
- Serial Present Detect (SPD)
- SDRAM Performance

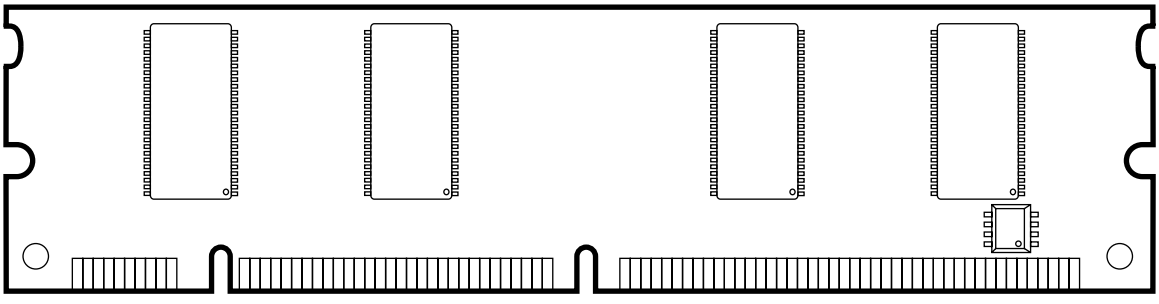
	Key Component Timing Parameters	-8PC	Units
t_{CK}	Clock Frequency (max.)	125	MHz
t_{AC}	Clock Access Time $\overline{CAS}$ Latency = 3	6	ns
t_{AC}	Latency = 2	6	ns

- Module Frequency vs AC Parameter

Frequency	CL ($\overline{CAS}$ Latency)	t_{RCD}	t_{RP}	t_{RC}	Unit
V43644R04V(C)TG-10PC 100 MHz (PC)	3	2	2	7	CLK
	2	2	2	7	CLK

Description

The V43644R04V(C)TG-10PC memory module is organized 4,194,304 x 64 bits in a 168 pin dual in line memory module (DIMM). The 4M x 64 memory module uses 4 Mosel-Vitelic 4M x 16 SDRAM. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.



V43644R04V(C)TG-10PC-01

Pin Configurations (Front Side/Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	I/O19	85	VSS	113	DQM5	141	I/O51
2	I/O1	30	$\overline{CS0}$	58	I/O20	86	I/O33	114	$\overline{CS1}$	142	I/O52
3	I/O2	31	DU	59	VCC	87	I/O34	115	RAS	143	VCC
4	I/O3	32	VSS	60	I/O21	88	I/O35	116	VSS	144	I/O53
5	I/O4	33	A0	61	NC	89	I/O36	117	A1	145	NC
6	VCC	34	A2	62	DU	90	VCC	118	A3	146	DU
7	I/O5	35	A4	63	CKE1	91	I/O37	119	A5	147	NC
8	I/O6	36	A6	64	VSS	92	I/O38	120	A7	148	VSS
9	I/O7	37	A8	65	I/O22	93	I/O39	121	A9	149	I/O54
10	I/O8	38	A10(AP)	66	I/O23	94	I/O40	122	BA0	150	I/O55
11	I/O9	39	BA1	67	I/O24	95	I/O41	123	A11	151	I/O56
12	VSS	40	VCC	68	VSS	96	VSS	124	VCC	152	VSS
13	I/O10	41	VCC	69	I/O25	97	I/O42	125	CLK1	153	I/O57
14	I/O11	42	CLK0	70	I/O26	98	I/O43	126	NC	154	I/O58
15	I/O12	43	VSS	71	I/O27	99	I/O44	127	VSS	155	I/O59
16	I/O13	44	DU	72	I/O28	100	I/O45	128	CKE0	156	I/O60
17	I/O14	45	$\overline{CS2}$	73	VCC	101	I/O46	129	$\overline{CS3}$	157	VCC
18	VCC	46	DQM2	74	I/O29	102	VCC	130	DQM6	158	I/O61
19	I/O15	47	DQM3	75	I/O30	103	I/O47	131	DQM7	159	I/O62
20	I/O16	48	DU	76	I/O31	104	I/O48	132	DU	160	I/O63
21	CBO*	49	VCC	77	I/O32	105	CB4*	133	VCC	161	I/O64
22	CB1*	50	NC	78	VSS	106	CB5*	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	CB2*	80	NC	108	NC	136	CB6*	164	NC
25	NC	53	CB3*	81	WP	109	NC	137	CB7*	165	SA0
26	VCC	54	VSS	82	SDA	110	VCC	138	VSS	166	SA1
27	$\overline{WE}$	55	I/O17	83	SCL	111	CAS	139	I/O49	167	SA2
28	DQM0	56	I/O18	84	VCC	112	DQM4	140	I/O50	168	VCC

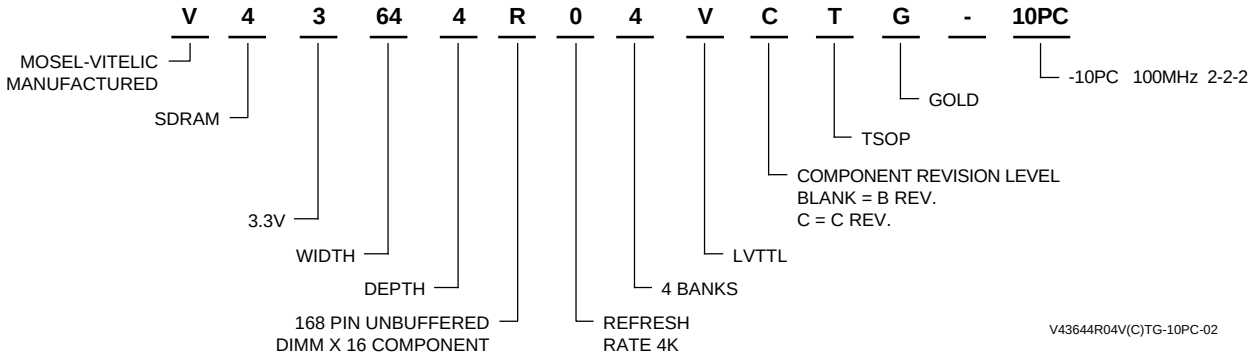
Notes:
* These pins are not used in this module.

Pin Names

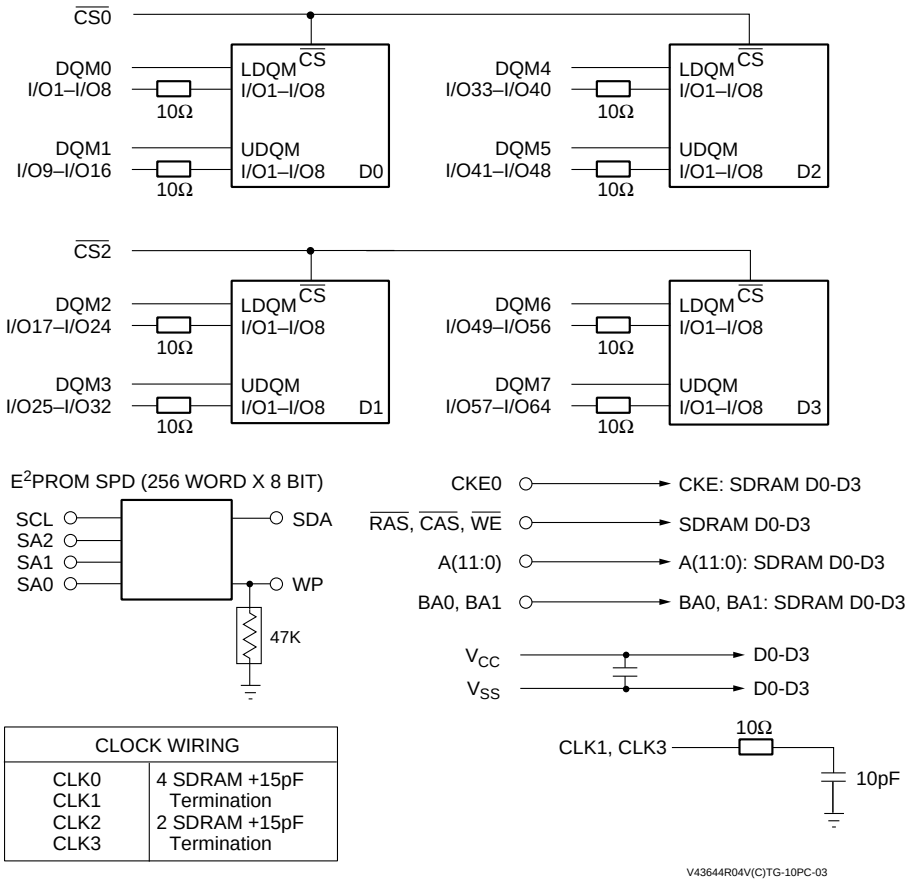
A0–A11	Address Inputs
I/O1–I/O64	Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
BA0, BA1	Bank Selects
$\overline{CKE0}$, $\overline{CKE1}$	Clock Enable
$\overline{CS0}$–$\overline{CS3}$	Chip Select
CLK0–CLK3	Clock Input
DQM0–DQM7	Data Mask
VCC	Power (+3.3 Volts)
VSS	Ground
SCL	Clock for Presence Detect

SDA	Serial Data OUT for Presence Detect
SA0–A2	Serial Data IN for Presence Detect
CB0–CB7	Check Bits (x72 Organization)
NC	No Connection
DU	Don't Use

Part Number Information



Block Diagram



CLOCK WIRING	
CLK0	4 SDRAM +15pF Termination
CLK1	
CLK2	2 SDRAM +15pF Termination
CLK3	

Serial Presence Detect Information

A serial presence detect storage device - E^2PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus)

SPD-Table:

Byte Number	Function Described	SPD Entry Value	Hex Value
			100 MHz -10PC
0	Number of SPD bytes	128	80
1	Total bytes in Serial PD	256	08
2	Memory Type	SDRAM	04
3	Number of Row Addresses (without BS bits)	12	0C
4	Number of Column Addresses (for x16 SDRAM)	8	08
5	Number of DIMM Banks	1	01
6	Module Data Width	64	40
7	Module Data Width (continued)	0	00
8	Module Interface Levels	LVTTL	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0
10	SDRAM Access Time from Clock at CL=3	6.0 ns	60
11	Dimm Config (Error Det/Corr.)	none	00
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80
13	SDRAM width, Primary	x16	10
14	Error Checking SDRAM Data Width	n/a / x8	00
15	Minimum Clock Delay from Back to Back Random Column Address	t_{ccd} = 1 CLK	01
16	Burst Length Supported	1, 2, 4, 8 & full Page	8F
17	Number of SDRAM Banks	4	04
18	Supported $\overline{CAS}$ Latencies	CL = 2 & 3	06
19	$\overline{CS}$ Latencies	$\overline{CS}$ Latency = 0	01
20	$\overline{WE}$ Latencies	WL = 0	01
21	SDRAM DIMM Module Attributes	Non Buffered/Non Reg.	00
22	SDRAM Device Attributes: General	Vcc tol ± 10%	0E
23	Minimum Clock Cycle Time at $\overline{CAS}$ Latency = 2	10.0 ns	A0
24	Maximum Data Access Time from Clock for CL = 2	6.0 ns	60
25	Minimum Clock Cycle Time at CL = 1	Not Supported	00
26	Maximum Data Access Time from Clock at CL = 1	Not Supported	00
27	Minimum Row Precharge Time t_{RP}	20 ns	14
28	Minimum Row Active to Row Active Delay t_{RRD}	16 ns	10
29	Minimum RAS to $\overline{CAS}$ Delay t_{RCD}	20 ns	14

SPD-Table: (Continued)

Byte Number	Function Described	SPD Entry Value	Hex Value 100 MHz -10PC
30	Minimum RAS Pulse Width t_{RAS}	45 ns	2D
31	Module Bank Density (Per Bank)	32 M	08
32	SDRAM Input Setup Time	2 ns	20
33	SDRAM Input Hold Time	1 ns	10
34	SDRAM Data Input Setup Time	2 ns	20
35	SDRAM Data Input Hold Time	1 ns	10
36-61	Superset Information (May be used in Future)		00
62	SPD Revision	Revision 1.2	12
63	Checksum for Bytes 0 - 62		FD
64-125	Manufacturers's Information (Optional) (FFh if not used)		XX
126	Max. Frequency Specification	100 MHz	64
127	100 MHz Support Details		AF
128+	Unused Storage Location		00

DC Characteristics

T_A = 0°C to 70°C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3V ± 0.3V

Symbol	Parameter	Limit Values Min.	Limit Values Max.	Unit
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	–0.5	0.8	V
V_{OH}	Output High Voltage (I_{OUT} = –2.0 mA)	2.4	—	V
V_{OL}	Output Low Voltage (I_{OUT} = 2.0 mA)	—	0.4	V
$I_{I(L)}$	Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0V)	–40	40	µA
$I_{O(L)}$	Output leakage current (DQ is disabled, 0V < V_{OUT} < V_{CC})	–40	40	µA

Capacitance

T_A = 0°C to 70°C; V_{DD} = 3.3V ± 0.3V, f = 1 MHz

Symbol	Parameter	Limit Values	Unit
C_{I1}	Input Capacitance (A0 to A11, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	45	pF
C_{I2}	Input Capacitance ($\overline{CS0}$-$\overline{CS3}$)	20	pF
C_{ICL}	Input Capacitance (CLK0-CLK3)	22	pF
C_{I3}	Input Capacitance (CKE0, CKE1)	22	pF
C_{I4}	Input Capacitance (DQM0-DQM7)	13	pF
C_{IO}	Input/Output Capacitance (I/O1-I/064)	13	pF
C_{SC}	Input Capacitance (SCL, SA0-2)	8	pF
C_{SD}	Input/Output Capacitance	10	pF

Standby and Refresh Currents[1]

T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions	4M x 64	Unit	Note
$I_{CC}1$	Operating Current	Burst length = 4, CL = 3 t_{RC}> = t_{RC}(min), t_{CK}> = t_{CK}(min), IO = 0 mA 2 Bank Interleave Operation	440	mA	1,2
$I_{CC}2P$	Precharged Standby Current in Power Down Mode	CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)	12	mA	
$I_{CC}2PS$		CKE< = V_{IL}(max), t_{CK} = Infinite	8	mA	
$I_{CC}2N$	Precharged Standby Current in Non-Power Down Mode	CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed once in 3 cycles	200	mA	$\overline{CS}$ = High
$I_{CC}2NS$		CKE> = V_{IH}(min), t_{CK} = Infinite, No Input change	20	mA	
$I_{CC}3P$	Active Standby Current in Power Down Mode	CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)	32	mA	
$I_{CC}3PS$		CKE< = V_{IL}(max), t_{CK} = Infinite	16	mA	
$I_{CC}3N$	Active Standby Current in Non-Power Down Mode	CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed one time	120	mA	$\overline{CS}$ = High
$I_{CC}3NS$		CKE> = V_{IH}(min), t_{CK} = Infinite, No Input change	80	mA	
$I_{CC}4$	Burst Operating Current	Burst length = Full Page, t_{RC} = Infinite, CL = 3, t_{CK}> = t_{CK}(min), IO = 0 mA 2 Banks Activated	620	mA	1, 2
$I_{CC}5$	Auto Refresh Current	t_{RC}>= t_{RC}(min)	520	mA	1,2
$I_{CC}6$	Self Refresh Current	CKE = <0,2 V	8	mA	1,2

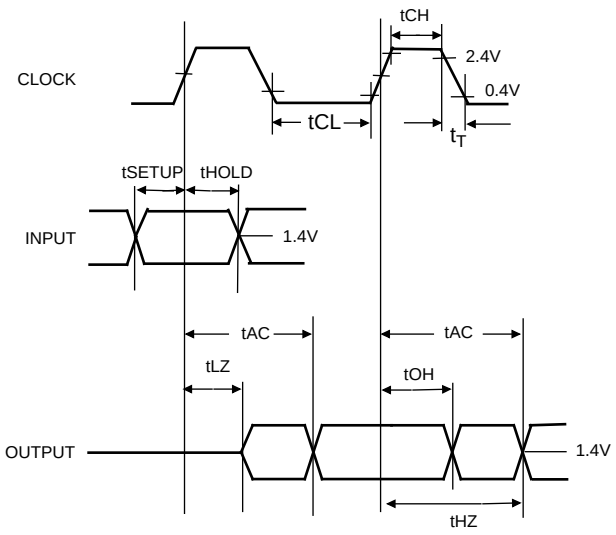
AC Characteristics [3,4]

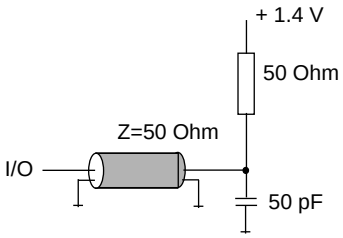
T_A = 0° to 70°C; V_{SS} = 0V; V_{CC} = 3.3V ± 0.3V, t_T = 1 ns

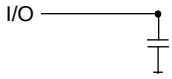
#	Symbol	Parameter	Limit Values -10PC Min.	Limit Values -10PC Max.	Unit	Note
Clock and Clock Enable						
1	t_{CK}	Clock Cycle Time $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 10 10		 ns ns	
2	f_{CK}	System frequency $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 – –	 100 100	 MHz MHz	
3	t_{AC}	Clock Access Time $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 – –	 6 6	 ns ns	4,5
4	t_{CH}	Clock High Pulse Width	3	–	ns	6
5	t_{CL}	Clock Low Pulse Width	3	–	ns	6
6	t_{CS}	Input Setup time	2	–	ns	7
7	t_{CH}	Input Hold Time	1	–	ns	7
8	t_{CKSP}	CKE Setup Time (Power down mode)	2.5	–	ns	8
9	t_{CKSR}	CKE Setup Time (Self Refresh Exit)	8	–	ns	9
10	t_T	Transition time (rise and fall)	1	–	ns	
Common Parameters						
11	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	20	–	ns	
12	t_{RC}	Cycle Time	70	120k	ns	
13	t_{RAS}	Active Command Period	45	–	ns	
14	t_{RP}	Precharge Time	20	–	ns	
15	t_{RRD}	Bank to Bank Delay Time	16	–	ns	
16	t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	1	–	CLK	
Refresh Cycle						
17	t_{SREX}	Self Refresh Exit Time	10	–	ns	9
18	t_{REF}	Refresh Period (4096 cycles)	64	–	ms	8
Read Cycle						
19	t_{OH}	Data Out Hold Time	3	–	ns	4
20	t_{LZ}	Data Out to Low Impedance Time	0	–	ns	
21	t_{HZ}	Data Out to High Impedance Time	3	9	ns	10
22	t_{DQZ}	DQM Data Out Disable Latency	2	–	CLK	
Write Cycle						
23	t_{DPL}	Data input to Precharge (write recovery)	2	–	CLK	
24	t_{DAL}	Data In to Active/refresh	5	–	CLK	11
25	t_{DQW}	DQM Write Mask Latency	0	–	CLK	

Notes:

1. The specified values are valid when addresses are changed no more than once during t_{CK}(min.) and when No Operation commands are registered on every rising clock edge during t_{RC}(min). Values are shown per module bank.
2. The specified values are valid when data inputs (DQ's) are stable during t_{RC}(min.).
3. All AC characteristics are shown for device level.
   An initial pause of 100 µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have V_{IL} = 0.4V and V_{IH} = 2.4V with the timing referenced to the 1.4V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown. Specific tac and toh parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0V.





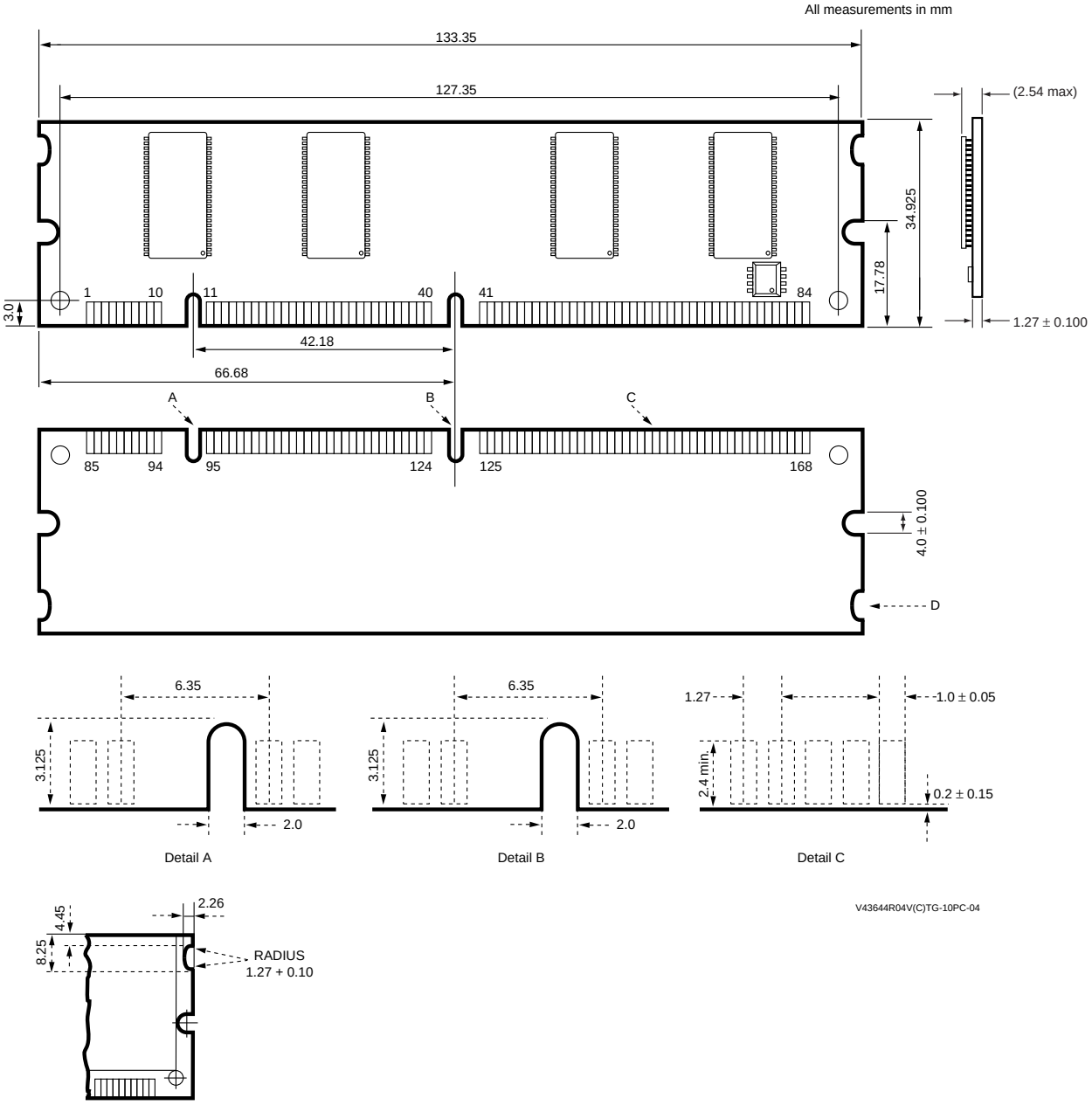


Measurement conditions for tac and toh

5. If clock rising time is longer than 1 ns, a time (t_T/2 -0.5) ns has to be added to this parameter.
6. Rated at 1.5V
7. If t_T is longer than 1 ns, a time (t_T -1) ns has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
11. t_{DAL} is equivalent to t_{DPL} + t_{RP}.

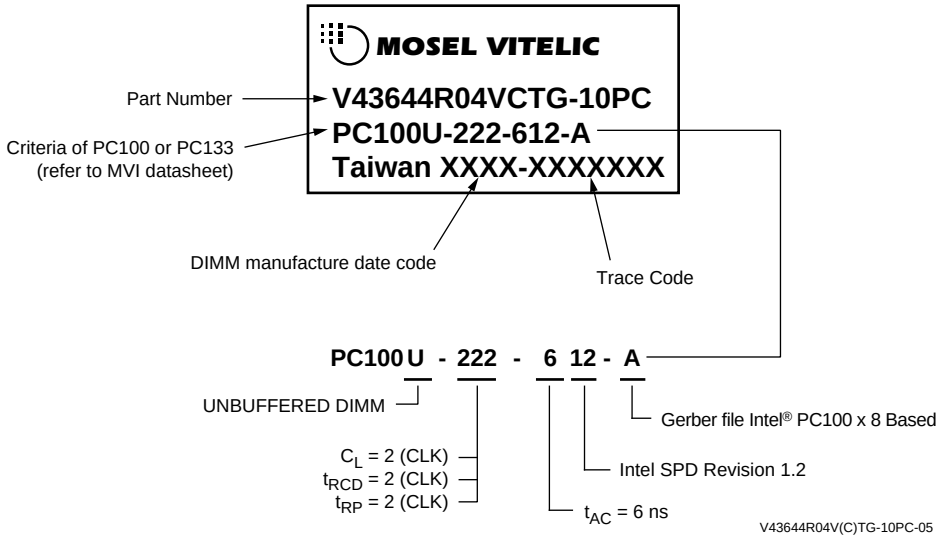
Package Diagram

SDRAM DIMM Module Package



Tolerances: ± (0.13) unless otherwise specified.

Label Information



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