TFT LCD Approval Specification

MODEL NO.: V460H1 - LH7

Customer: _____

Approved by: _____

Note:

Approved By	TV Product Marketing & Management Div
	Chao-Chun Chung

Reviewed By	QA Dept.	Product Development Div.
	Hsin-Nan Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	Josh Chi	Lynn Cheng

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Nov. 19,'09	All	All	Approval Specification was first issued.
Ver 2.1	Dec. 21,'09	34,35,36	9	The packing information was verified. - Box Dimensions : 1175(L)x 282(W)x 725(H)mm - Container Dimenions : see Figure. 9-2

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V460H1-LH7 is a 46" TFT Liquid Crystal Display module with 14-CCFL Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 full HDTV format and can display true 1.073G colors (8bit+Hi-FRC -bit/color). The balance board module for backlight is built-in.

1.2 FEATURES

- High brightness (500nits)
- High contrast ratio (6500:1)
- Fast response time (Gray to Gray average 4.5 ms)
- High color saturation (72% NTSC)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 100/120 Hz frame rate
- Ultra wide viewing angle: Super MVA technology

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1018.08(H) x 572.67(V) (46" diagonal)	mm	(1)
Bezel Opening Area	1024.4(H) x 579.2(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.17675(H) x 0.53025(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.073G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Glare coating, Hardness (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	-	1083	-	mm	(1), (2)
	Vertical (V)	-	627	-	mm	
	Depth (D)	-	53.8	-	mm	
Weight		-	13020	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	T_{ST}		-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}		0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	50	G	(3), (5)
		Z axis	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

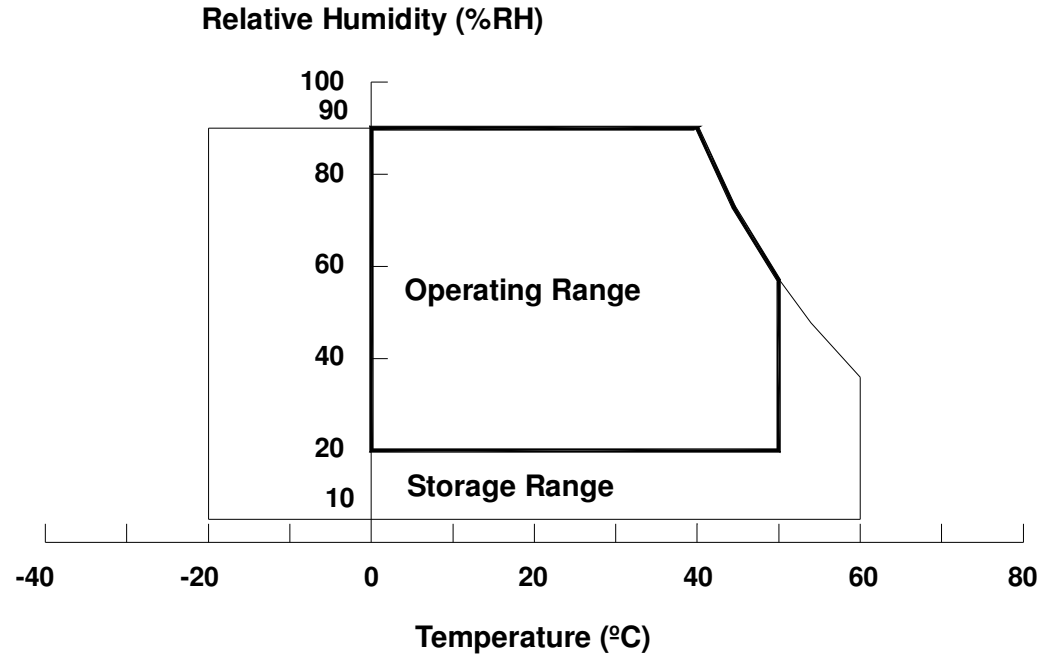
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, and ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

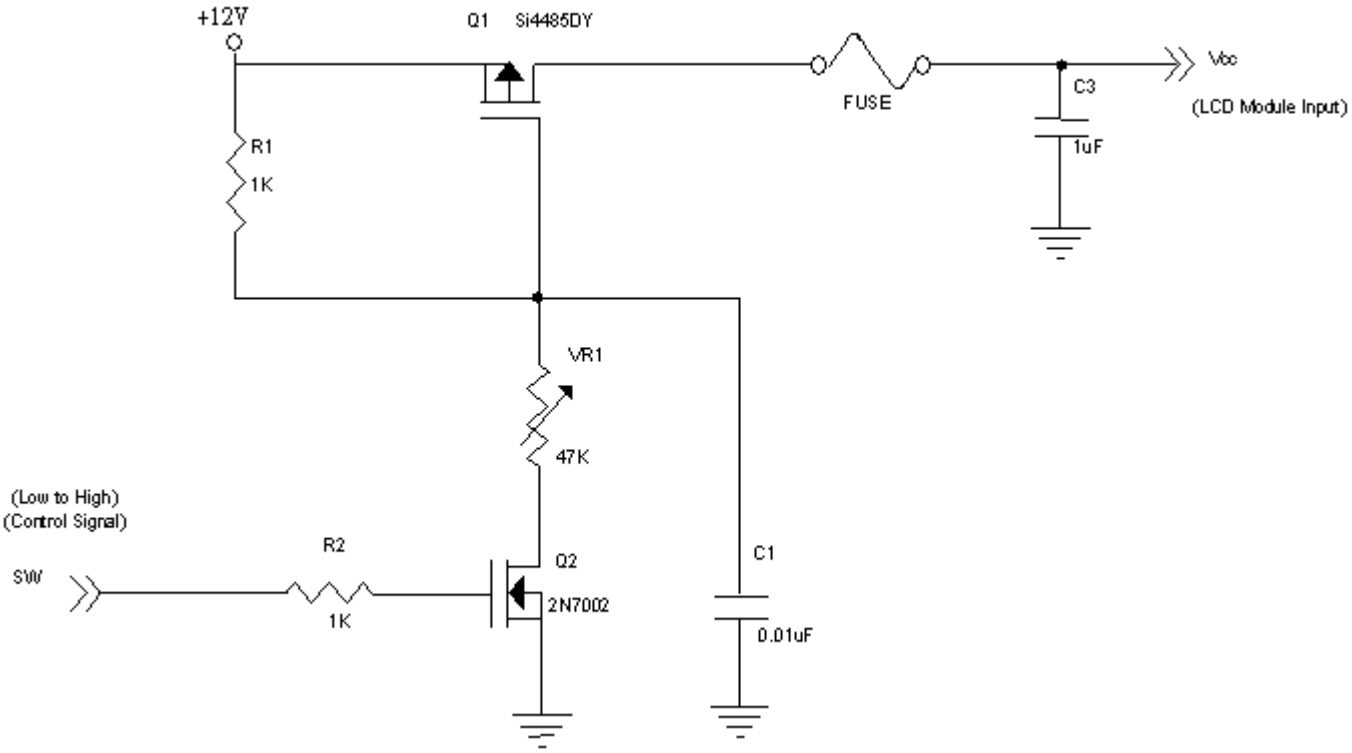
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE (Ta = 25 ± 2 ºC)

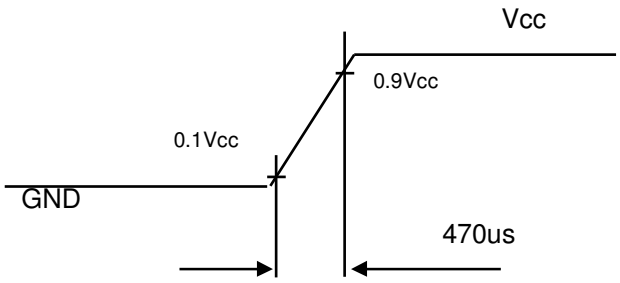
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	5	A	(2)
Power Supply Current	White Pattern	-	-	0.51	0.663	A	(3)
	Horizontal Stripe	-	-	0.98	1.274	A	
	Black Pattern	-	-	0.45	0.585	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

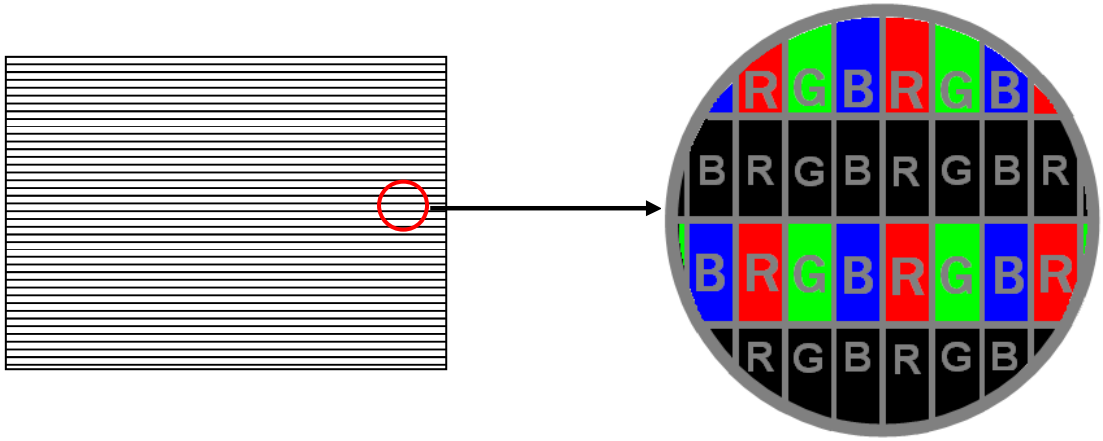
a. White Pattern

Active Area

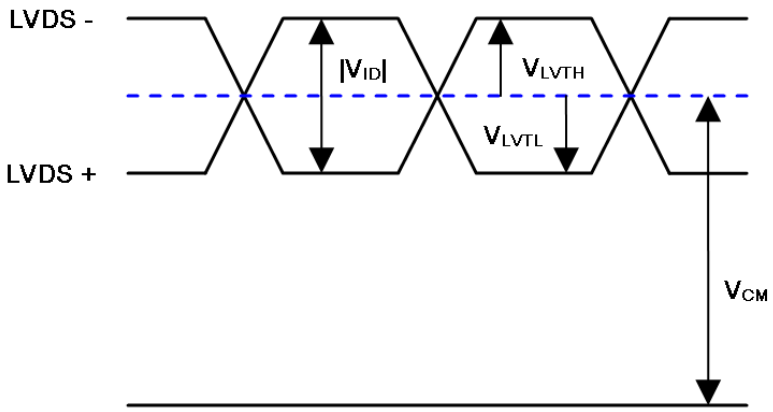
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1050	-	V_{RMS}	-
Lamp Current	I_L	11.5	12.0	12.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	1820	V_{RMS}	(2), Ta = 0 ºC
		-	-	1650	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_L	30	-	80	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.:

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2 ℃ and I_L = 11.5~12.5 mArms.

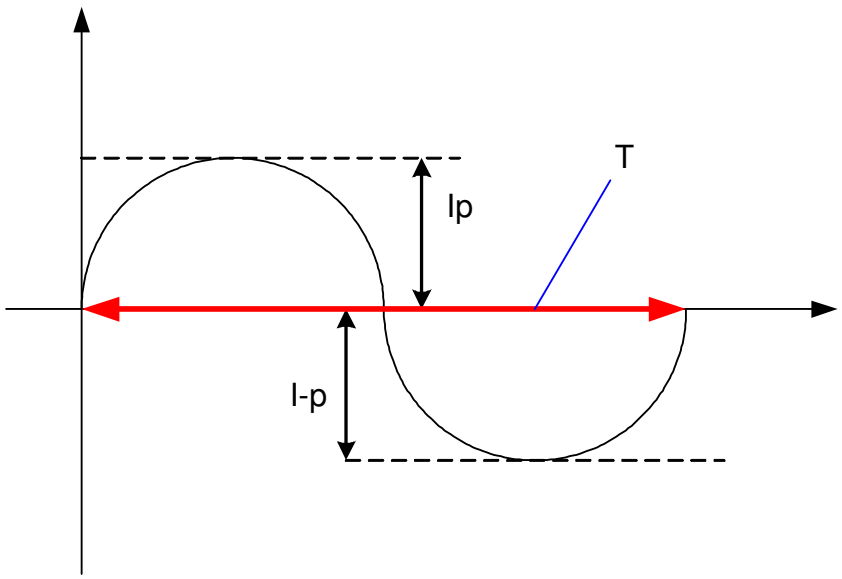
3.2.2 BALANCE BOARD CHARACTERISTICS (Ta = 25 ± 2 ºC)

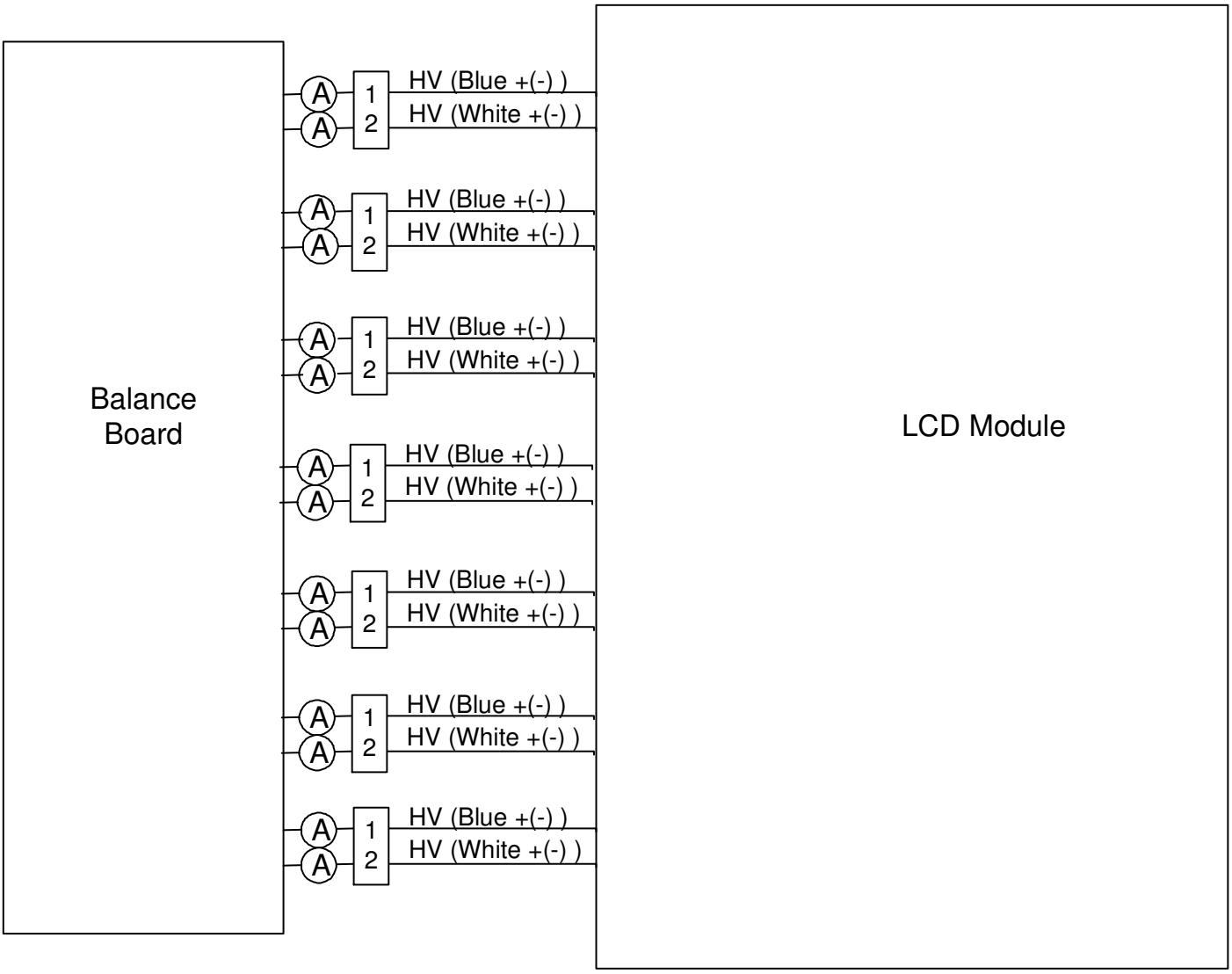
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Input High Voltage		V_{HV}	-	1050	-	V	(6)
Protection Circuit Supply Voltage		Vcc	10	12	15	V	
Input Current		$I_{BL(HV)}$		168		mArms	No Dimming
Oscillating Frequency		F_W	-	-	-	kHz	
Individual Lamp Current		I_L	11.5	12.0	12.5	mA	H.V (5)
Lamp Detection	High (LD)	LD	5			V	Normal Operation
	Low (LD)	LD			1.5	V	Lamp Connector Open
Dimming frequency		F_B	135	150	165	Hz	
Minimum Duty Ratio		D_{MIN}	-	15	-	%	

Note (5) Lamp current is measured master board by utilizing high frequency current meters as shown below:

Note (6) Input voltage Hv based on spec. +-7% tolerance.

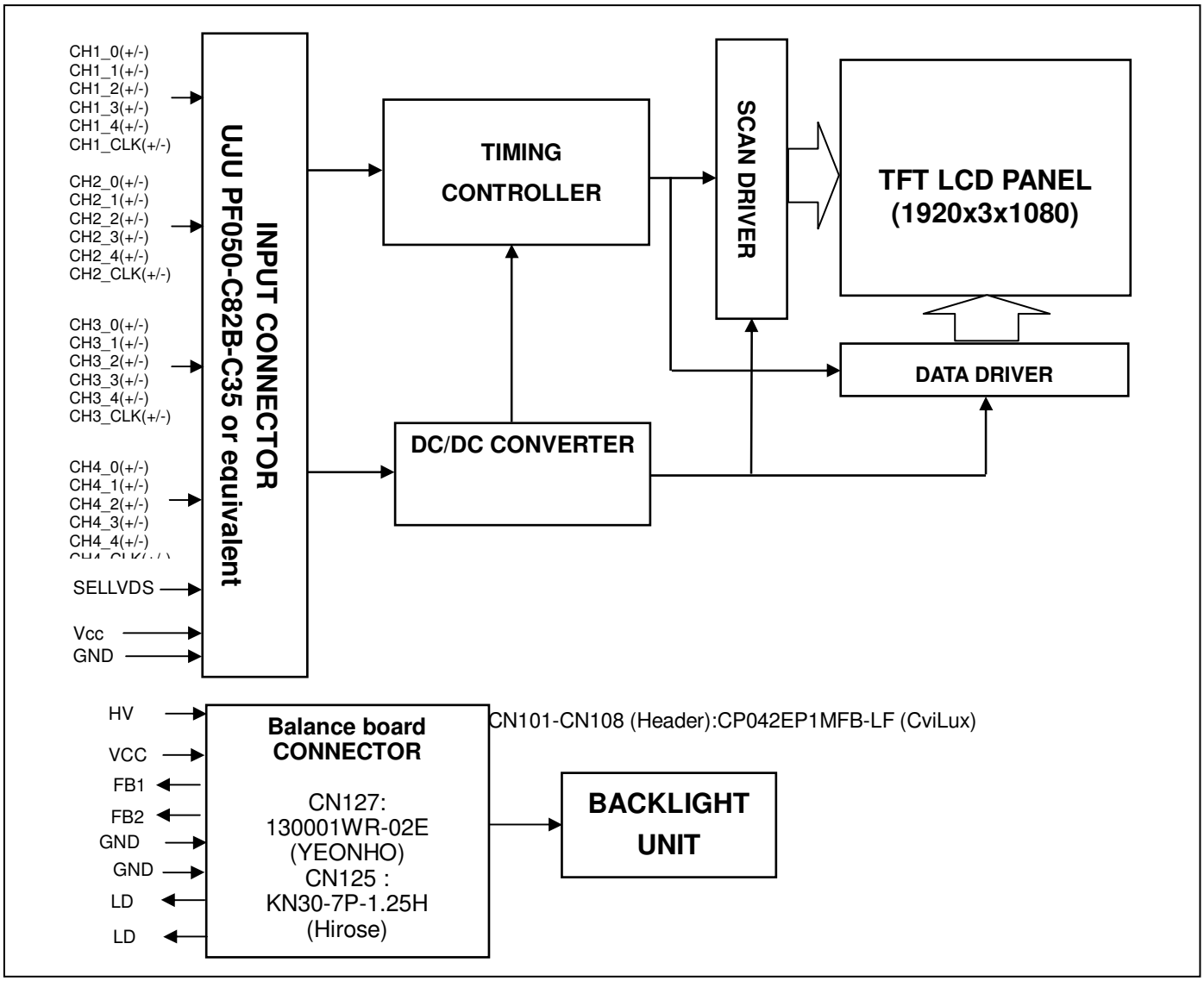
Note (7) Asymmetric ratio must be from 90% to 110% ($0.9<Ip/ I_{rms@T/2X\sqrt{2}}<1.1$)




Balance Board
A
A
1
2
HV (Blue +(-))
HV (White +(-))
LCD Module

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module

CNF1 Connector Pin Assignment (40550-8210,UJU(宇宙) or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	N.C.	No Connection	(1)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
11	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
12	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
13	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
14	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
15	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH1CLK-	First pixel Negative LVDS differential clock input.	
18	CH1CLK+	First pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
21	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
22	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
23	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
26	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
27	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
28	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
29	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
30	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	CH3CLK-	Third pixel Negative LVDS differential clock input.	
33	CH3CLK+	Third pixel Positive LVDS differential clock input.	

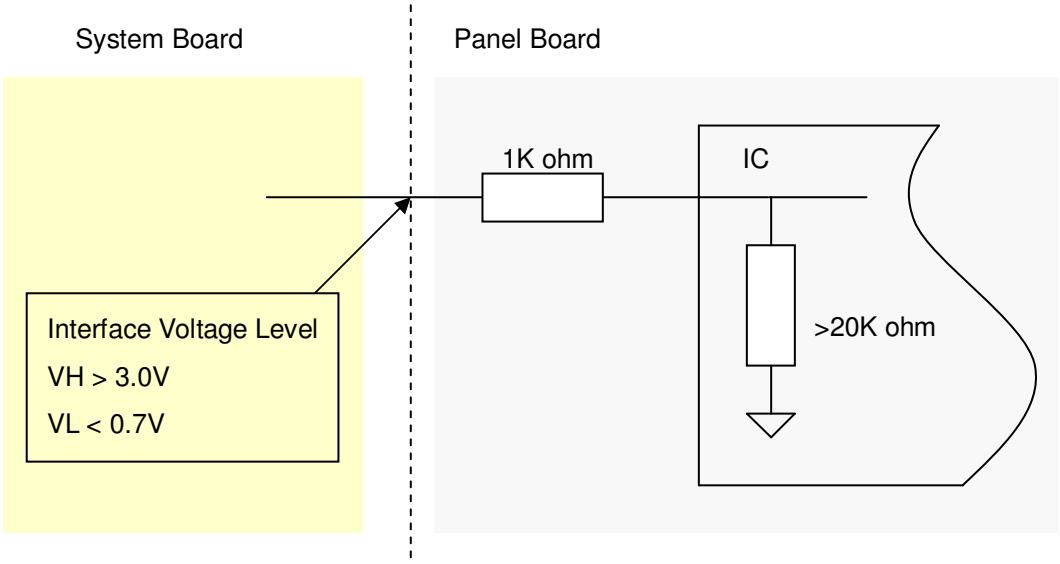
34	GND	Ground	
35	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
36	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
37	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
38	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	SCL	I2C Bus	
41	N.C.	No Connection	(1)
42	N.C.	No Connection	(1)
43	WP	Write Protection for EEPROM	
44	SDA	I2C Bus	
45	LVDS_SEL	LVDS Data Format Selection	(2)
46	N.C.	No Connection	(1)
47	N.C.	No Connection	(1)
48	N.C.	No Connection	(1)
49	N.C.	No Connection	(1)
50	N.C.	No Connection	(1)
51	N.C.	No Connection	(1)
52	GND	Ground	
53	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
54	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
55	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
56	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
57	GND	Ground	
58	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
59	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
60	GND	Ground	
61	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
62	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
63	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
64	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
65	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
66	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
67	GND	Ground	
68	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
69	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
70	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	

71	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
72	GND	Ground	
73	CH2CLK+	Second pixel Positive LVDS differential clock input.	
74	CH2CLK-	Second pixel Negative LVDS differential clock input.	
75	GND	Ground	
76	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
77	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
78	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
79	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
80	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
81	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	
82	GND	Ground	

Note (1) Reserved for internal use. Please leave it open.

Note (2) High=connect to +3.3V or Open : VESA Format ； Low= connect to GND : JEIDA Format.

Note (3) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.



Note (4) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

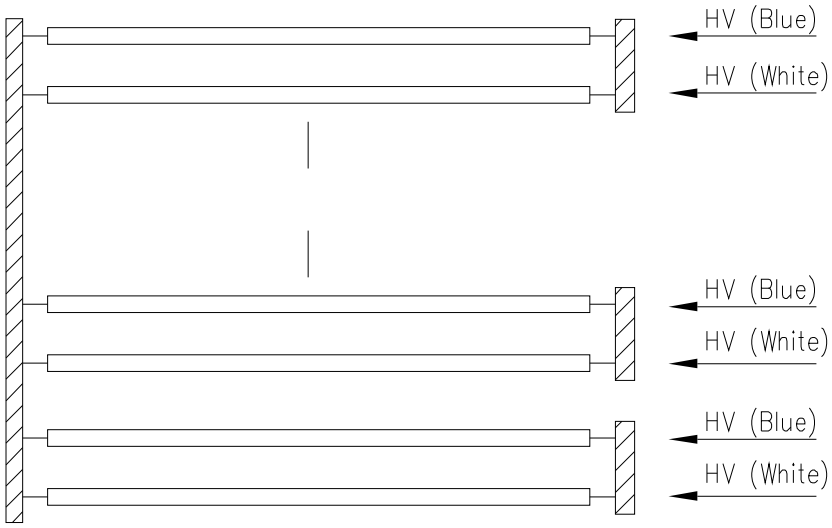
5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN101-CN107: CP042ESFA00 (Cvilux)

Pin	Name	Description	Wire Color
1	HV	High Voltage	Blue
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model CP042ESFA00, manufactured by Cvilux. The mating header on inverter part number is CP042EP1MFB-LF (Cvilux)



5.3 BALANCE BOARD UNIT

CN127 (Header) (Master): 130001WR-02E (YEONHO)

Pin No.	Symbol	Description
1	HV+(-)	High Voltage Input
2	HV+(-)	High Voltage Input

CN227 (Header) (Slave): 130001WR-02E (YEONHO)

Pin No.	Symbol	Description
1	HV-(+)	High Voltage Input
2	HV-(+)	High Voltage Input

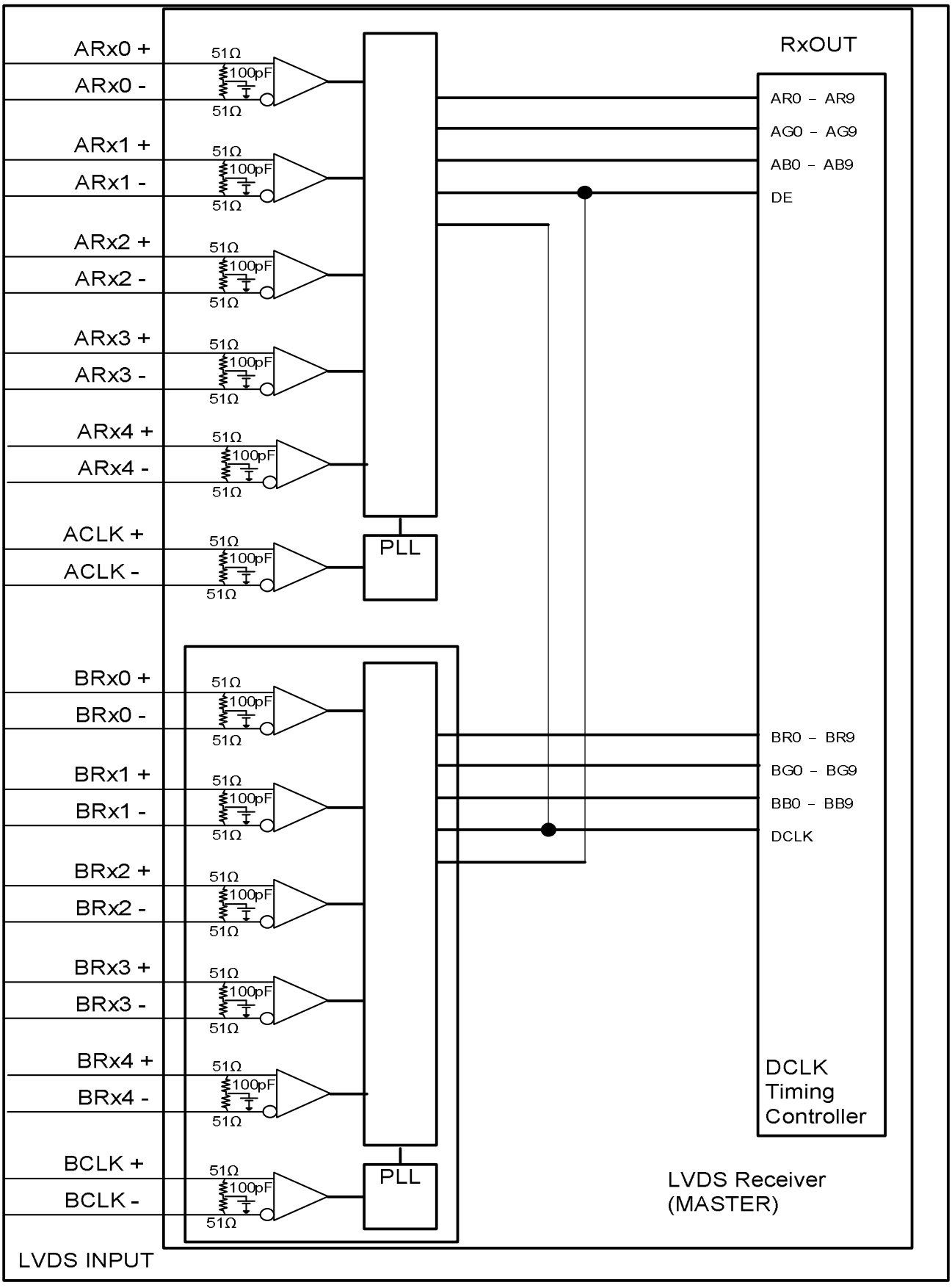
CN101-CN108 (Header) (Master): CP042EP1MFB-LF (CviLux)

Pin No.	Symbol	Description
1	CCFL HOT	CCFL High voltage
2	CCFL HOT	CCFL High voltage

CN125 (Header): KN30-7P-1.25H (Hirose).

Pin No.	Symbol	Description
1	VCC	Power Supply for Protection Circuit
2	FB1	Lamp Current Feedback 1
3	FB2	Lamp Current Feedback 2
4	GND	Signal Ground
5	GND	Signal Ground
6	LD	CCFL Connector Open & Non-lighting signal
7	LD	CCFL Connector Open & Non-lighting signal

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data
AG0~AG9: First pixel G data
AB0~AB9: First pixel B data
BR0~BR9: Second pixel R data
BG0~BG9: Second pixel G data
BB0~BB9: Second pixel B data
DE: Data enable signal
DCLK: Data clock signal

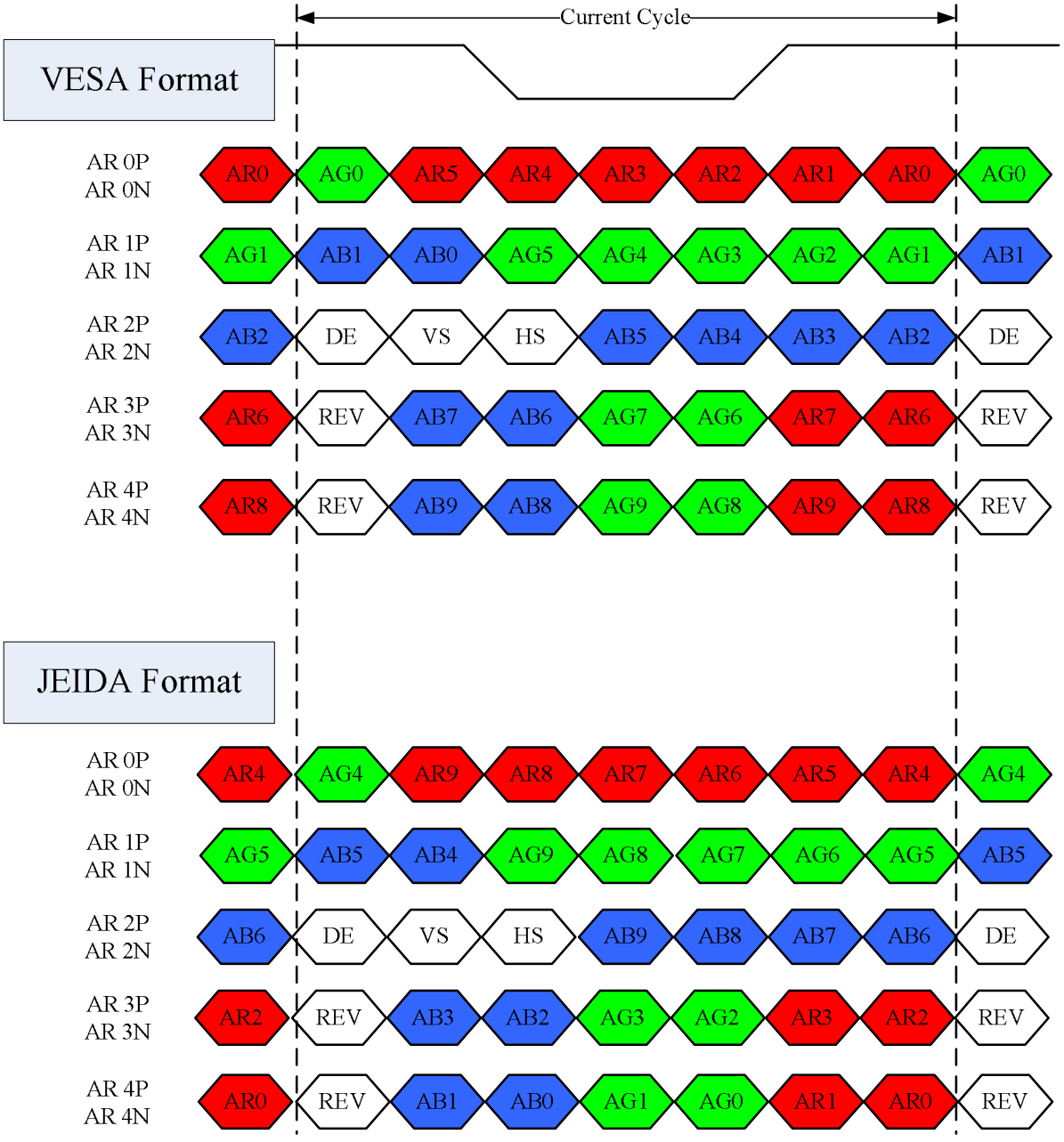
The third and fourth pixel are followed the same rules.
CR0~CR9: Third pixel R data
CG0~CG9: Third pixel G data
CB0~CB9: Third pixel B data
DR0~DR9: Fourth pixel R data
DG0~DG9: Fourth pixel G data
DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.
Note (2) The system must have the transmitter to drive the module.
Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

VESA Format: SELLVDS = H or Open

JEIDA Format: SELLVDS = L



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE: Data enable signal

DCLK: Data clock signal

RSV: Reserved

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	;	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0

	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	97	100	103	Hz	(6)
		F_{r6}	117	120	123	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	—
	Blank	Thb	60	70	95	Tc	—

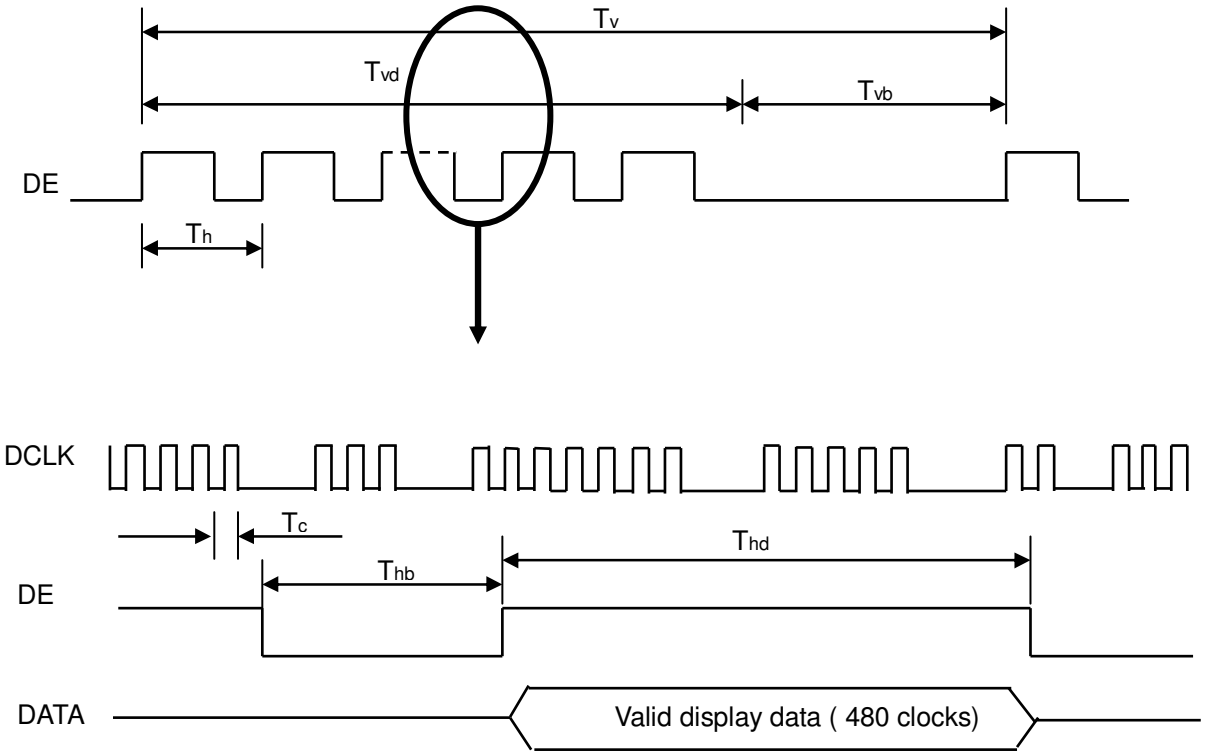
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

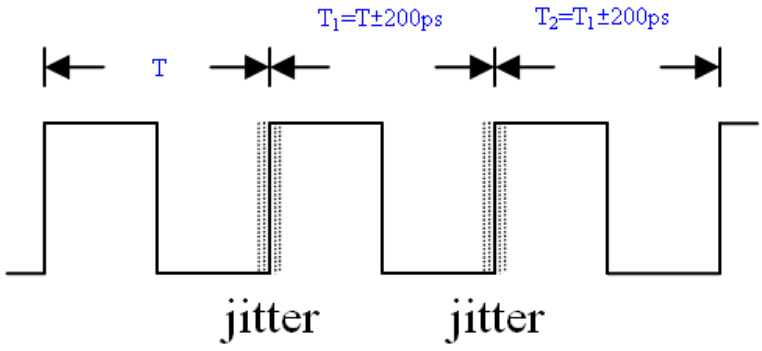
$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$Fr5 \times Tv \times Th \geqq F_{clkin(min)}$

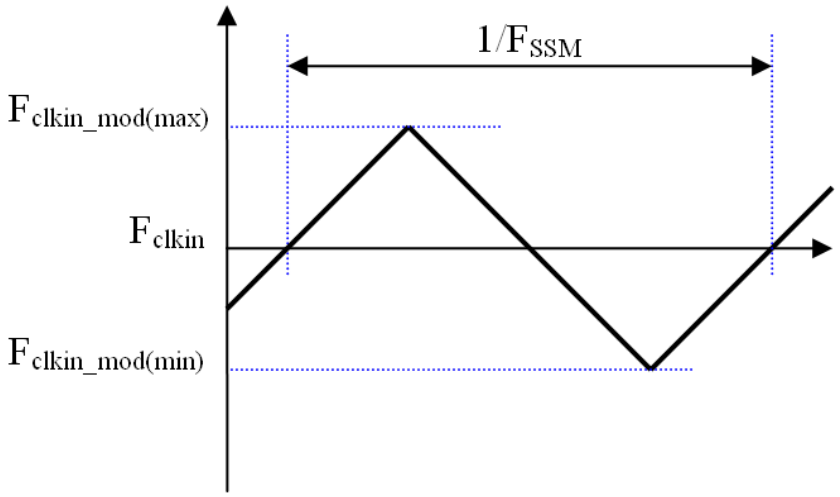
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T1 – TI

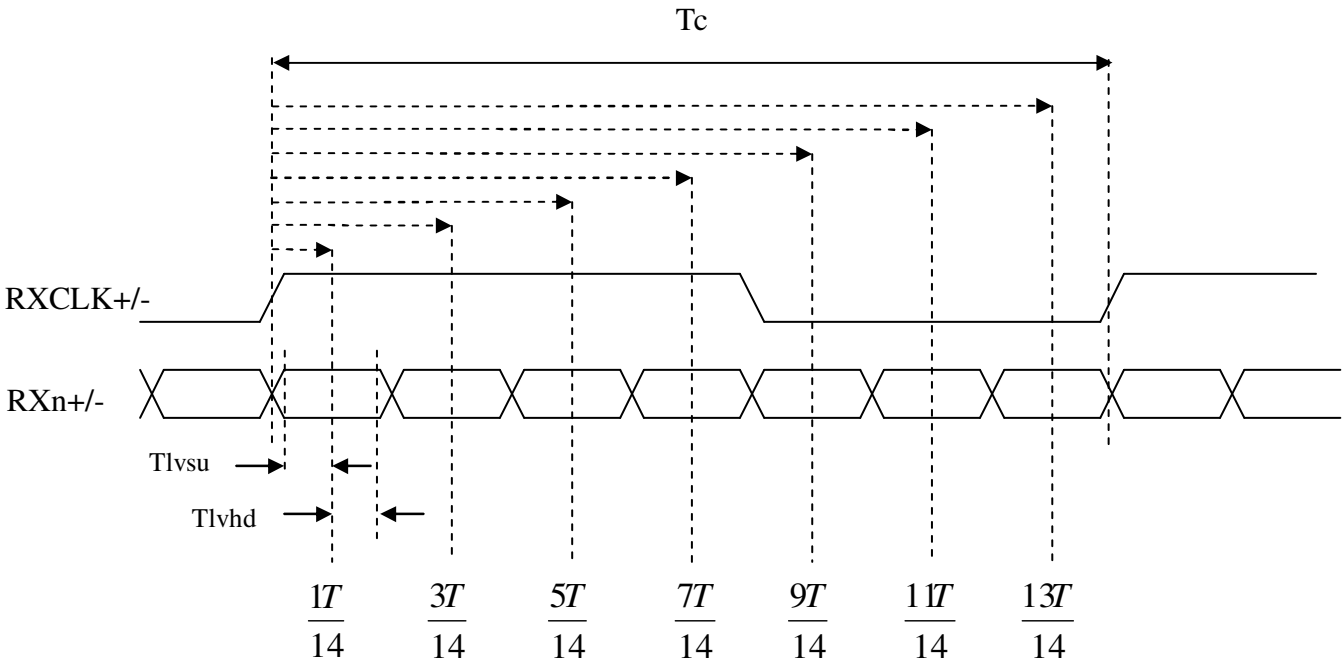


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

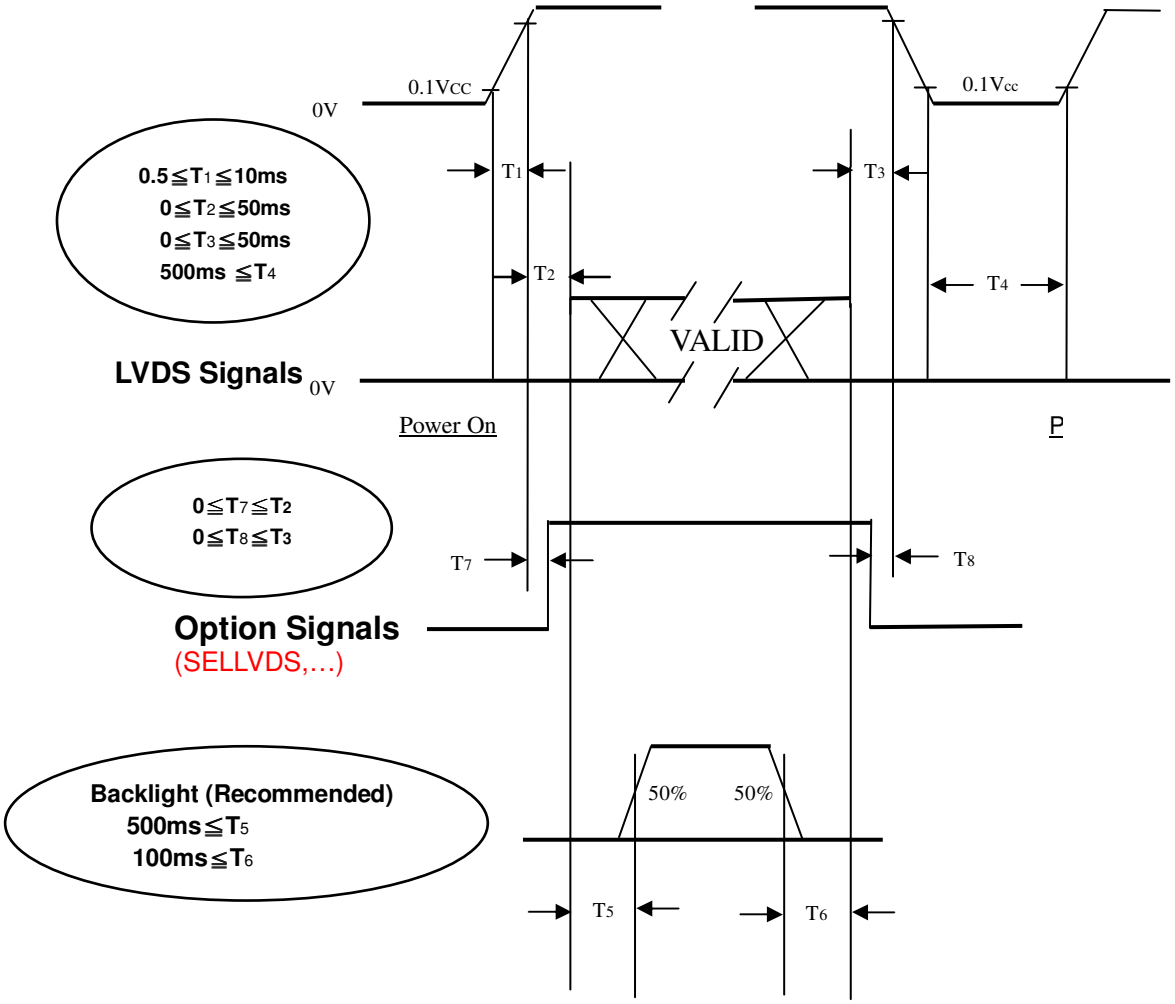
LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) : (ODSEL) = H/L or open for 100/120Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	12.0±0.5	mA
Oscillating Frequency (Inverter)	F_W	47±2	KHz
Vertical Frame Rate	Fr	60	Hz

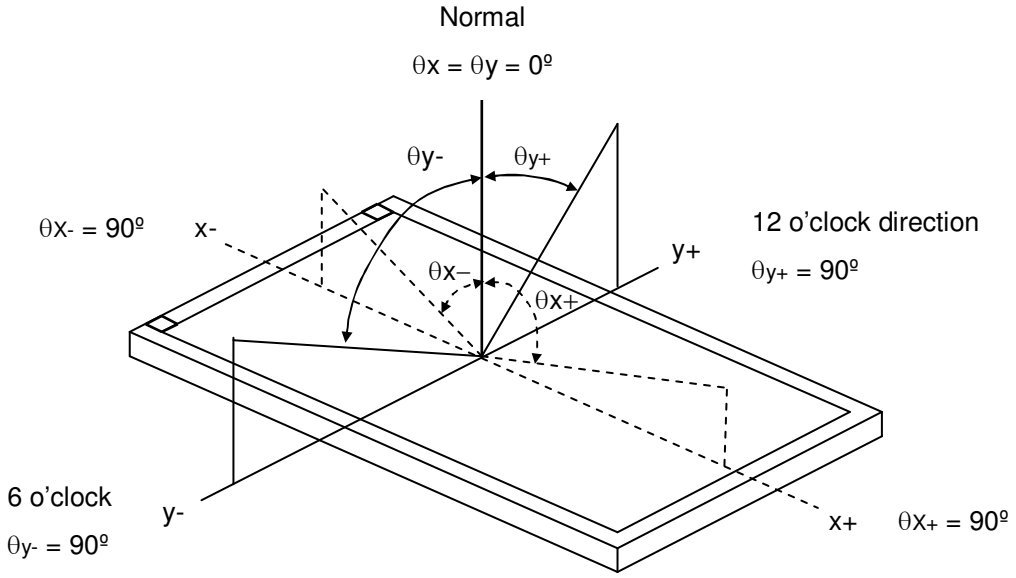
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing angle at normal direction	4500	6500	-	-	Note (2)
Response Time		Gray to gray		-	4.5	8	ms	Note (3)
Center Luminance of White		L_C		400	500	-	cd/m^2	Note (4)
White Variation		δW		-	-	1.3	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ.-0.03	0.633	Typ.+0.03	-	Note (6)
		Ry			0.324		-	
	Green	Gx			0.284		-	
		Gy			0.599		-	
	Blue	Bx			0.147		-	
		By			0.048		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut				72	-	%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	Note (1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

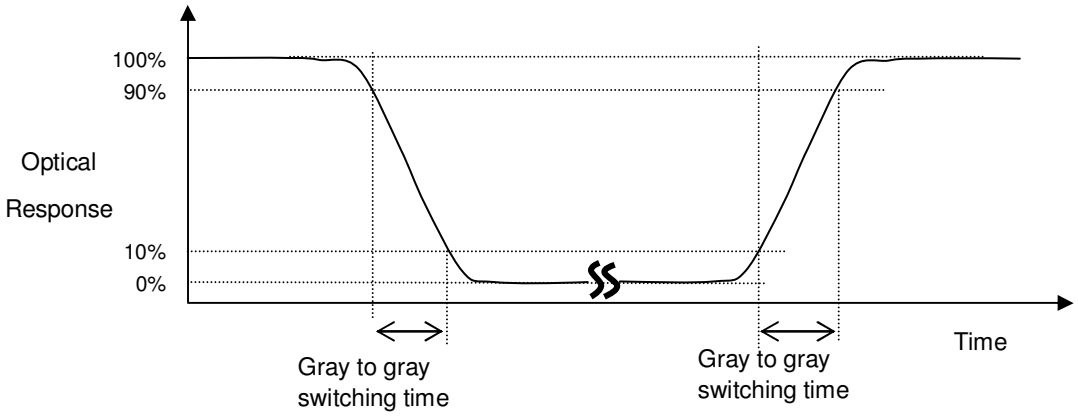
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7)

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other .

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

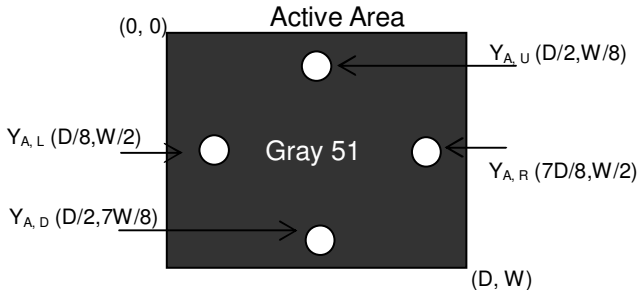
$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

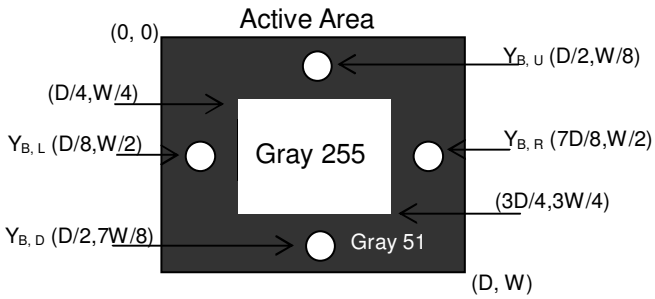
Where:

(a)

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)

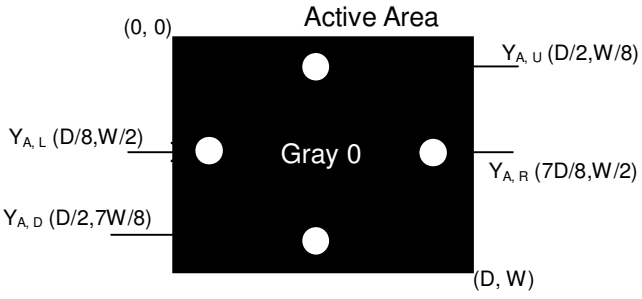


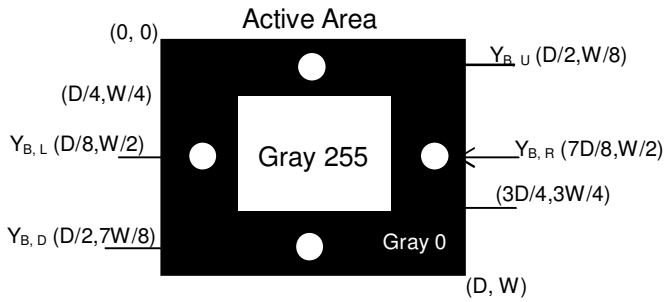


(b)

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

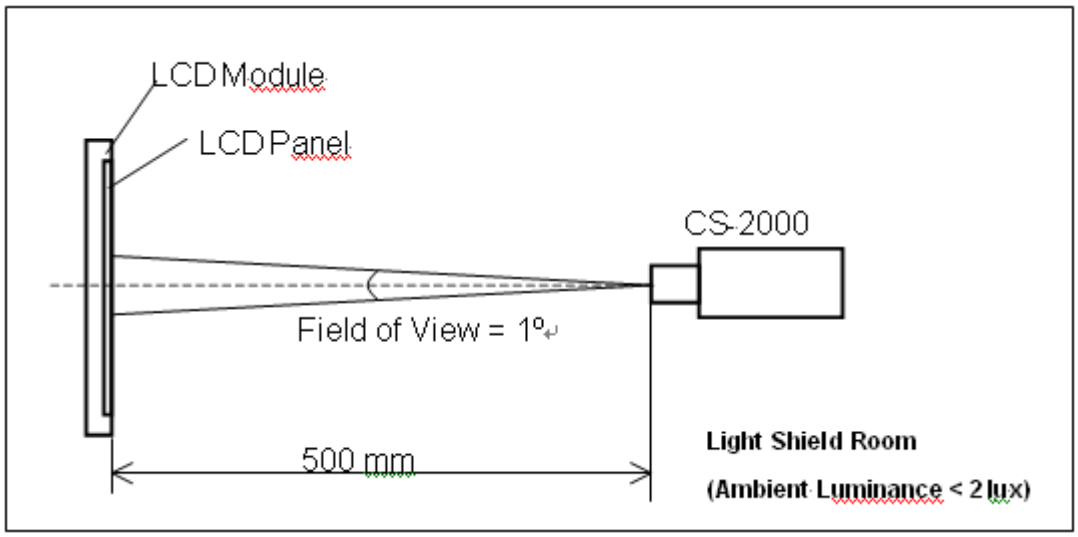
Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)





Note (6) Measurement Setup:

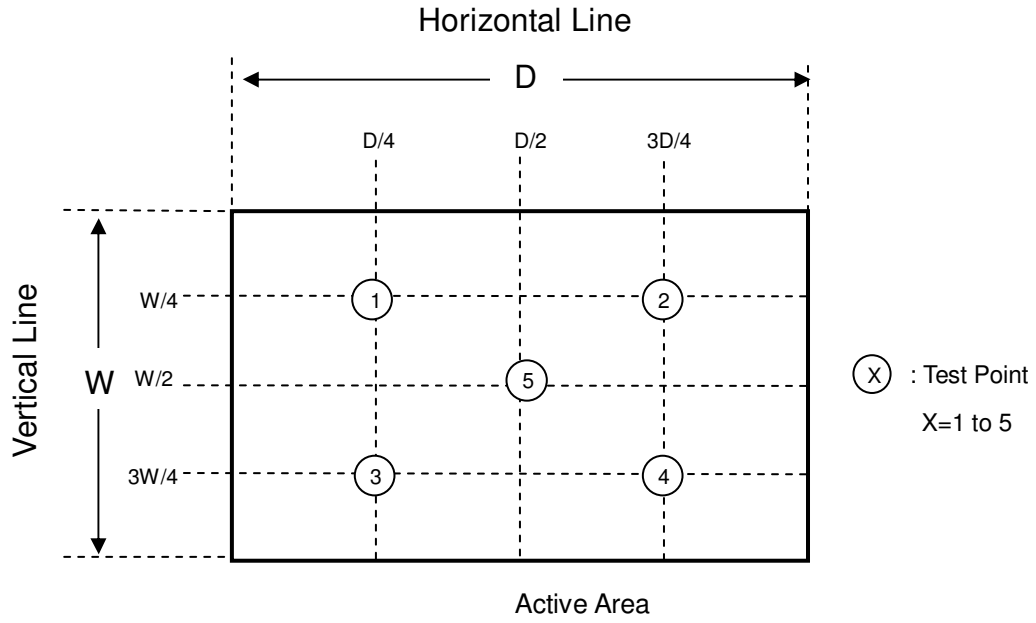
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

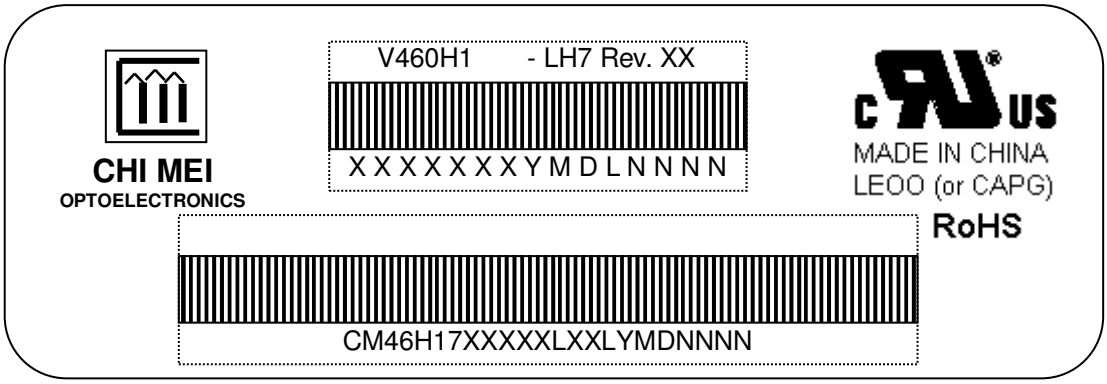
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V460H1-LH7

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X-XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4… Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1st to 31st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
L	Product line #	Line 1=1, Line 2=2, Line 3=3, …
NNNN	Serial number	Manufacturing sequence of product

(d) Customer's barcode definition:

Serial ID: CM-46H17-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
46H17	Model number	V460H1-LH7=46H17
X	Revision code	C1=A, C2=B, …..
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C, OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
X	Gate driver IC code	
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN
L	Module line #	1~12=0~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4… Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1st to 31st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
NNNN	Serial number	By LCD supplier

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 3 LCD TV modules / 1 Box

(2) Box dimensions : 1175(L)x 282(W)x 725(H)mm

(3) Weight : approximately 45Kg (3 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

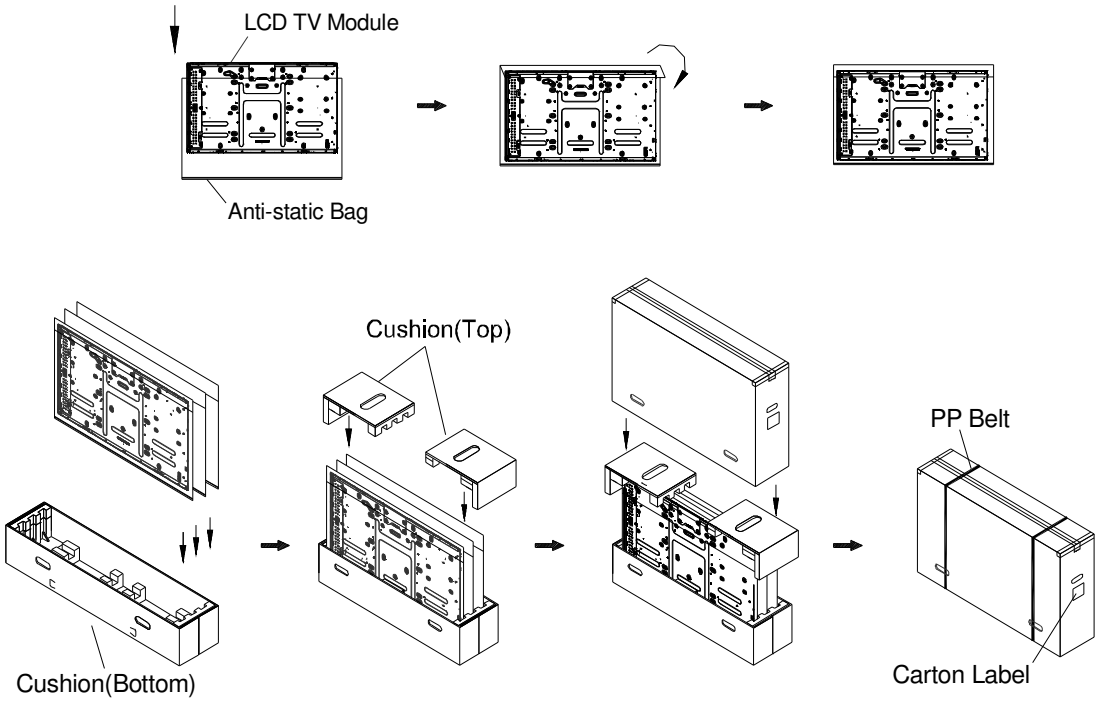
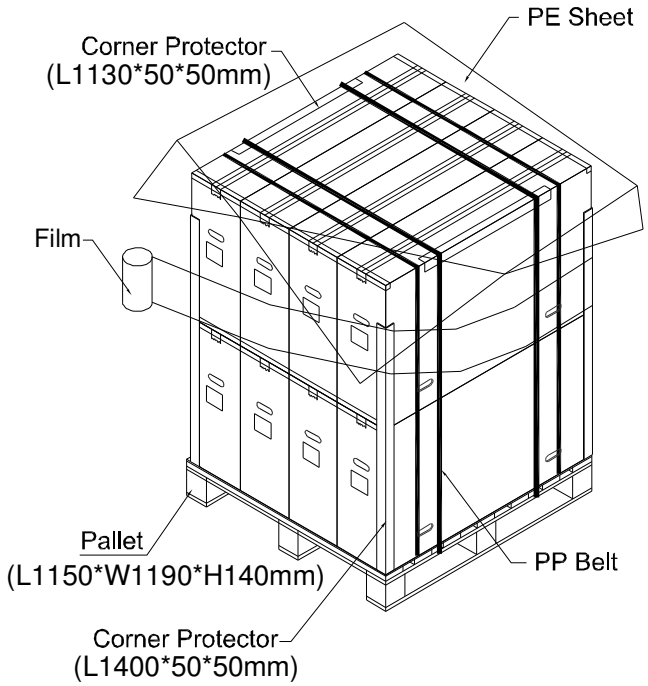


Figure.9-1 packing method

Air Transportation &

Sea / Land Transportation (40ft Container)



Sea / Land Transportation (40ft HQ Container)

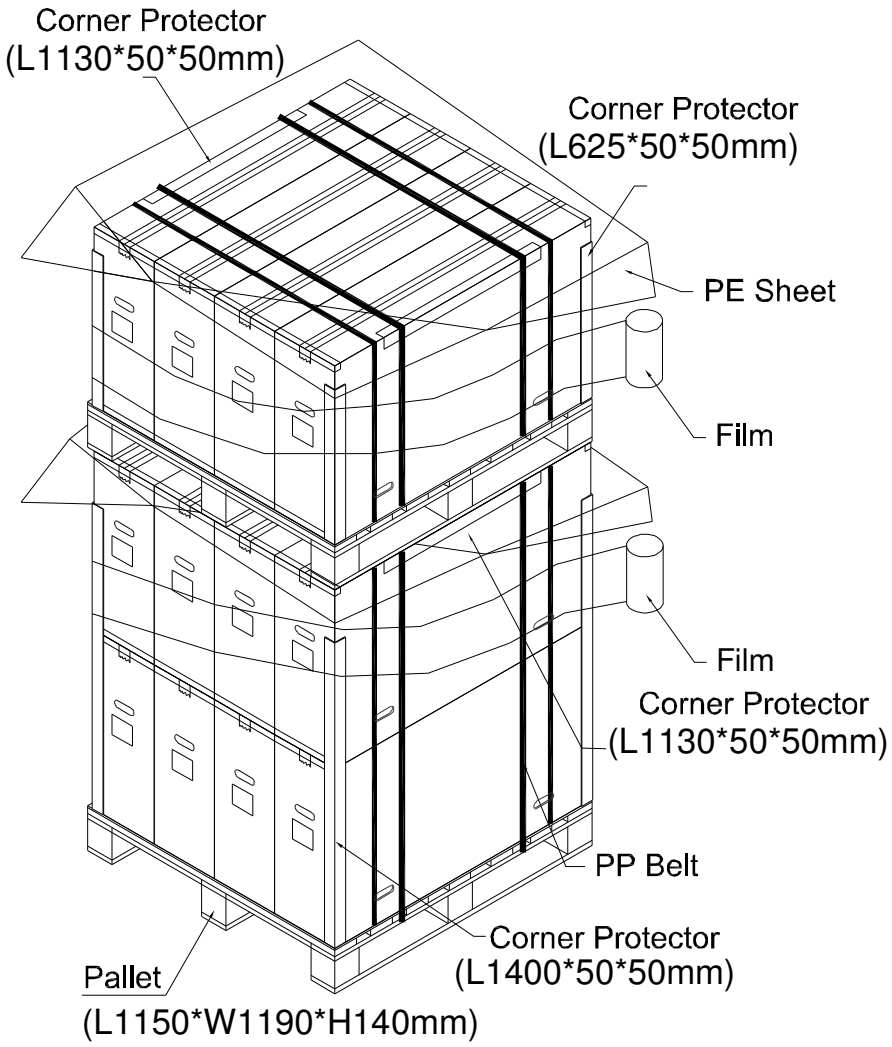


Figure.9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

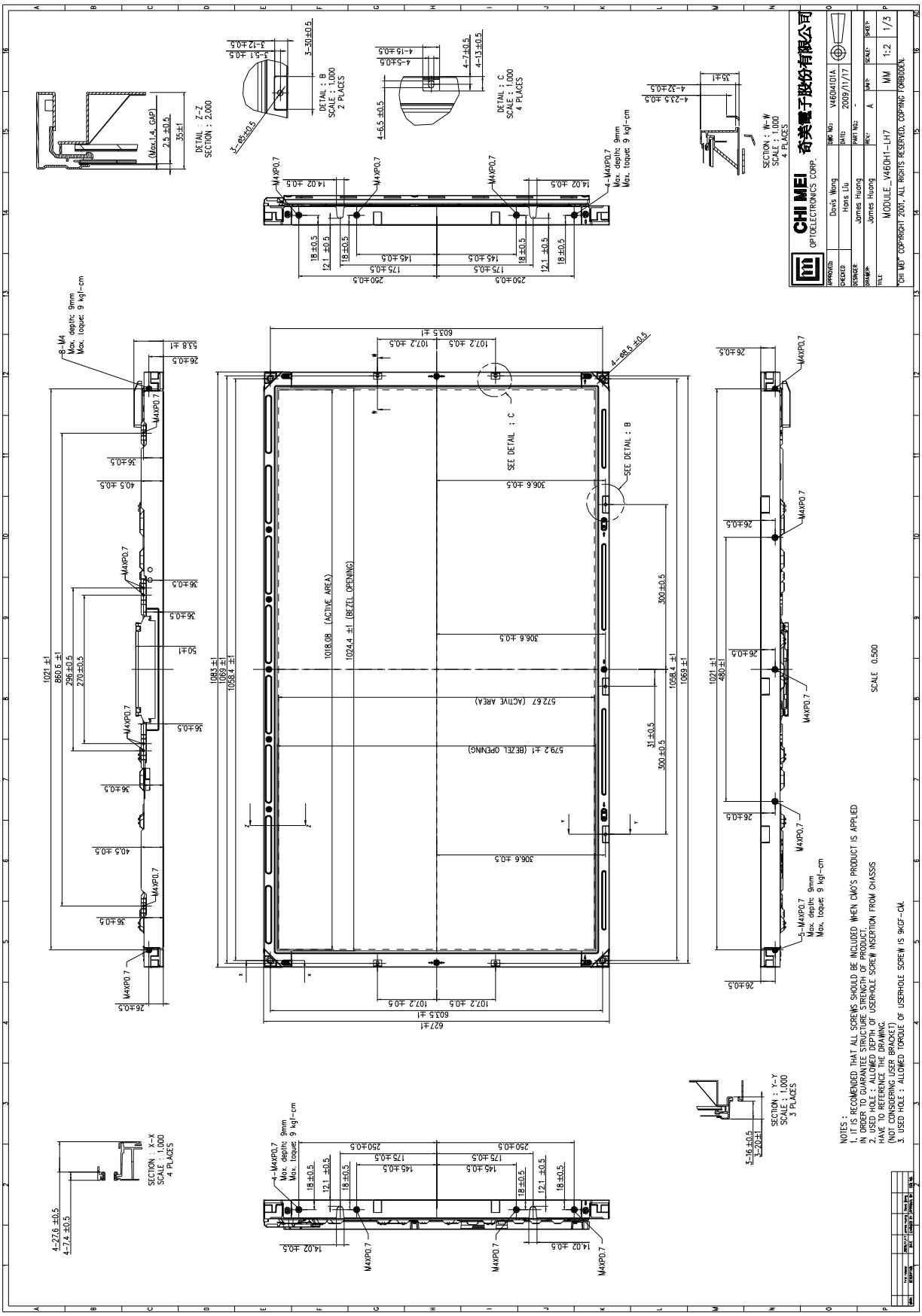
10.3 SAFETY STANDARDS

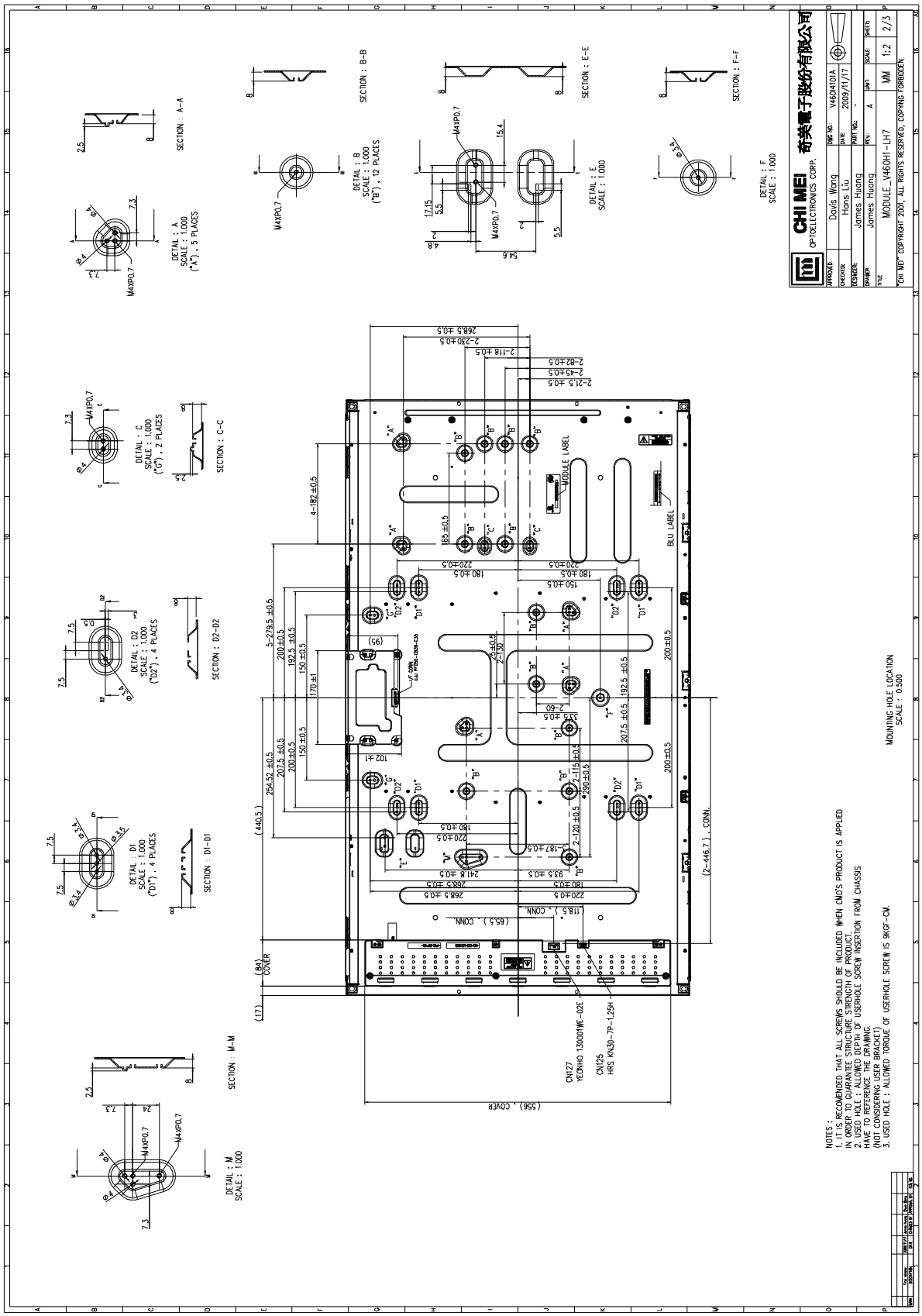
The LCD module should be certified with safety regulations as follows:

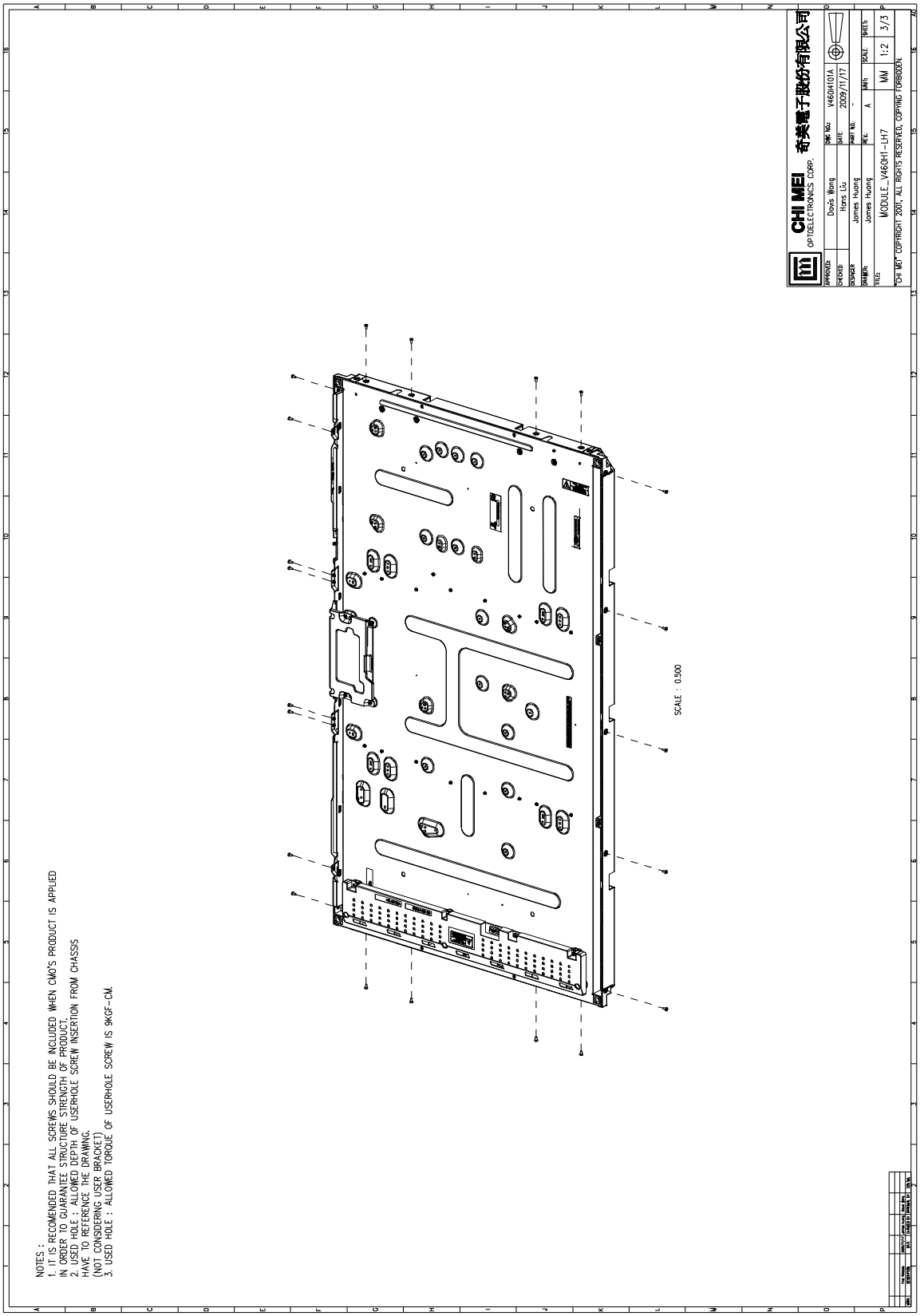
Regulatory	Item	Standard
Information Technology equipment	UL	UL 60950-1: 2003
	cUL	CAN/CSA C22.2 No.60950-1-03
	CB	IEC 60950-1:2001
Audio/Video Apparatus	UL	UL 60065: 2003
	cUL	CAN/CSA C22.2 No.60065-03
	CB	IEC 60065:2001

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

11. MECHANICAL CHARACTERISTIC




CHI MEI OPTOELECTRONICS CORP.
奇美電子股份有限公司
MODULE_V460H1-LH7
V460H1-A
2009/1/17
1:2
2/3
"CHI MEI" COPYRIGHT 2001, ALL RIGHTS RESERVED, COPYING FORBIDDEN
SECTION : A-A
SECTION : B-B
SECTION : C-C
SECTION : D1-D1
SECTION : D2-D2
SECTION : E-E
SECTION : F-F
SECTION : W-W
DETAIL : A SCALE : 1.000 ("A"), 5 PLACES
DETAIL : B SCALE : 1.000 ("B"), 12 PLACES
DETAIL : C SCALE : 1.000 ("C"), 2 PLACES
DETAIL : D1 SCALE : 1.000 ("D1"), 4 PLACES
DETAIL : D2 SCALE : 1.000 ("D2"), 4 PLACES
DETAIL : E SCALE : 1.000
DETAIL : F SCALE : 1.000
DETAIL : W SCALE : 1.000
MODULE LABEL
BLU LABEL
MOUNTING HOLE LOCATION SCALE : 0.500
CN127 YEONHO 13001WE-02E
CN125 HRS KN3D-7P-1.25H
NOTES :
1. IT IS RECOMENDED THAT ALL SCREWS SHOULD BE INCLUDED WHEN CMO'S PRODUCT IS APPLIED IN ORDER TO GUARANTEE STRUCTURE STRENGTH OF PRODUCT.
2. USED HOLE : ALLOWED DEPTH OF USERHOLE SCREW INSERTION FROM CHASSIS HAVE TO REFERENCE THE DRAWING.
(NOT CONSIDERING USER BRACKET)
3. USED HOLE : ALLOWED TORQUE OF USERHOLE SCREW IS 9KGF-CM.


CHI MEI 奇美電子股份有限公司
OPTOELECTRONICS CORP.
APPROVED: Davis Wang
CHECKED: Hans Liu
DESIGNER: James Huang
DRAWN: James Huang
TITLE: MODULE_V460H1-LH7
DWG NO: V460H1-01A
DATE: 2009/11/17
PART NO. -
REV: A
UNIT: MM
SCALE: 1:2
SHEETS: 3/3
"CHI MEI" COPYRIGHT 2001, ALL RIGHTS RESERVED, COPYING FORBIDDEN.
SCALE : 0.500
NOTES :
1. IT IS RECOMENDED THAT ALL SCREWS SHOULD BE INCLUDED WHEN CMO'S PRODUCT IS APPLIED IN ORDER TO GUARANTEE STRUCTURE STRENGTH OF PRODUCT.
2. USED HOLE : ALLOWED DEPTH OF USERHOLE SCREW INSERTION FROM CHASSIS HAVE TO REFERENCE THE DRAWING.
(NOT CONSIDERING USER BRACKET)
3. USED HOLE : ALLOWED TORQUE OF USERHOLE SCREW IS 9KGF-CM.