CHI MEI OPTOELECTRONICS CORP.

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Model No.: V460H1 - LH9-901
Tentative

TFT LCD Tentative Specification

MODEL NO.: V460H1 - LH9-901

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 0.0	Nov. 27,'09	All	All	Tentative Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V460H1-LH9 is a 46" TFT Liquid Crystal Display module with 14-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color). The inverter for backlight is built-in.

1.2 FEATURES

- High brightness (450nits)
- High contrast ratio (6000:1)
- Fast response time (Gray to Gray average 6.5 ms)
- High color saturation (72% NTSC)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
  — DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 100/120 Hz frame rate
- Ultra wide viewing angle: Super MVA technology

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1018.08(H) x 572.67(V) (46" diagonal)	mm	(1)
Bezel Opening Area	1024.4(H) x 579.2(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.17675(H) x 0.53025(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 11%) Hardness (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	-	1083	-	mm	(1), (2)
	Vertical (V)	-	627	-	mm	
	Depth (D)	-	51.2	-	mm	
Weight		-	TBD	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	T_{ST}		-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}		0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	50	G	(3), (5)
		Z axis	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≤ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

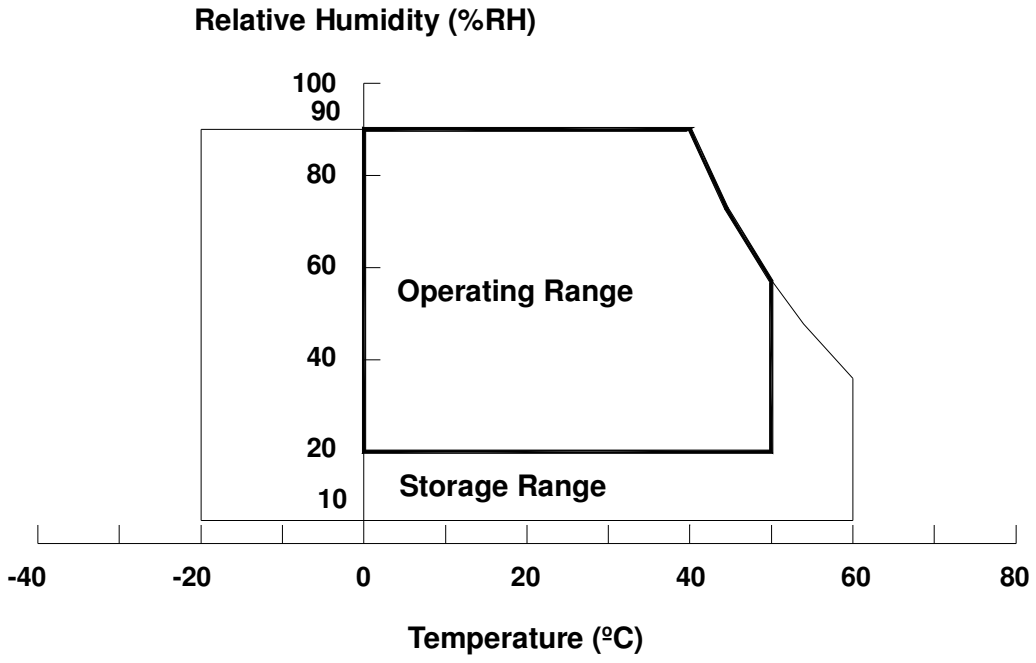
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, and ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

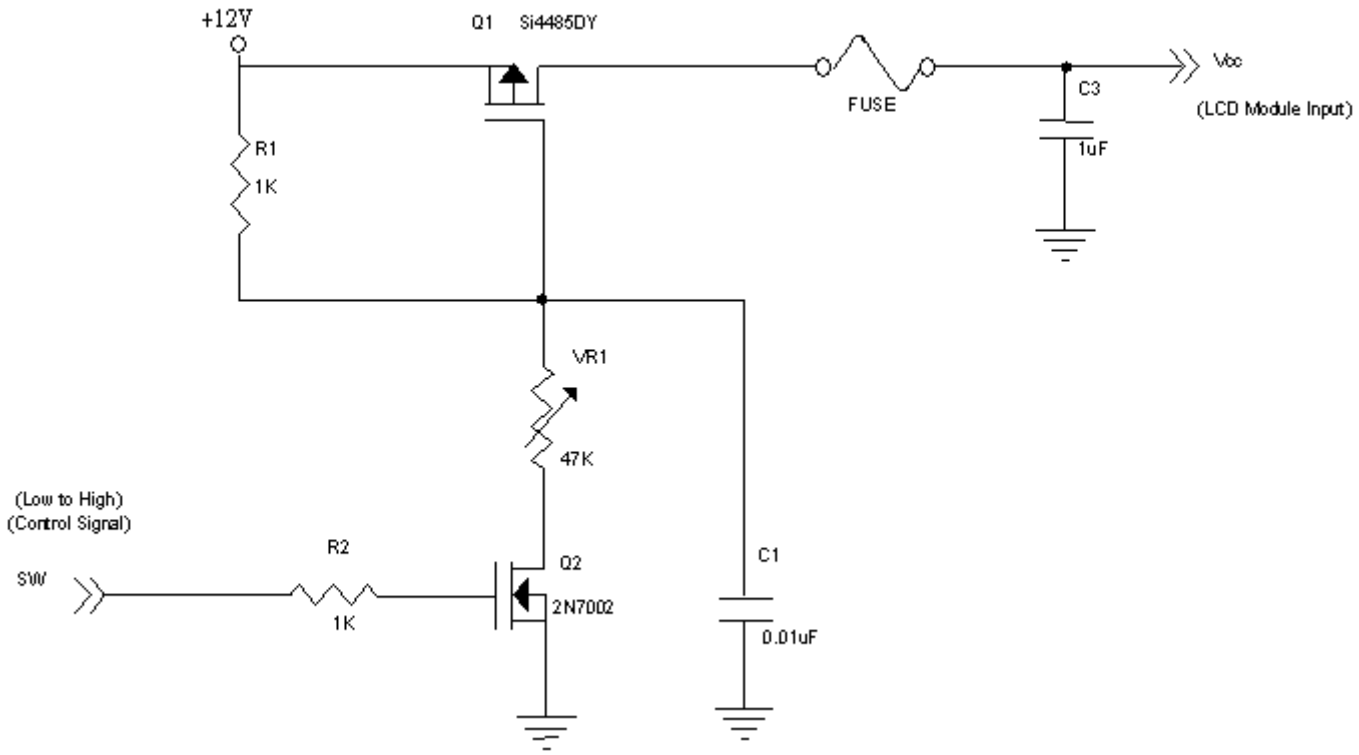
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE (Ta = 25 ± 2 ºC)

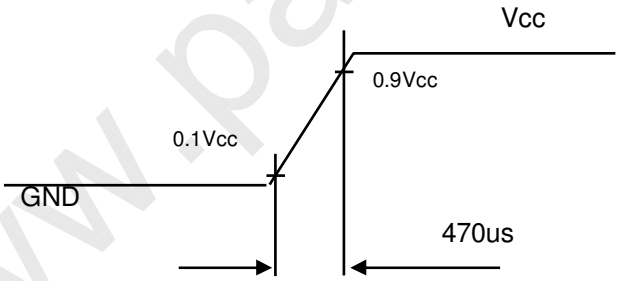
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	3.5	A	(2)
Power Supply Current	White Pattern	I_{CC}	-	0.9	-	A	(3)
	Black Pattern		-	0.86	-	A	
	Horizontal Stripe		-	2	2.4	A	
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	ohm	
	Terminating Resistor	R_T	-	100	-		
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

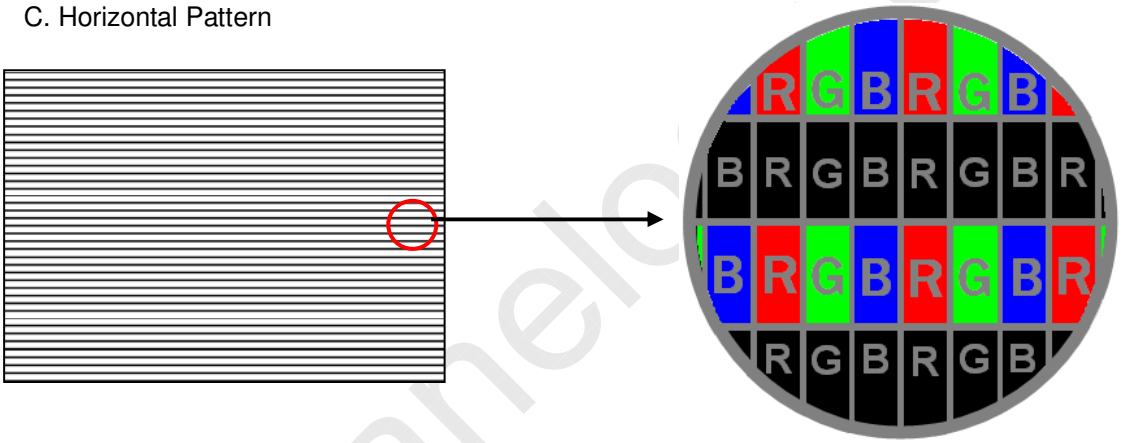
a. White Pattern

Active Area

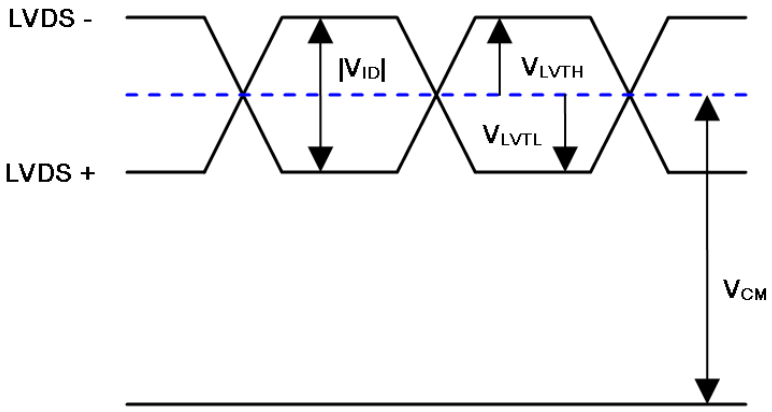
b. Black Pattern

Active Area

C. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1100	-	V_{RMS}	-
Lamp Current	I_L	9.7	10.2	10.7	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	1820	V_{RMS}	(2), Ta = 0 ºC
		-	-	1650	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_L	30	-	80	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Power Consumption	P_{255}	-	155	TBD	V	(6)
Power Supply Voltage	V_{BL}	22.8	24	25.2	V	
Power Supply Current	I_{BL}	-	6.46	TBD	Arms	No Dimming
Input Ripple Noise	-	-	-	912	kHz	
Oscillating Frequency	F_W	37	40	43	mA	H.V (5)
Dimming frequency	F_B	150	160	170	Hz	Dimming frequency
Minimum Duty Ratio	D_{MIN}	-	20	-	%	Minimum Duty Ratio

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

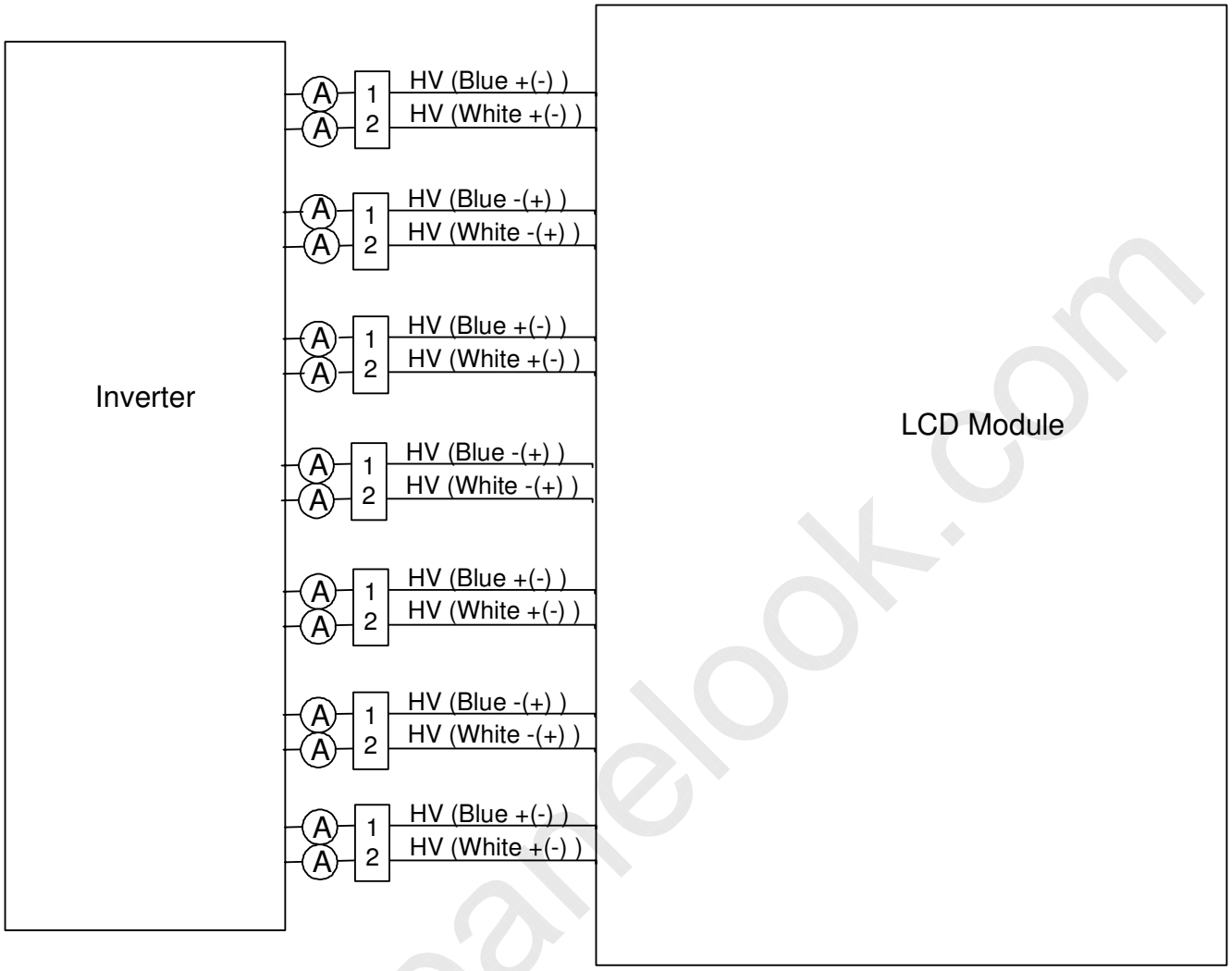
Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 9.7~ 10.7mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 46" backlight unit under input voltage 24V, average lamp current 10.5 mA and lighting 30 minutes later.



3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	—	2.85	3.0	3.15	V	Maximum duty ratio
	MIN			—	0	—	V	Minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	—	2.0	—	5.0	V	Duty on
	LO			0	—	0.8	V	Duty off
Status Signal	HI	Status	—	3.0	3.3	3.6	V	Normal
	LO			0	—	0.8	V	Abnormal
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V_{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
PWM Delay Time		T_{PWM}	—	100		—	ms	
BLON Delay Time		T_{on}	—	300	—	—	ms	
		T_{on1}	—	300	—	—	ms	
BLON Off Time		T_{off}	—	300	—	—	ms	

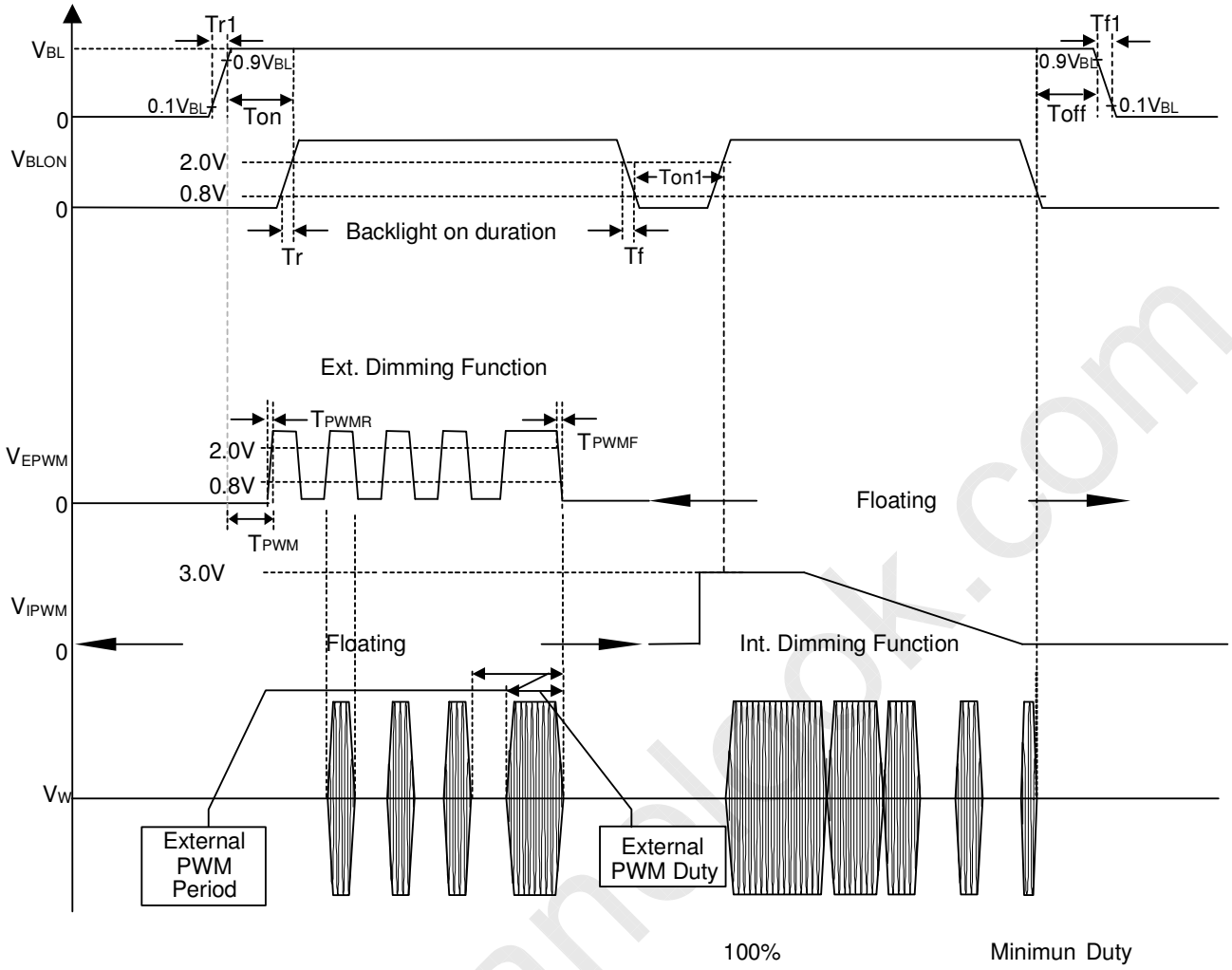
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

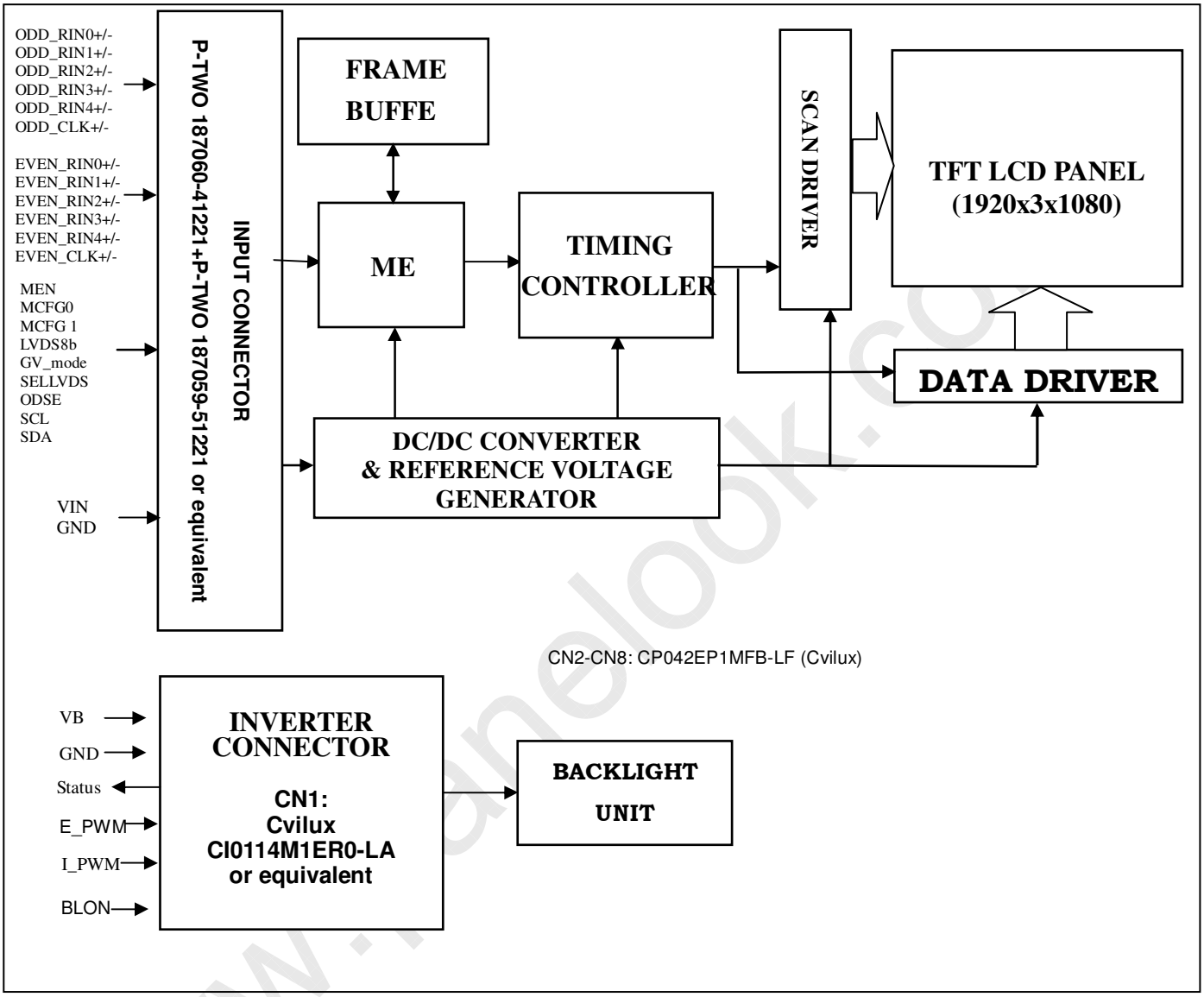
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



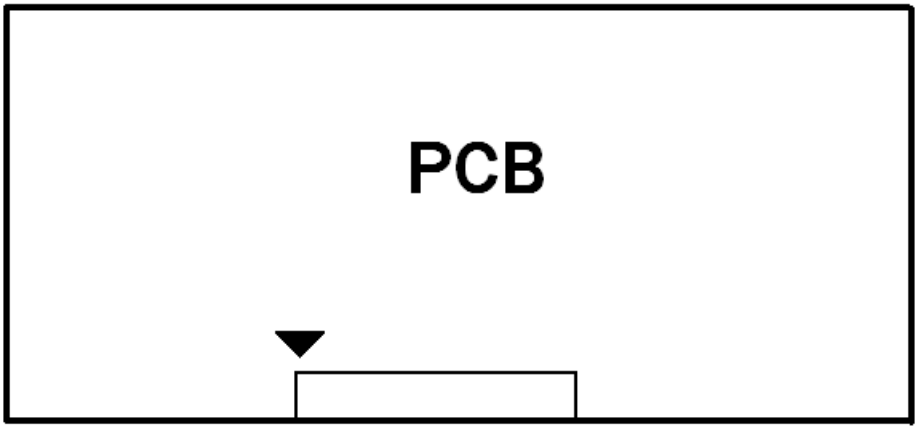
5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module

CNF1 Connector Part No.: JAE Taiwan (台灣航空電子) FI-RE51S-HF or equivalent.

Pin	Name	Description	Note
1	RPF	Reverse picture function (default low)	
2	MEN	MEMC function selection	
3	MCFG0	MEMC function selection	
4	MCFG1	MEMC function selection	
5	LVDS8b	8bit/10bit LVDS input selection	
6	GV_mode	Graphic / Video mode selection	
7	SELLVDS	LVDS data format Selection	
8	SCL	I2C CLK Signal	
9	SDA.	I2C Data Signal	
10	ODSEL	Overdrive Lookup Table Selection	
11	GND	Ground	
12	ERX0-	2nd pixel Negative LVDS differential data input. Channel 0	
13	ERX0+	2nd pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	2nd pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	2nd pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	2nd pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	2nd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	2nd pixel Negative LVDS differential clock input.	
20	ECLK+	2nd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ERX3-	2nd pixel Negative LVDS differential data input. Channel 3	
23	ERX3+	2nd pixel Positive LVDS differential data input. Channel 3	
24	ERX4-	2nd pixel Negative LVDS differential data input. Channel 4	
25	ERX4+	2nd pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	
27	N.C.	No Connection	
28	ORX0-	1st pixel Negative LVDS differential data input. Channel 0	
29	ORX0+	1st pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	1st pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	1st pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	1st pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	1st pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	1st pixel Negative LVDS differential clock input.	
36	OCLK+	1st pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ORX3-	1st pixel Negative LVDS differential data input. Channel 3	
39	ORX3+	1st pixel Positive LVDS differential data input. Channel 3	
40	ORX4-	1st pixel Negative LVDS differential data input. Channel 4	
41	ORX4+	1st pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) LVDS connector pin orderdefined as follows



Note (2) Reserved for internal use. Please leave it open.

Note (3)

SELLVDS	Mode
L(default)	VESA
H	JEIDA

L: Connect to GND, H: Connect to +3.3V

Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL	Description
L(default)	Lookup table was optimized for 60 Hz frame rate input.
H	Lookup table was optimized for 50 Hz frame rate input.

L: Connect to GND, H: Connect to +3.3V

Note (5) Motion Engine (ME) Level & Demo Function Table

Motion engine level must be adjusted after video mode is selected (or entered).

Adjusting the motion engine level in graphic mode has no effect

		MEN	MCFG1	MCFG0	Notes		
Blanking	Blanking disable	0	0	0	(a)		
	Auto blanking	0	0	1	(b)		
	Blanking enable	0	1	0	(c)		
				Effect of ME →	De blur	De judder	Halo
Demo mode (d)		0	1	1	Demo Window		
ME Level	Strong	1	0	0	Enable	Strong	Strong
	Medium(Default)	1	0	1	Enable	Normal	Normal
	Weak	1	1	0	Enable	×	×
	OFF	1	1	1	×	×	×
		(e) (f) (g)					

(a) Module re-starts processing video signals from Frontend scaler control board.

(b) During sync unstable period such as format change, 60Hz <-> 50Hz .
MCFG0 can be used to insert blanking of 500ms. This signal is toggled.

(c) Module continues to insert blanking until blanking disable signal is received from frontend scaler board.

(d) Demo window mode: Demo Window appears to the left half of display area. Left side with frame is 120Hz with MEMC, and right side is 120Hz w/o motion compensation.

(e) GPIO (General Purpose I/O) sequence of ME Level: (1) MEN; (2) MCFG1; (3) MCFG0.
GPIO sequence of Blanking Enable, Blanking Disable and Demo window: (1) MCFG1; (2) MCFG0; (3) MEN.

(f) Each scaler command must be maintained the same voltage level at least 100ms.

(g) 0 : Connect to GND, 1 : +3.3V

Note (6) 8bit/10bit LVDS input selection

LVDS8b	Bit depth
H(default)	8bit
L	10bit

L : Connect to GND, H : Connect to +3.3V

Note (7) Graphic / Video mode selection

There is no prohibited time period for switching between Graphic mode and Video mode.
When this switching signal is input, LCD will be reset and will re-start selected mode.

GV_mode	**Mode select**	**MEMC ON/OFF**
H(default)	Graphic mode	MEMC OFF
L	Video mode	MEMC ON

L : Connect to GND, H : Connect to +3.3V

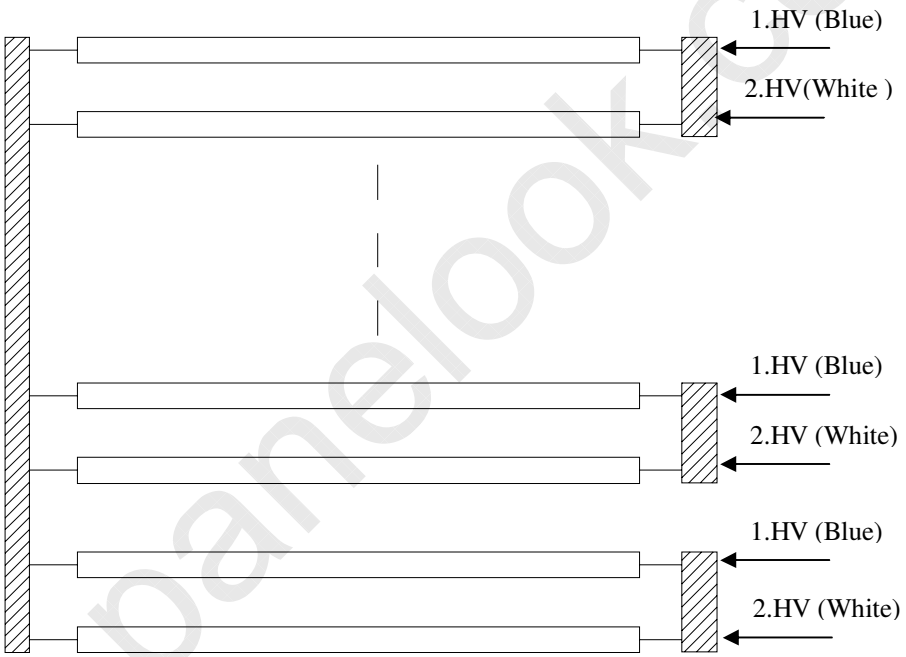
5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN2-CN8: CP042EP1MFB-LF (Cvilux)

Pin	Name	Description	Wire Color
1	HV	High Voltage	Blue
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model CP042EP1MFB-LF, manufactured by Cvilux. The mating header on inverter part number is CP042EP1MFB-LF (Cvilux)



5.3 INVERTER UNIT

CN1: CI0114M1ER0-LA (Cvilux) or equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	STATUS	Normal (3.3V) Abnormal(GND)
12	E_PWM	External PWM Control Signal
13	I_PWM	Internal PWM Control Signal
14	BLON	BL ON/OFF

Note (1) Pin 12: External PWM control (use pin 12): Pin 13 must open.

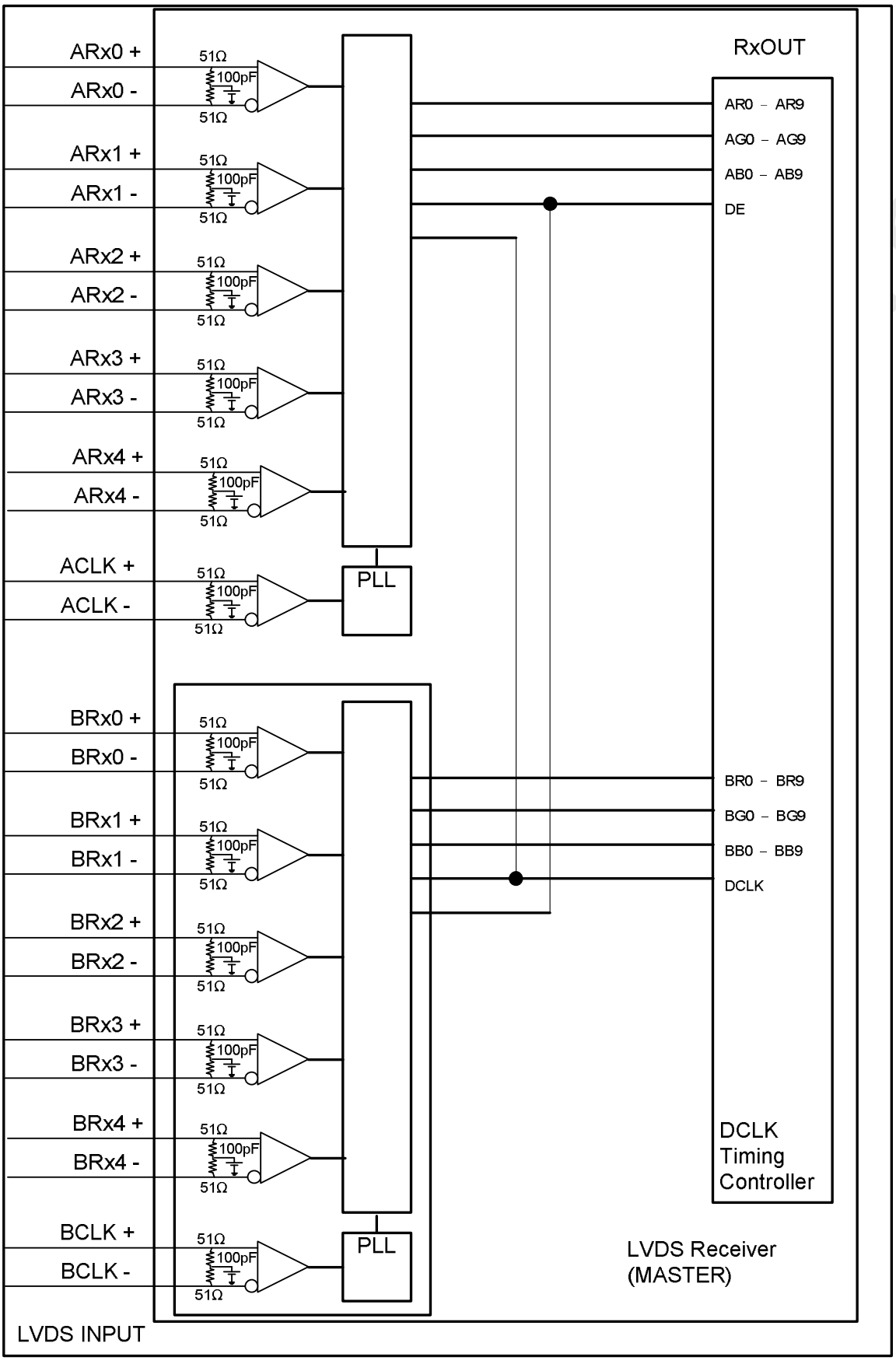
Note (2) Pin 13: Internal PWM control (use pin 13): Pin 12 must open.

Note (3) Pin 12 and Pin 13 can't open in the same period.

CN2~CN8: CP042EP1MFB-LF (Cvilux)

Pin №	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

Notes:

(1) The system must have the transmitter to drive the module.

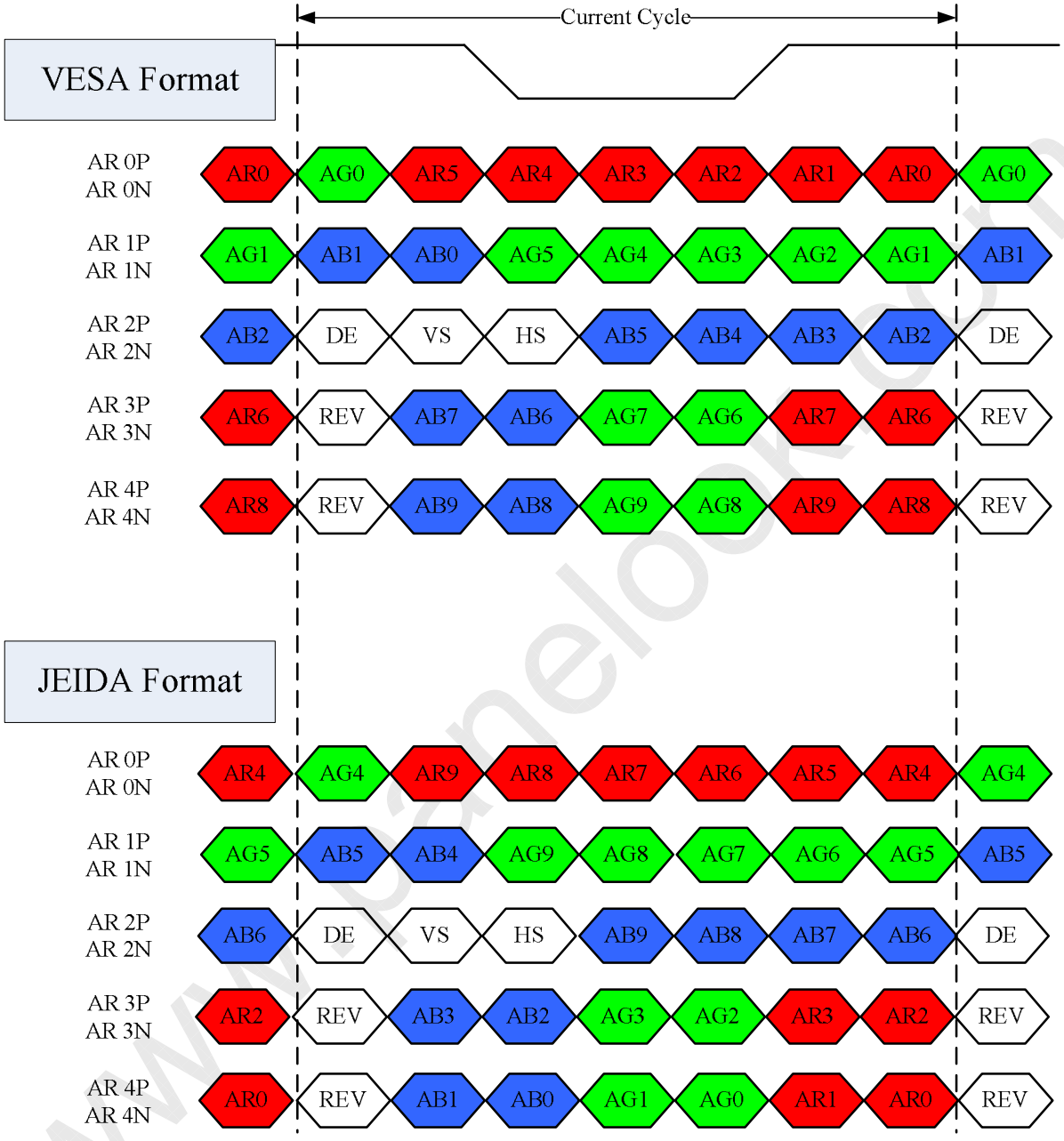
(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

(3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.5 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

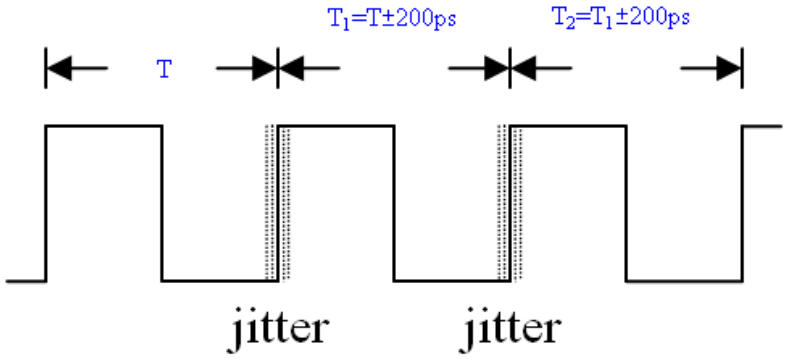
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	78	MHZ	-
	Input cycle to cycle jitter	Trcl	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	30	—	50	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	—	—	ps	- -(5)
	Hold Time	Tlvhd	600	—	—	ps	
Vertical Active Display Term	Frame Rate	Fr6	47	50	53	Hz	(6)
		Fr5	57	60	62		
	Total	Tv	1110	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	30	45	55	Th	-
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	-
	Blank	Thb	90	140	190	Tc	-

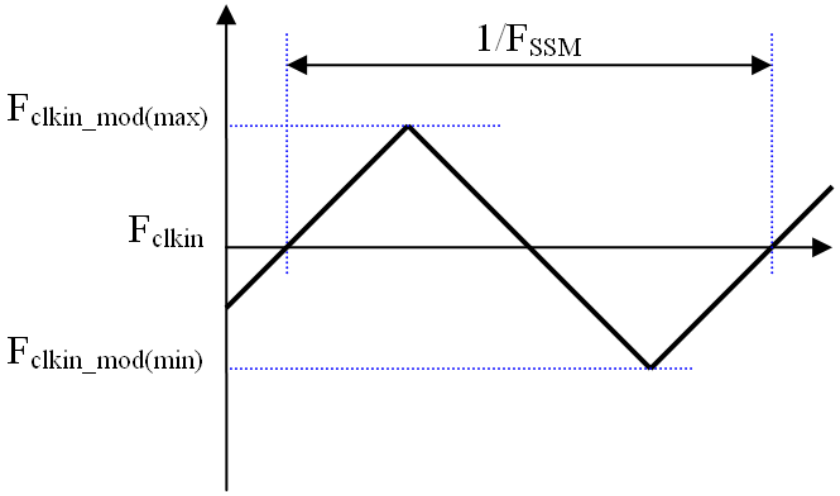
Note (1) Please make sure the range of frame rate has follow the below equation：

$Fr(max) \geqq Fclkin \ / \ TvxTh \leqq Fr(min)$

Note (2) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

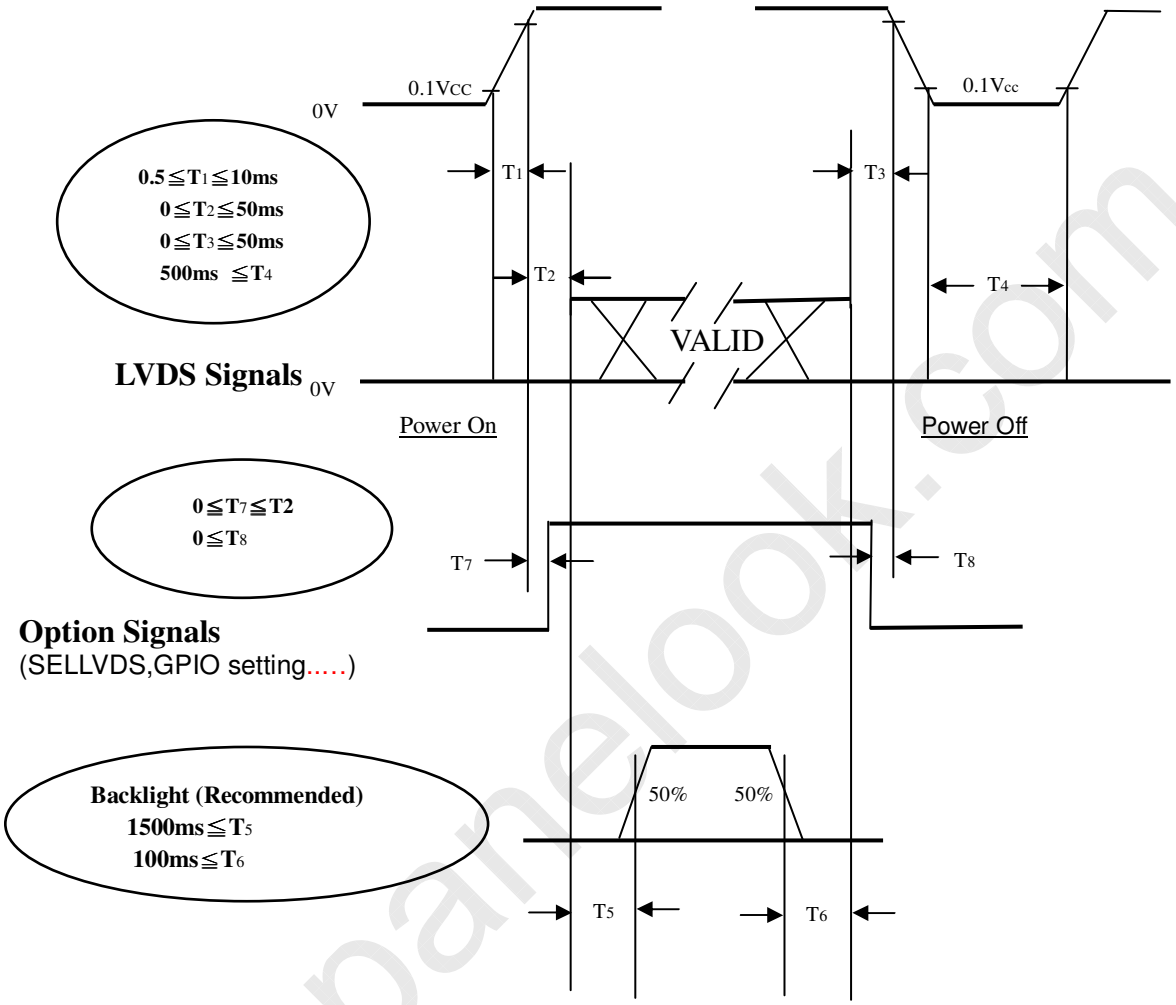


Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note:

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	12.0±0.5	mA
Oscillating Frequency (Inverter)	F_W	40±3	KHz
Vertical Frame Rate	Fr	60	Hz

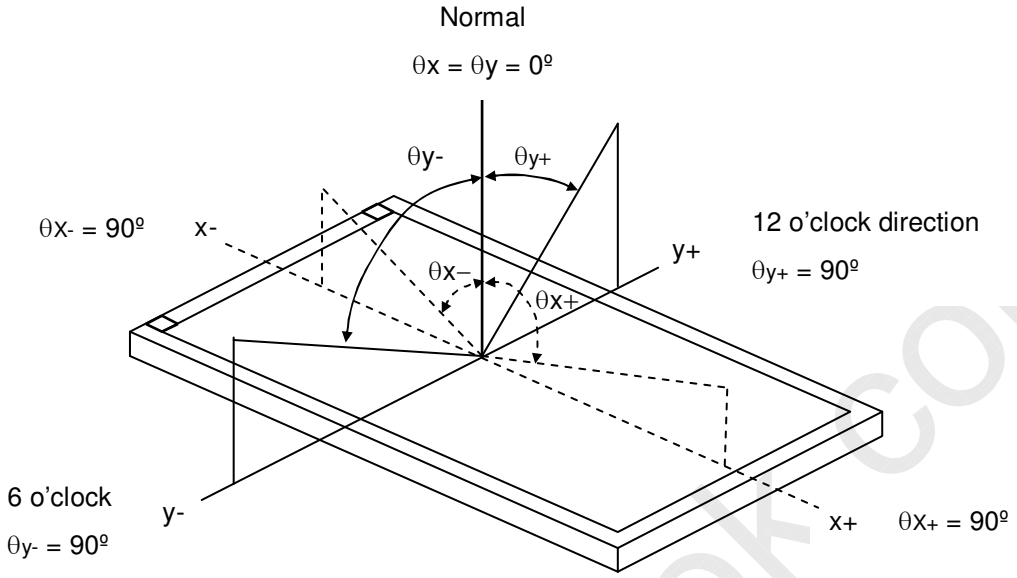
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing angle at normal direction	4500	6000	-	-	Note (2)
Response Time		Gray to gray		-	6.5	12	ms	Note (3)
Center Luminance of White		L_C		360	450	-	cd/m^2	Note (4)
White Variation		δW		-	-	1.3	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ.-0.03	0.633	Typ.+0.03	-	Note (6)
		Ry			0.324		-	
	Green	Gx			0.284		-	
		Gy			0.599		-	
	Blue	Bx			0.147		-	
		By			0.048		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut			70	72	-	%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	Note (1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

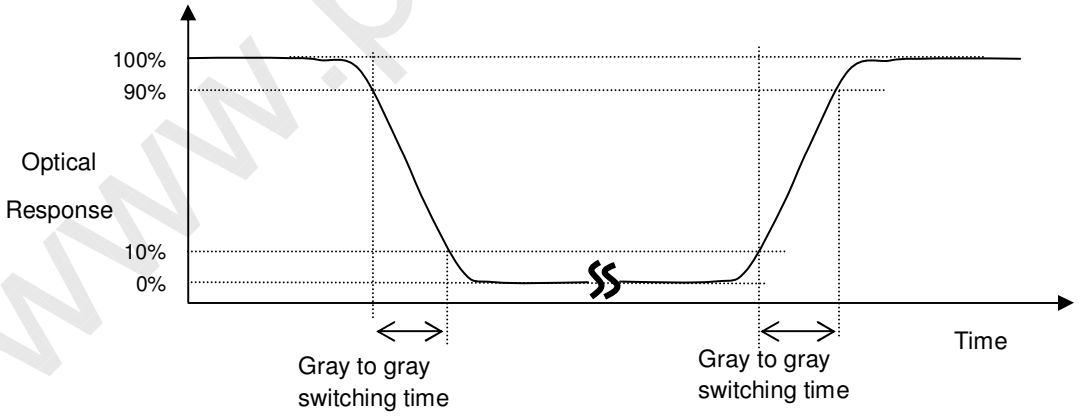
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7)

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other .

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

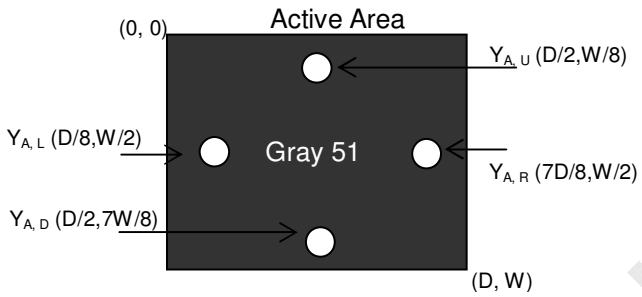
$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

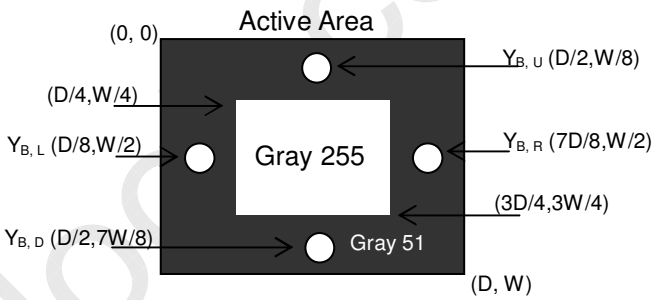
Where:

(a)

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)

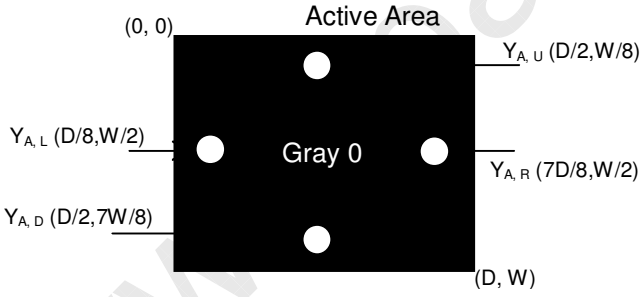


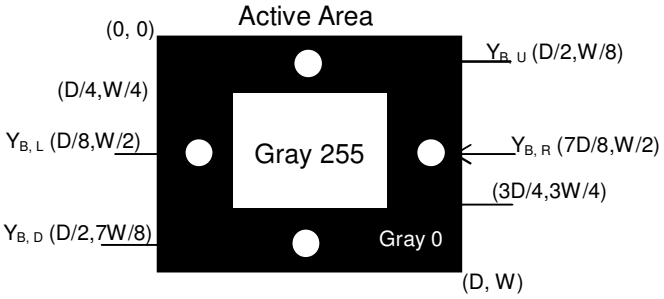


(b)

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

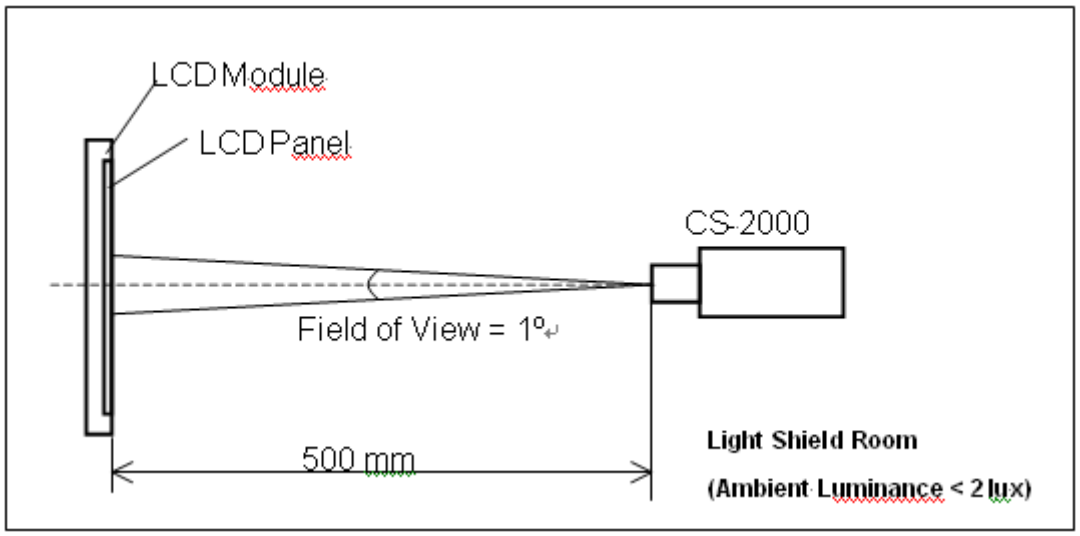
Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)





Note (6) Measurement Setup:

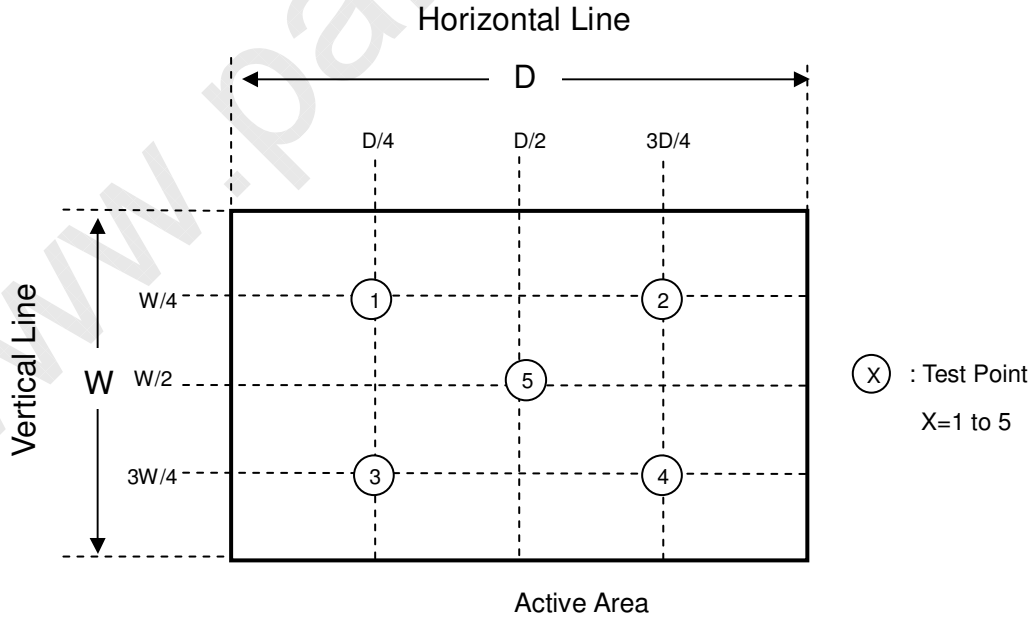
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

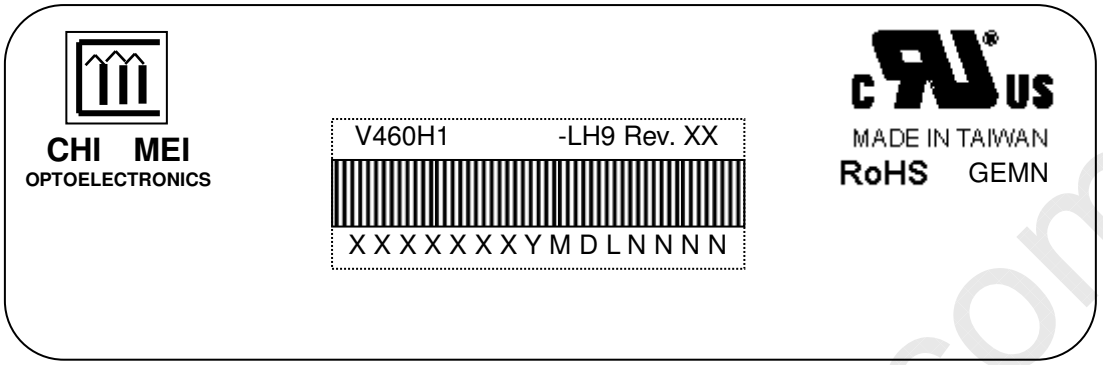
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

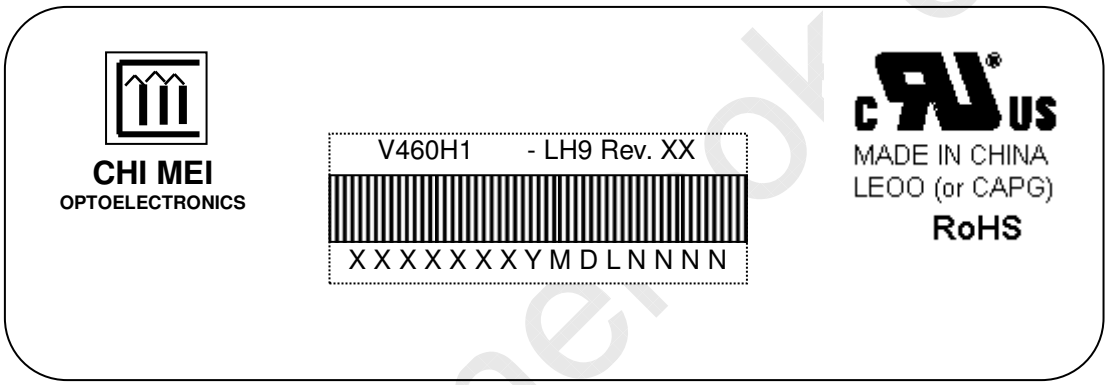


8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

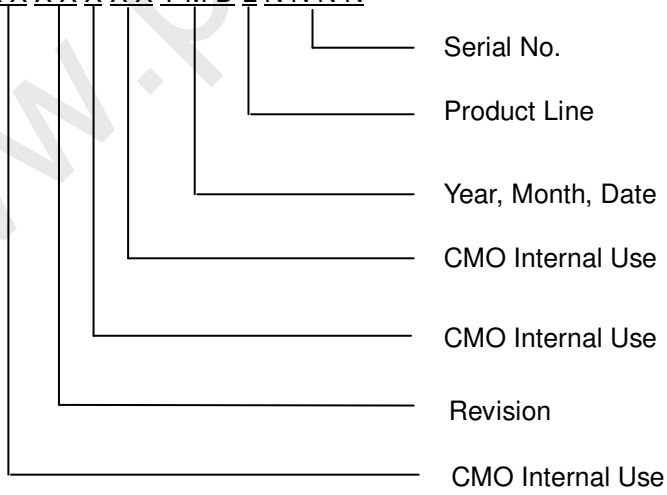




(a) Model Name: V460H-LH9

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X Y M D L N N N N



(d) Production Location:XXXX, for example:TAIWAN or CHINA .

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 3 LCD TV modules / 1 Box

(2) Box dimensions : 1144(L)x 266(W)x 725(H)mm

(3) Weight : approximately 45Kg (3 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

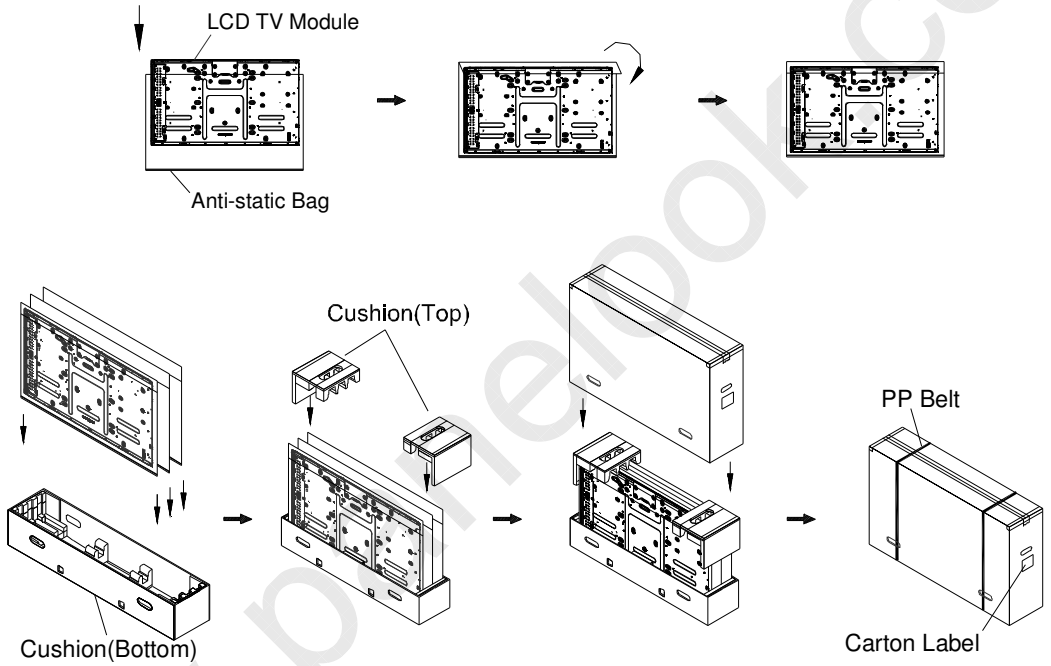
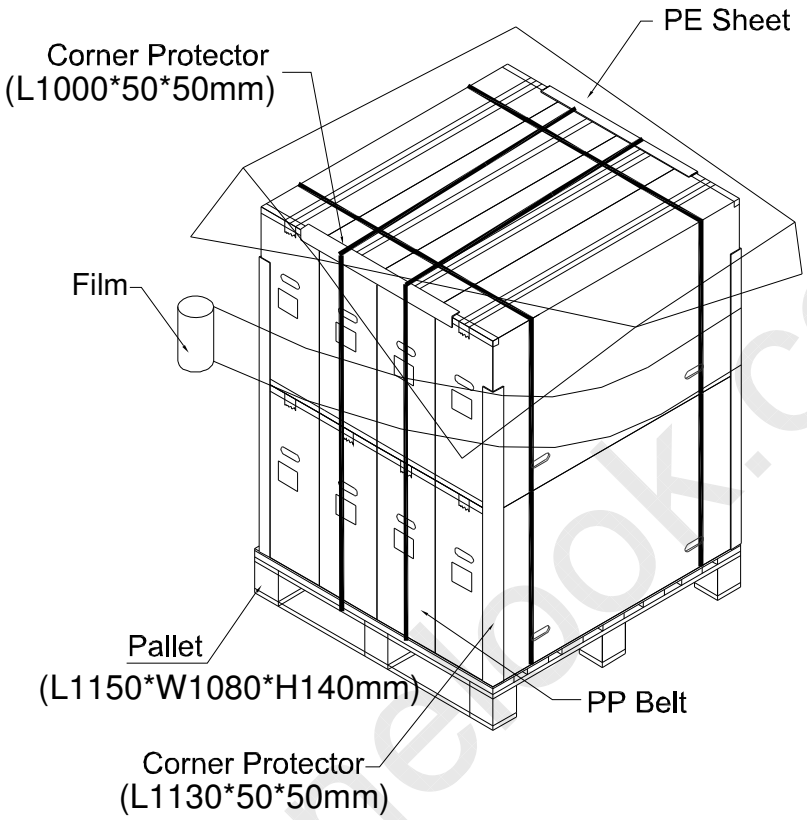


Figure.9-1 packing method

Air Transportation &

Sea / Land Transportation (40ft Container)



Sea / Land Transportation (40ft HQ Container)

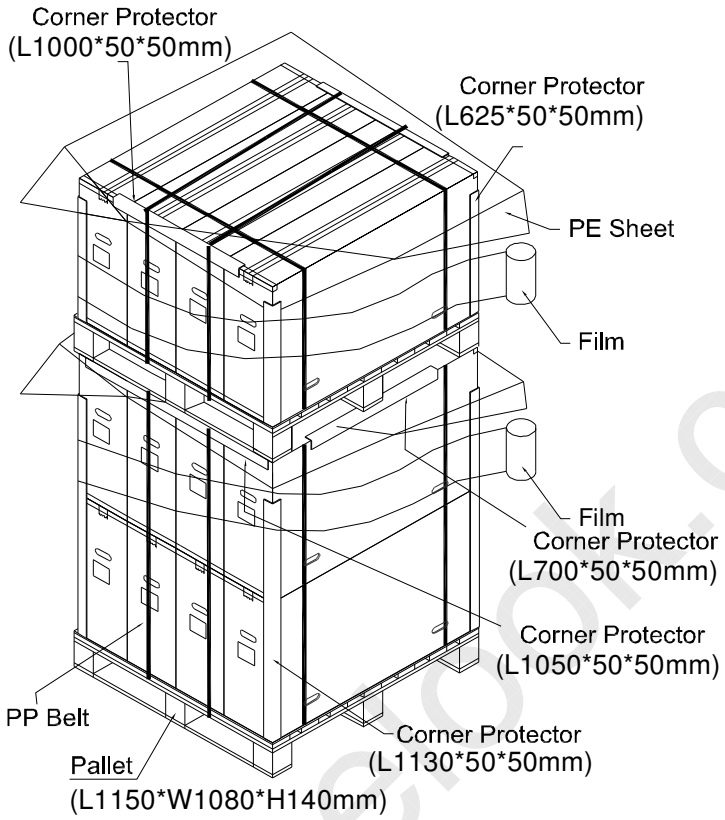


Figure.9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

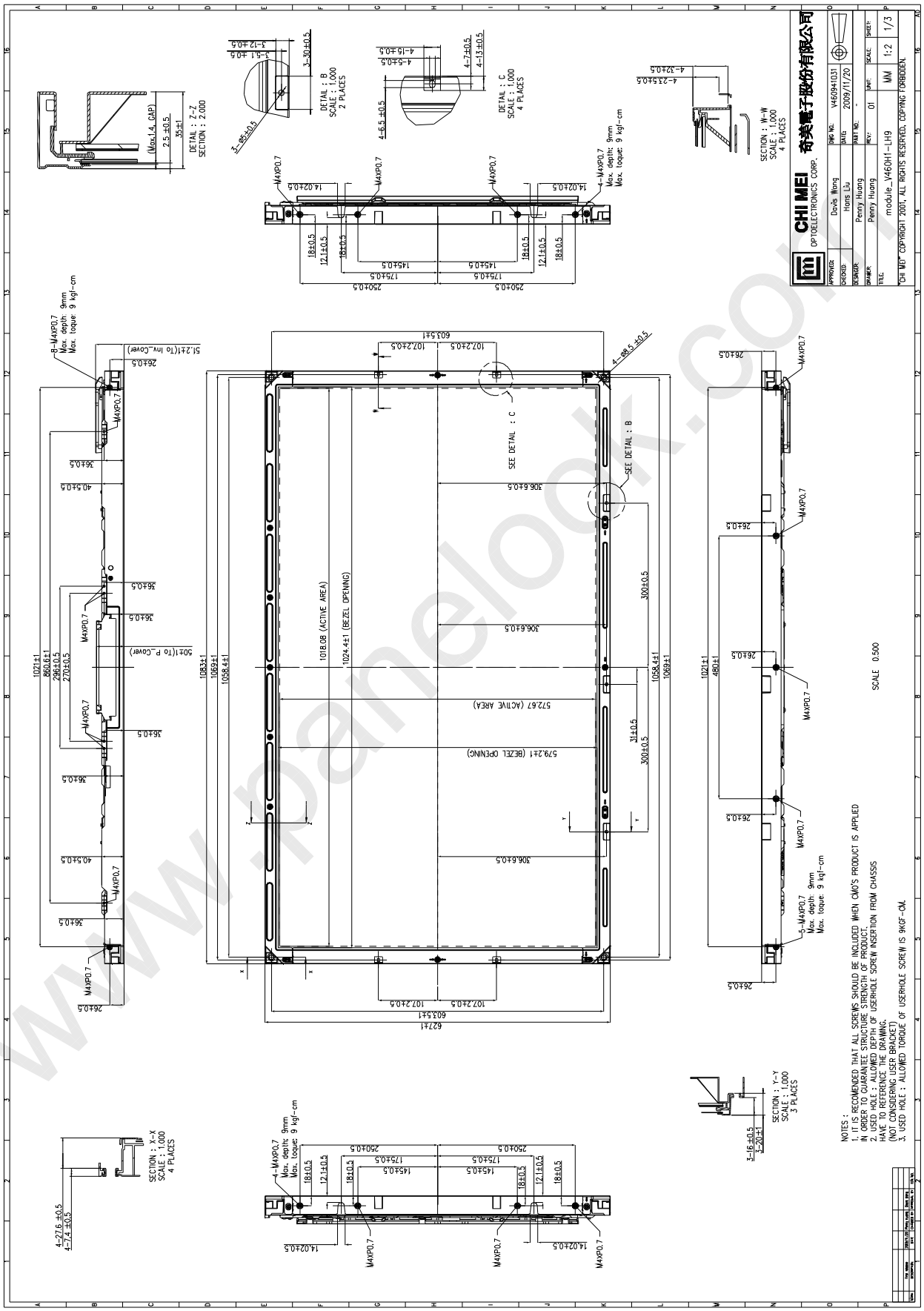
10.3 SAFETY STANDARDS

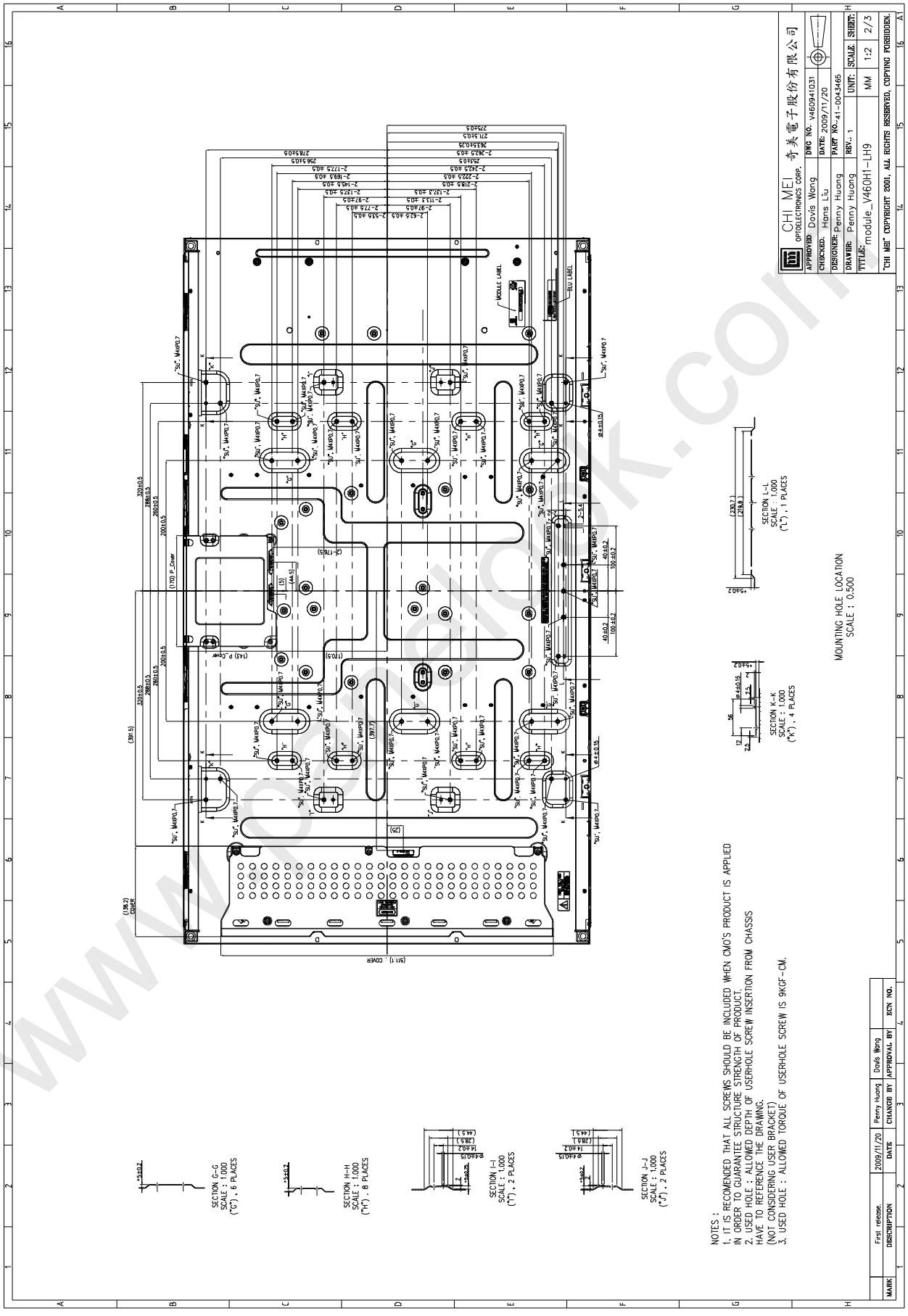
The LCD module should be certified with safety regulations as follows:

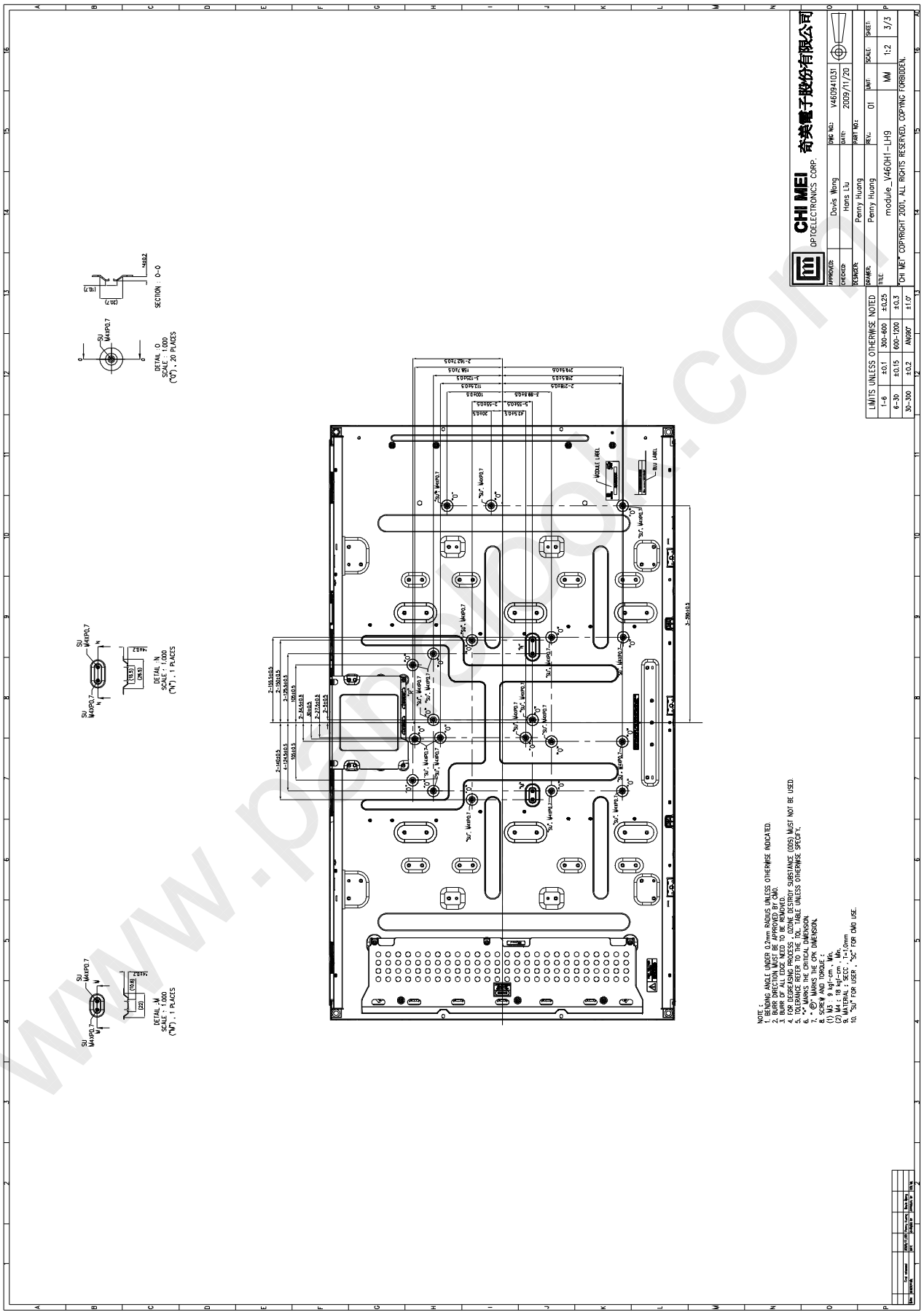
Regulatory	Item	Standard
Information Technology equipment	UL	UL 60950-1: 2003
	cUL	CAN/CSA C22.2 No.60950-1-03
	CB	IEC 60950-1:2001
Audio/Video Apparatus	UL	UL 60065: 2003
	cUL	CAN/CSA C22.2 No.60065-03
	CB	IEC 60065:2001

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

11. MECHANICAL CHARACTERISTIC







Appendix – TWO Wire BUS INTRODUCTION

A.1 PIN ASSIGNMENT

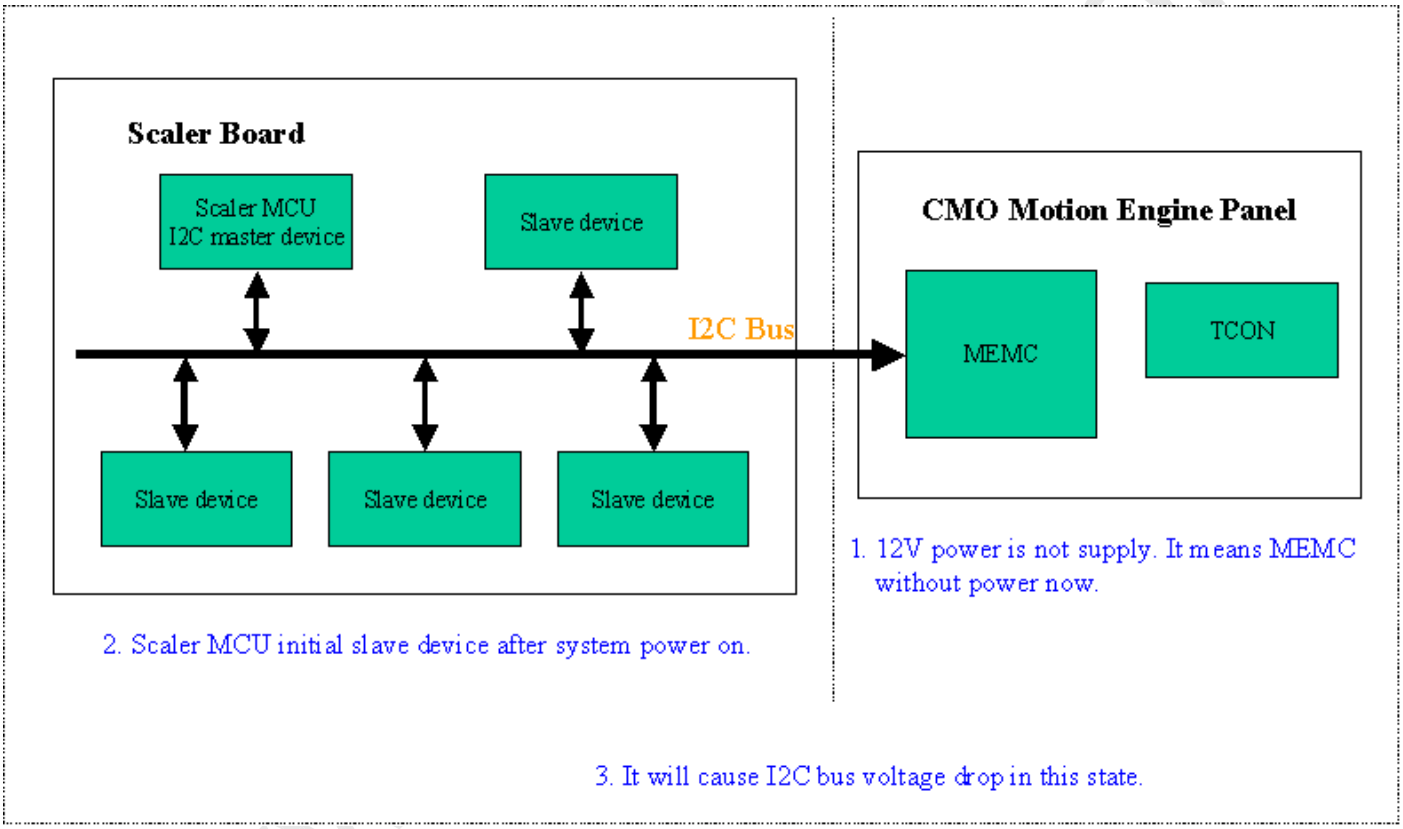
51pins LVDS connector

Pin8: SCL

Pin9: SDA

A.2 I2C BUS APPLICATION NOTE

I2C bus: (The I2C bus must for MEMC only or prevent the I2C bus voltage drop down in initial state)



A.3 TWO WIRE BUS DEVICE ADDRESS

Two wire device address: default is 0x40, 1 byte

Two wire command: the range is 0x00 to 0xFF, 1 byte, see the two wire command table.

Two wire bus format:

Device Address : 0x40 default							
D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	W/R

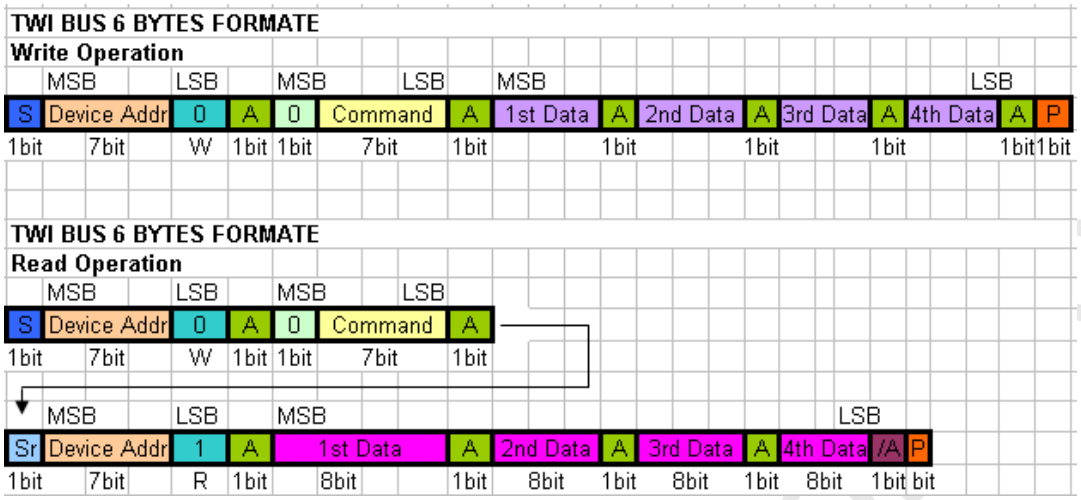
Command							
D7	D6	D5	D4	D3	D2	D1	D0
L	x	x	x	x	x	x	x

W/R	write : 0; Read : 1
L	1 : 1Byte Data Length; 0: 4Byte Data Length
S	TWI-Bus Start condition from master
Sr	TWI-Bus Start condition from master
A	TWI-Bus Acknowledge bit from master
/A	TWI-Bus Not Acknowledge bit from salve
P	TWI-Bus Stop condition from master
Data	TWI Bus Data from master
Data	TWI Bus Data from salve

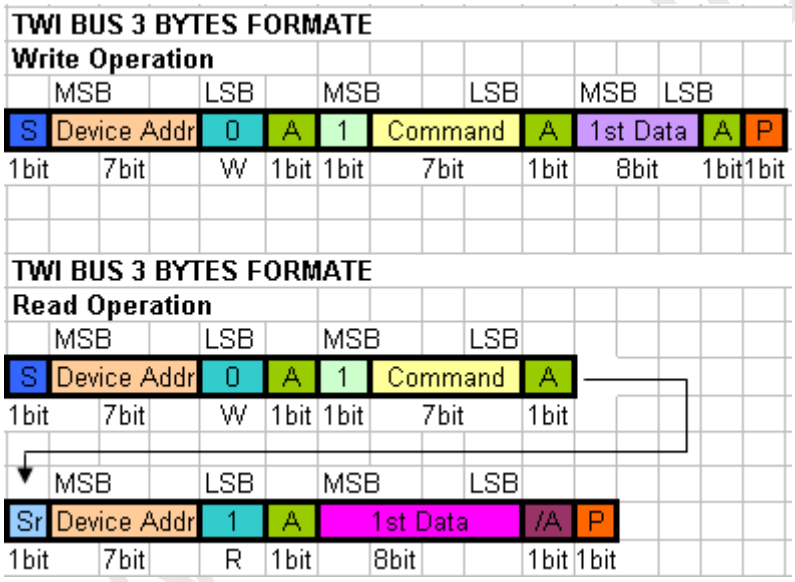
A.4 TWO WAY TO CONTROL THE TWO WIRE BUS

There are two options to control the two wires bus command.

Two wire bus 6 bytes format



Two wire bus 3 bytes format



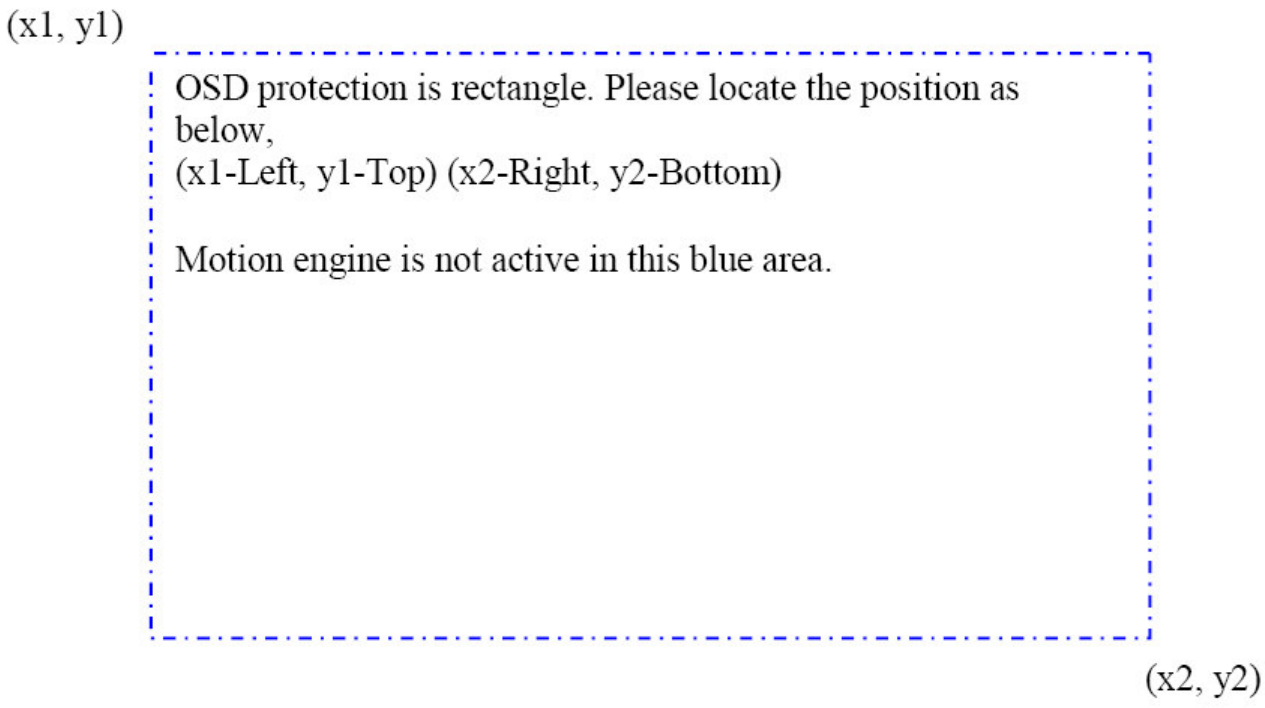
Note:

A transmission basically consists of a START condition, a SLA+R/W, one or more data packets and a STOP condition. An empty message, consisting of a START followed by a STOP condition, is illegal. Note that the wired-ANDing of the SCL line can be used to implement handshaking between the master and the slave. The slave can extend the SCL low period by pulling the SCL line low. This is useful if the clock speed set up by the master is too fast for the slave, or the slave needs extra time for processing between the data transmissions. The slave extending the SCL low period will not affect the SCL high period, which is determined by the master. As a consequence, the slave can reduce the TWI data transfer speed by prolonging the SCL duty cycle.

A.5 TWO WIRE BUS COMMAND TABLE

There is two wire bus command table.

Command Name		Access Mode	Description
All OSD Protection	0x00	R/W	OSDx Enable Flag Contorl
OSD1_Start_Protection	0x01	R/W	OSD1 Protection Start Position
OSD2_Start_Protection	0x02	R/W	OSD2 Protection Start Position
OSD3_Start_Protection	0x03	R/W	OSD3 Protection Start Position
OSD4_Start_Protection	0x04	R/W	OSD4 Protection Start Position
OSD1_End_Protection	0x05	R/W	OSD1 Protection End Position
OSD2_End_Protection	0x06	R/W	OSD2 Protection End Position
OSD3_End_Protection	0x07	R/W	OSD3 Protection End Position
OSD4_End_Protection	0x08	R/W	OSD4 Protection End Position
Demo Window	0x09	R/W	ME Performance Demo
MEMC Level	0x0A	R/W	ME Performance
GV Mode	0x0B	R/W	ME Operation
Blanking	0x0C	R/W	Blinking the screen
RPF	0x0D	R/W	Rotation picture function



Enable All OSD Protection

AllOSD Protection : 0x00										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D28	Unused
	Unused				OSDx				D27	OSD4 flag 1 : On ; 0 : Off
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D26	OSD3 flag 1 : On ; 0 : Off
	Unused								D25	OSD2 flag 1 : On ; 0 : Off
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8	D24	OSD1 flag 1 : On ; 0 : Off
	Unused								D23~D0	Unused
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused									

AllOSD Protection : 0x80										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D4	Unused
	Unused				OSDx				D3	OSD4 flag 1 : On ; 0 : Off
									D2	OSD3 flag 1 : On ; 0 : Off
									D1	OSD2 flag 1 : On ; 0 : Off
									D0	OSD1 flag 1 : On ; 0 : Off

OSD # 1~4 Start Protection

OSD1_Start_Protection : 0x01 OSD2_Start_Protection : 0x02 OSD3_Start_Protection : 0x03 OSD4_Start_Protection : 0x04										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31	OSDx flag 1 : On ; 0 : Off
		Unused							D30~D27	Unused
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D26~D16	OSDx Left position
	OSD Left								D15~D11	Unused
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8	D10~D0	OSDx Top position
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	OSDx Top								Left position Max : 1919 Top position Max : 1079	

OSD # 1~4 End Protection

OSD1_End_Protection : 0x05 OSD2_End_Protection : 0x06 OSD3_End_Protection : 0x07 OSD4_End_Protection : 0x08										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D27	Unused
	Unused								D26~D16	OSDx Right position
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D15~D11	Unused
	OSD Right								D10~D0	OSDx Bottom position
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	OSD Bottom								Right position Max : 1919 Bootom position Max : 1079	

Demo Window

Demo Window : 0x09										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D25	Unused
	Unused								D24	Demo Window 1 : On ; 0 : Off
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0	Unused
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused									
Demo Window : 0x89										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused
	Unused								D0	Demo Window 1 : On ; 0 : Off

MEMC Level

ME Level : 0x0A										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D29	Unused
	Unused			ME Level					D28~24	ME Level 0~16
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16		
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		0 : Strong 1 : Normal 2 : Weak 3 : Off
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused								D23~D0	Unused
ME Level : 0x8A										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D5	Unused
	Unused			ME Level					D4~D0	ME Level 0~16
										0 : Strong 1 : Normal 2 : Weak 3 : Off

GV Mode

GV Mode : 0x0B										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D25	Unused
	Unused								D24	1 : Graphic ; 0 : Video
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0	Unused
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused									
GV Mode : 0x8B										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused
	Unused								D0	1 : Graphic ; 0 : Video

Blanking (Enable/Disable)

Blanking : 0x0C										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D26	Unused
	Unused								D24	Blanking; 1 : On ; 0 : Off
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0	Unused
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	When the input signal is unstable, the screen should be blanked.	
	Unused									

Blanking : 0x8C										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused
	Unused								D0	Blanking; 1 : On ; 0 : Off

RPF : 0x0D										
4 Bytes Data Length										
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D25	Unused
	Unused								D24	1 : Rotation ; 0 : Default
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0	Unused
	Unused									
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8		
	Unused									
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0		
	Unused									

GV Mode : 0x8D										
1 Byte Data Length										
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused
	Unused								D0	1 : Rotation ; 0 : Default

A.6 TWO WIRE BUS REQUIREMENT

Symbol	Parameter	Condition	Min	Max	Unite
V_{IL}	Input Low-voltage		0	0.7	V
V_{IH}	Input High-voltage		2.7	3.3	V
V_{hys}(1)	Hysteresis of Schmitt Trigger Inputs		0.16	–	V
V_{OL}(1)	Output Low-voltage	3 mA sink current	0	0.4	V
t_r(1)	Rise Time for both SDA and SCL		$20 + 0.1C_b$(3)(2)	300	ns
t_{of}(1)	Output Fall Time from V_{IHmin} to V_{ILmax}	10 pF < C_b < 400 pF(1)	$20 + 0.1C_b$(3)(2)	250	ns
t_{SP}(1)	Spikes Suppressed by Input Filter		0	50(2)	ns
I_i	Input Current each I/O Pin	$0.1V_{CC} < V_i < 0.9V_{CC}$	-10	10	µA
C_i(1)	Capacitance for each I/O Pin		–	10	pF
f_{SCL}	SCL Clock Frequency	f_{CK}(4) > max(16f_{SCL}, 250kHz)(5)	0	400	kHz
Rp	Value of Pull-up resistor	$f_{SCL} \leq 100$ kHz	3000	$\frac{1000ns}{C_b}$	Ω
		$f_{SCL} > 100$ kHz	3000	$\frac{300ns}{C_b}$	Ω
$t_{HD;STA}$	Hold Time (repeated) START Condition	$f_{SCL} \leq 100$ kHz	4.0	–	µs
		$f_{SCL} > 100$ kHz	0.6	–	µs
t_{LOW}	Low Period of the SCL Clock	$f_{SCL} \leq 100$ kHz(6)	4.7	–	µs
		$f_{SCL} > 100$ kHz(7)	1.3	–	µs
t_{HIGH}	High period of the SCL clock	$f_{SCL} \leq 100$ kHz	4.0	–	µs
		$f_{SCL} > 100$ kHz	0.6	–	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100$ kHz	4.7	–	µs
		$f_{SCL} > 100$ kHz	0.6	–	µs
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100$ kHz	0	3.45	µs
		$f_{SCL} > 100$ kHz	0	0.9	µs
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100$ kHz	250	–	ns
		$f_{SCL} > 100$ kHz	100	–	ns
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100$ kHz	4.0	–	µs
		$f_{SCL} > 100$ kHz	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100$ kHz	4.7	–	µs
		$f_{SCL} > 100$ kHz	1.3	–	µs

A.7 THE TWO WIRE BUS SEQUENCE