CHI MEI OPTOELECTRONICS CORP.

Issued Date: Apr. 16, 2010
Model No.: V460H1-P09
Approval

TFT LCD Approval Specification

MODEL NO.:V460H1-P09

Customer: _____

Approved by: _____

Note:

Approved By	TV Product Marketing & Management Div
	Chao-Chun Chung

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Mar,01,2010	All	All	Approval Specification was first issued.
Ver 2.1	Apr,16,2010	28	9.2	Update Figures 9-1 and 9-2 are the packing method

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V460H1- P09 is a 46" TFT Liquid Crystal Display cell with driver ICs and 2ch-LVDS interface This cell supports 1920 x 1080 HDTV format and can display true 16.7M colors (8bit /color).

1.2 CHARACTERISTICS

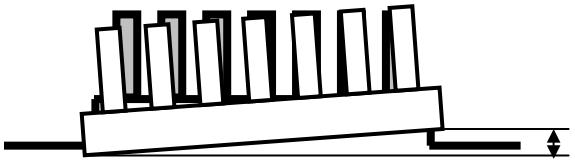
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	46
Pixels [lines]	1920 x 1080
Active Area [mm]	1018.08(H) x 572.67(V) (46" diagonal)
Sub -Pixel Pitch [mm]	0.17675(H) x 0.53025(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 2550
Physical Size [mm]	1050.58(W) x 631.92(H) * 1.78(D) Typ.
Display Mode	Tranmissive mode / Normally black
Contrast Ratio	6000:1 Typ. (Typical value measured at CMO's module)
Glass thickness (Array/CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H),+88/-88(V) Typ. (Typical value measured at CMO's module)
Color Chromaticity	Rc=(0.651, 0.326) Gc=(0.299, 0.600) Bc=(0.145, 0.082) Wc=(0.329, 0.371) (Light source is the standard light source "C" which is defined by CIE)
Cell Transparency [%]	4.4%Typ. (Typical value measured at CMO's module)
Polarizer (CF side)	Super Wide View Glare coating, 1030.18 (W) x 586.37(H). Hardness: 3H
Polarizer (TFT side)	Super Wide View, 1030.18(W) x 586.37(H).

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	2250	2550	2850	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ±0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position



+/- 0.5mm

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT (BASED ON CMO MODULE V460H1-L09)

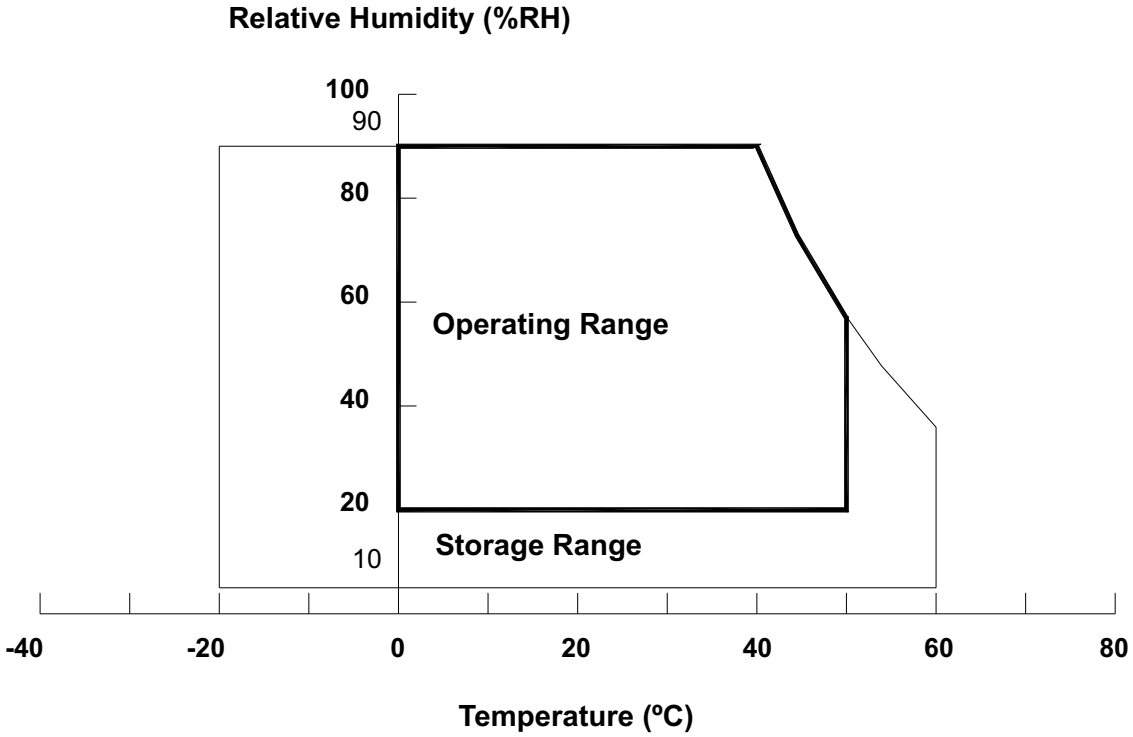
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1), (3)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2), (3)
Altitude Operating	A_{OP}	0	5000	M	(3)
Altitude Storage	A_{ST}	0	12000	M	(3)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation..



Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Storage Condition : With shipping package.

Storage temperature range : 25±5 ℃

Storage humidity range : 50±10%RH

Shelf life : a month

2.3 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL)

2.3.1 ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

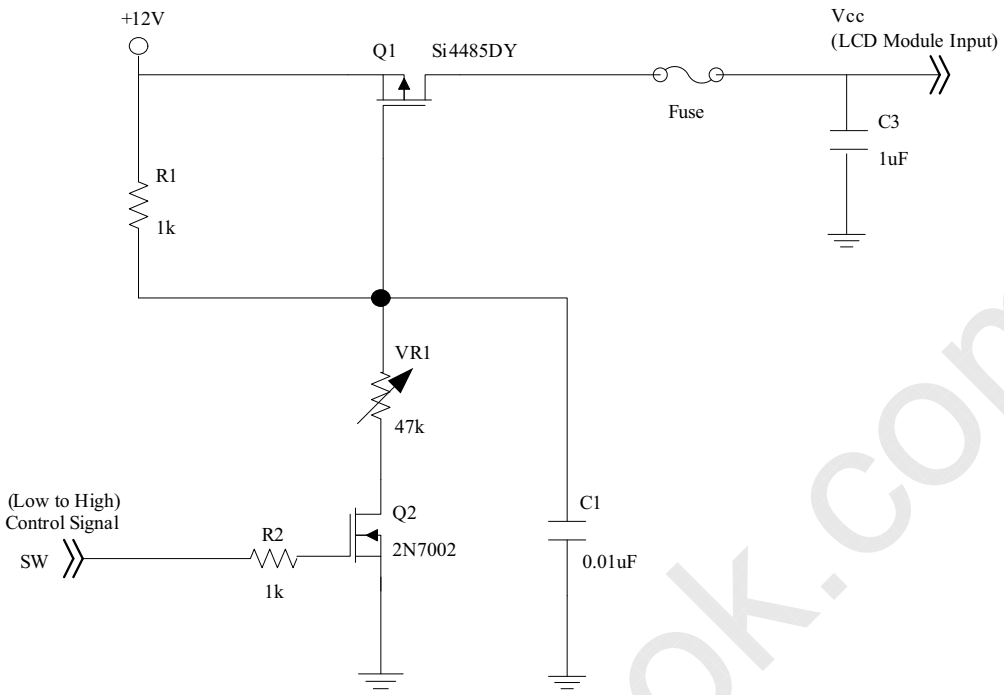
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

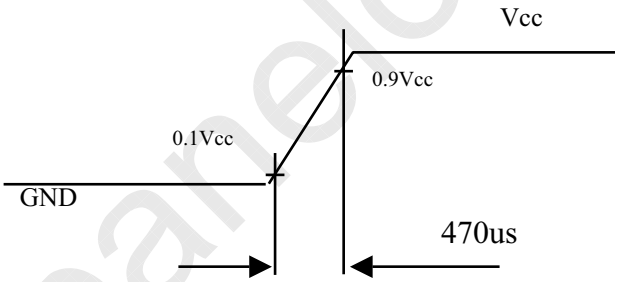
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	4.7	A	(2)
Power Supply Current	White Pattern	I_{CC}	—	0.58	—	A	(3)
	Black Pattern		—	0.5	—	A	
	Horizontal Stripe		—	1.2	1.5	A	
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	—	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

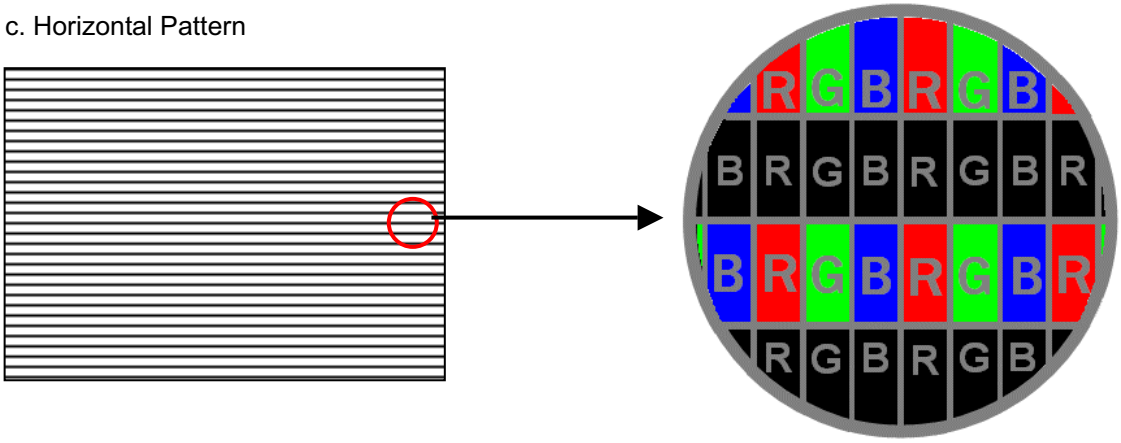
a. White Pattern

Active Area

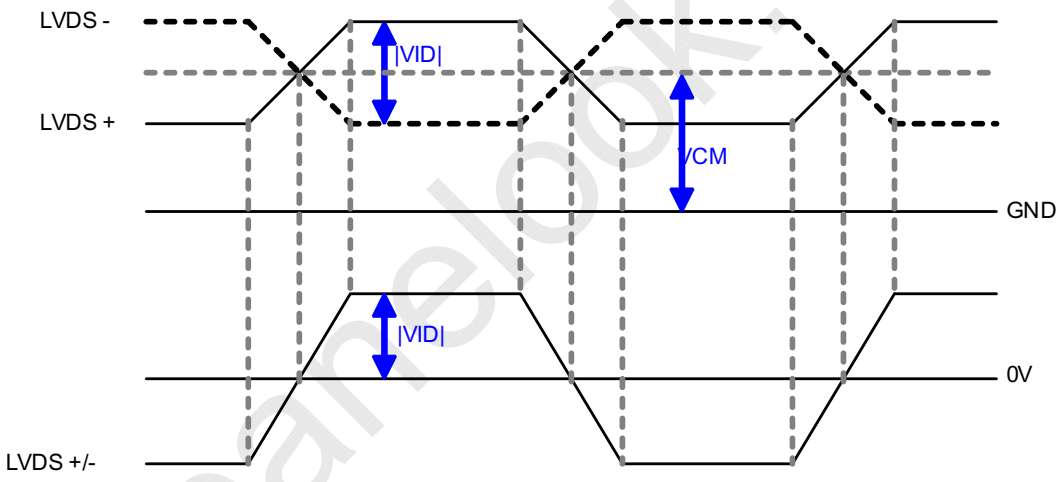
b. Black Pattern

Active Area

c. Horizontal Pattern

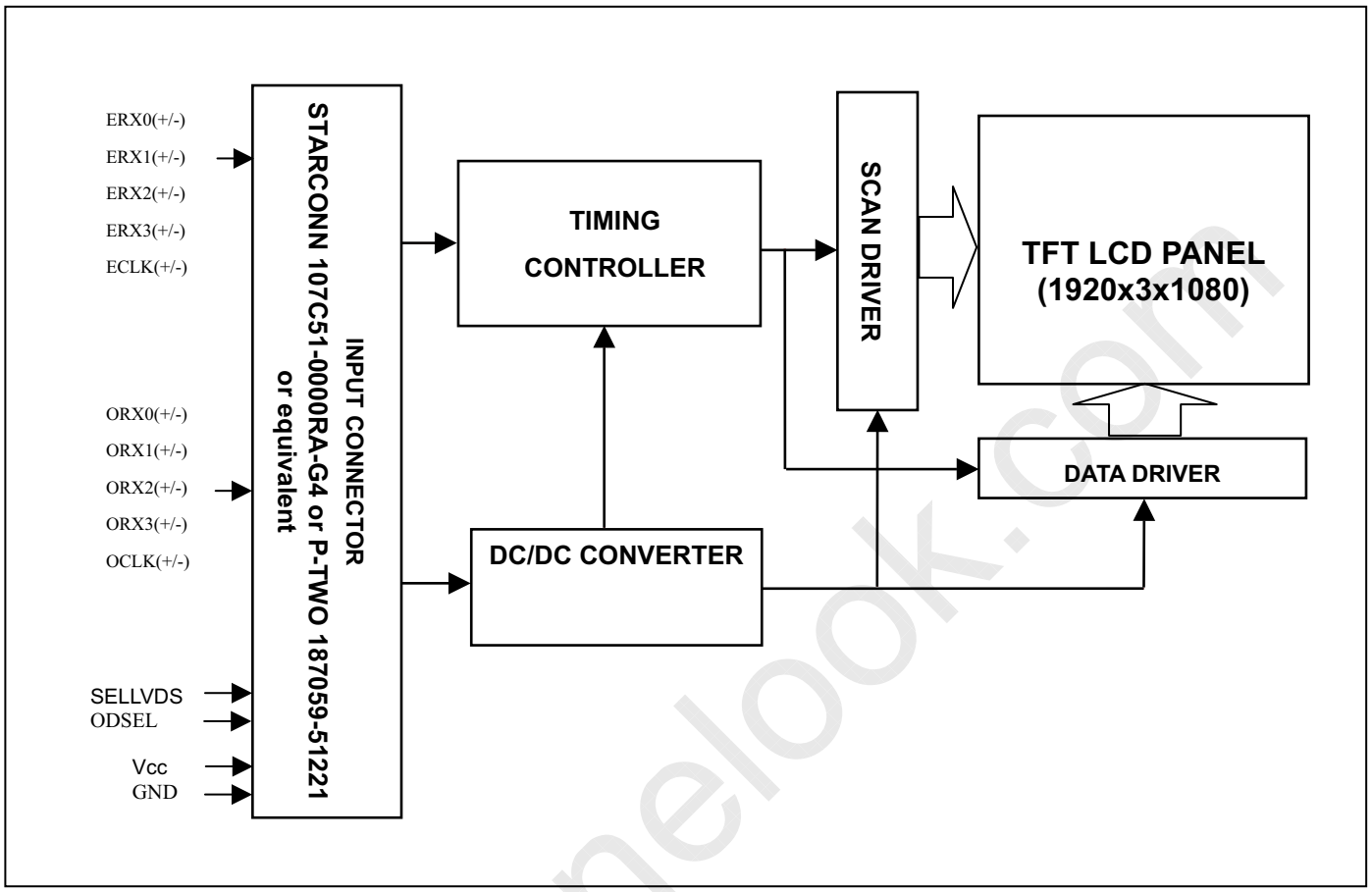


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD OPEN CELL



5. INPUT TERMINAL PIN ASSIGNMENT

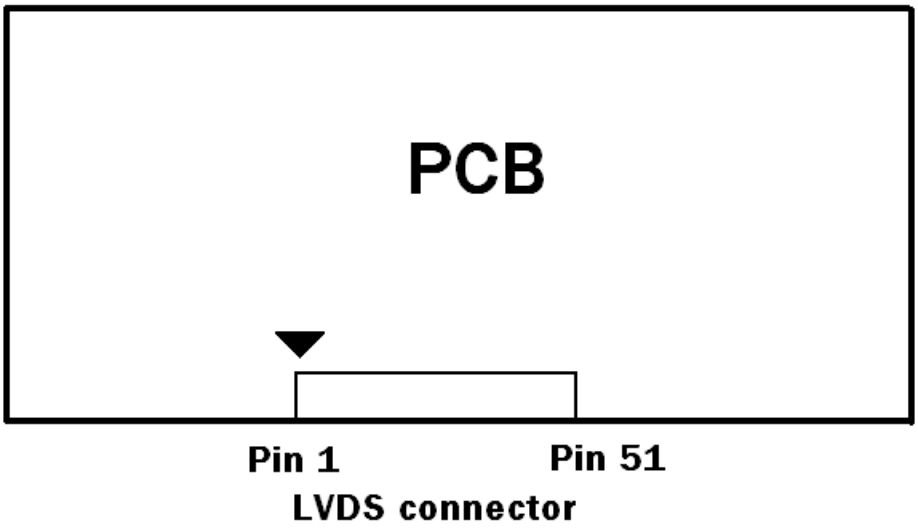
5.1 TFT LCD Module

CNF1 Connector Part No.:187059-51221 (P-TWO) or equivalent

Pin	Name	Description	Note
1	GND	Ground	
2	SCL	Series clock input	
3	SDA	Series data input	
4	N.C.	No Connection	(2)
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(3)(5)
8	N.C.	No Connection	(2)
9	ODSEL	Overdrive Lookup Table Selection	(4)(6)
10	TST_PGM	Write protect input.	(2)
11	GND	Ground	
12	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(7)
13	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	(7)
14	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	(7)
15	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	(7)
16	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	(7)
17	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	(7)
18	GND	Ground	
19	ECLK-	Even pixel Negative LVDS differential clock input.	(7)
20	ECLK+	Even pixel Positive LVDS differential clock input.	(7)
21	GND	Ground	
22	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(7)
23	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	(7)
24	N.C.	No Connection	(2)
25	N.C.	No Connection	(2)
26	GND	Ground	
27	GND	Ground	
28	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(7)
29	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	(7)
30	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	(7)
31	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	(7)
32	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	(7)
33	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	(7)
34	GND	Ground	

35	OCLK-	Odd pixel Negative LVDS differential clock input	(7)
36	OCLK+	Odd pixel Positive LVDS differential clock input	(7)
37	GND	Ground	
38	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(7)
39	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	(7)
40	N.C.	No Connection	(2)
41	N.C.	No Connection	(2)
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(2)
48	VCC	Power input (+12V)	
49	VCC	Power input (+12V)	
50	VCC	Power input (+12V)	
51	VCC	Power input (+12V)	

Note (1) LVDS connector pin order defined as follows



Note (2) Reserved for internal use. Please leave it open.

Note (3) Low = Open or connect to GND: VESA Format, High = Connect to +3.3V: JEIDA Format.

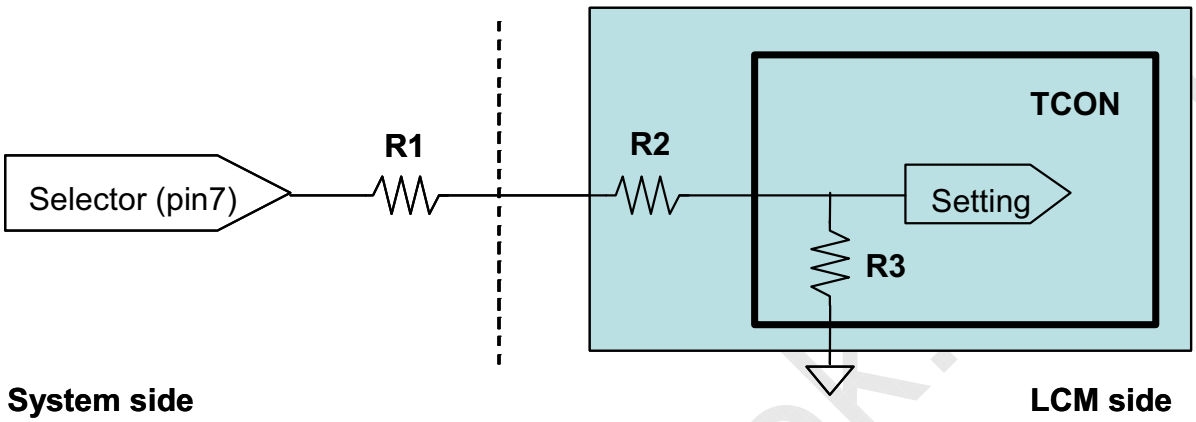
Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

Low = Open or connect to GND, High = Connect to +3.3V

ODSEL	Note
L or open	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

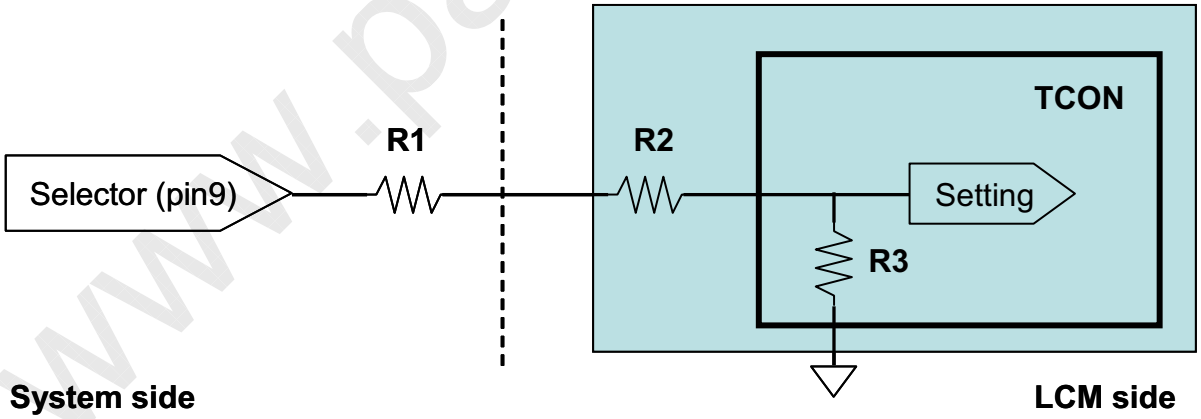
Note (5) LVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



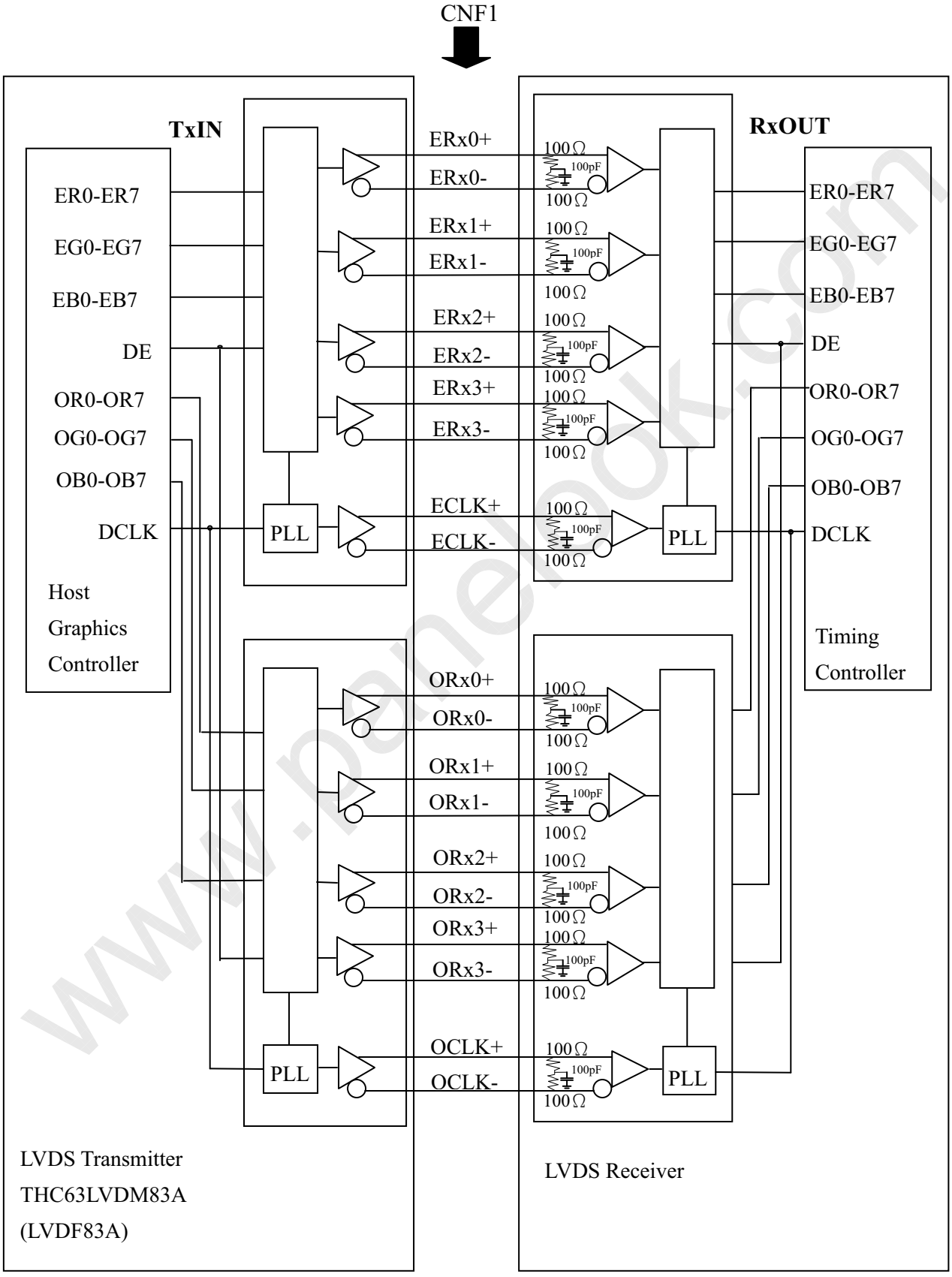
Note (6) ODSEL signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



Note (7) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.2 BLOCK DIAGRAM OF INTERFACE

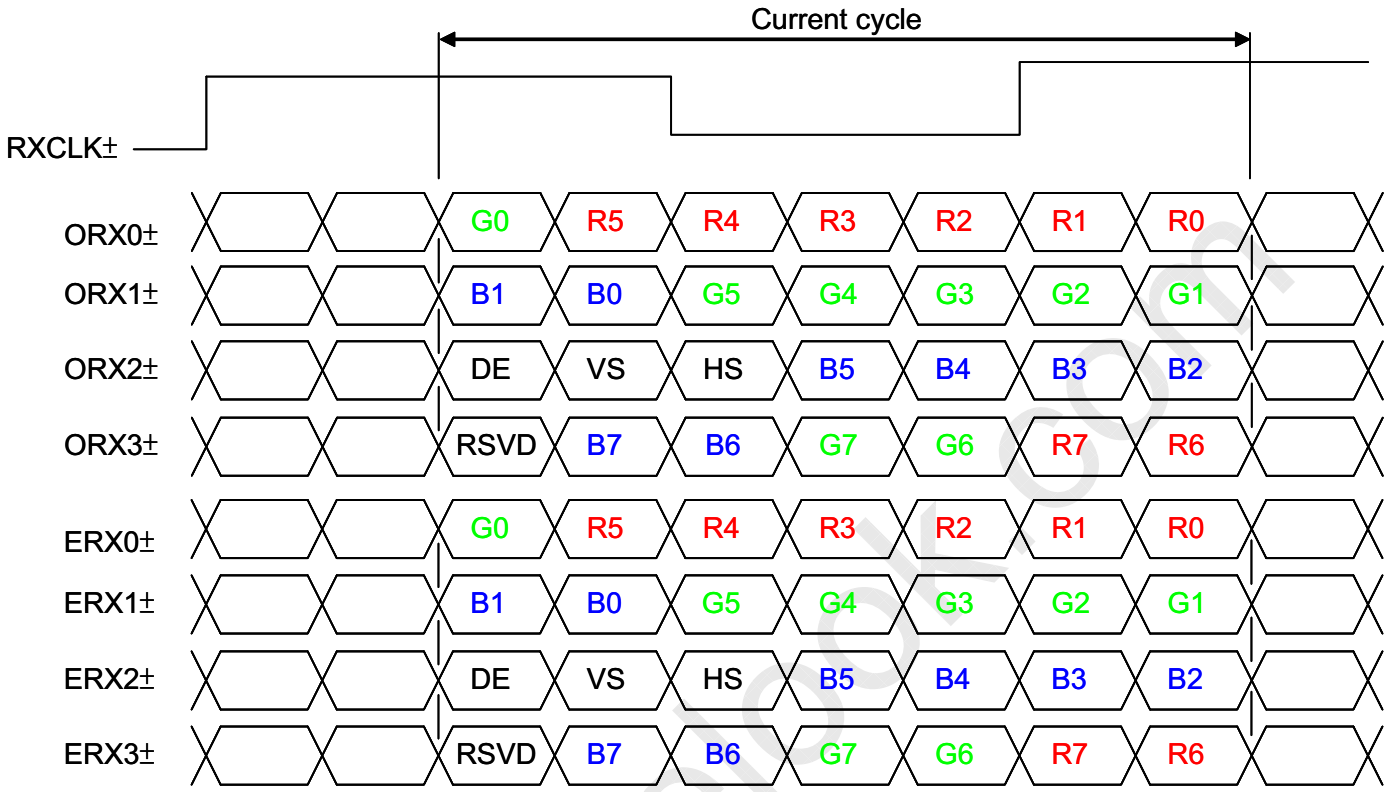


ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7 : Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

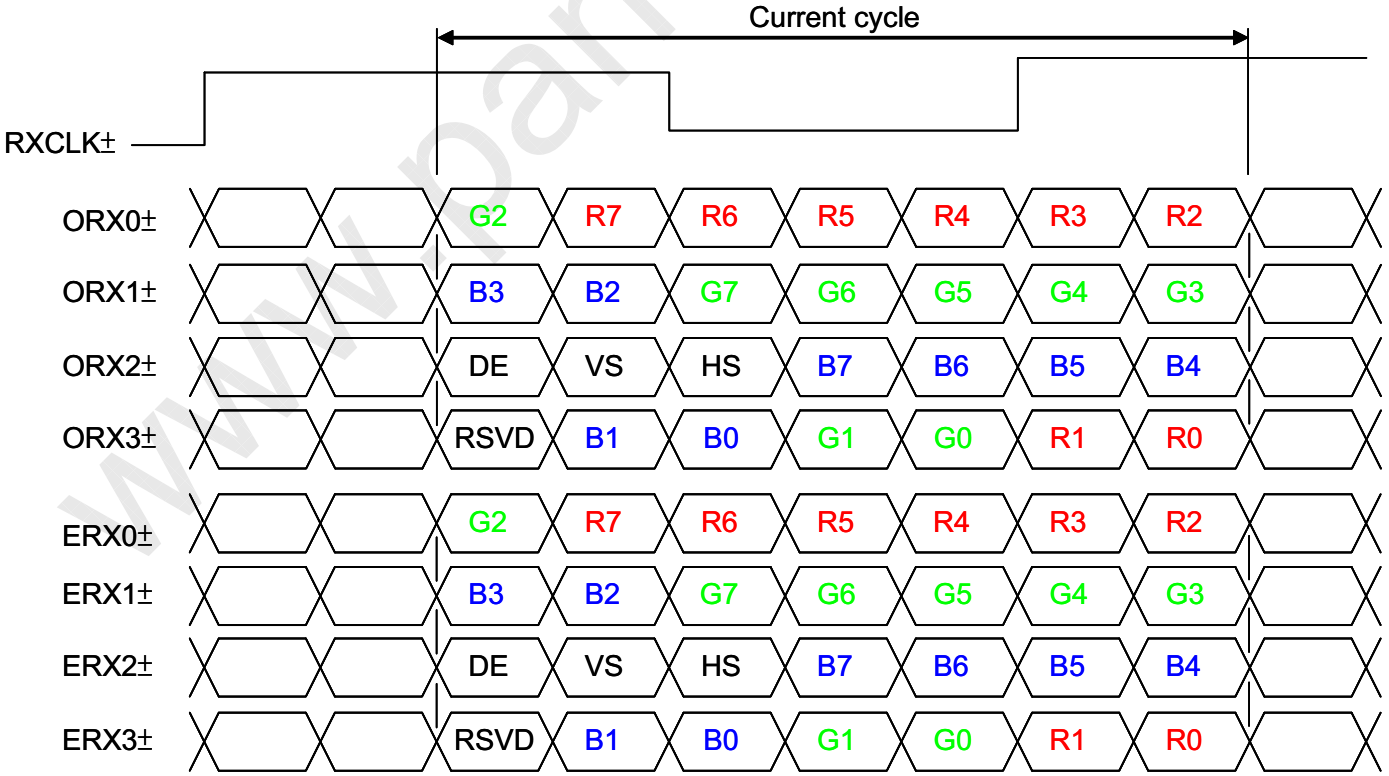
Notes (1) The system must have the transmitter to drive the module.
Notes (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
Notes (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.3 LVDS INTERFACE

VESA LVDS format：(SELLVDS pin=L or OPEN)



JEIDA LVDS format：(SELLVDS pin=H)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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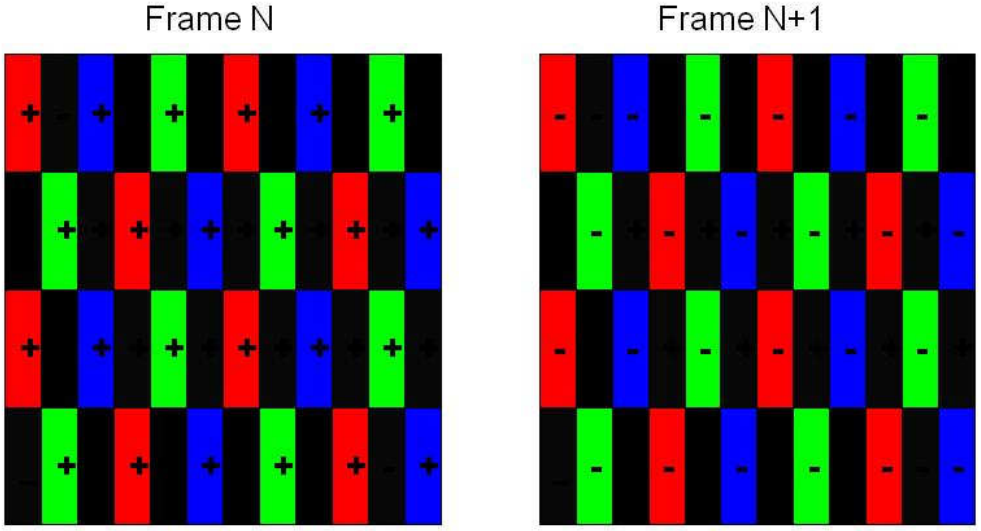
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Gray	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Scale	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 PATTERN FOR VCOM ADJUSTMENT



6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/Tc)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-200	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	—	—	ps	(5)
	Hold Time	Tlvhd	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(6)
		F_{r6}	57	60	63	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	—
	Blank	Thb	90	140	190	Tc	—

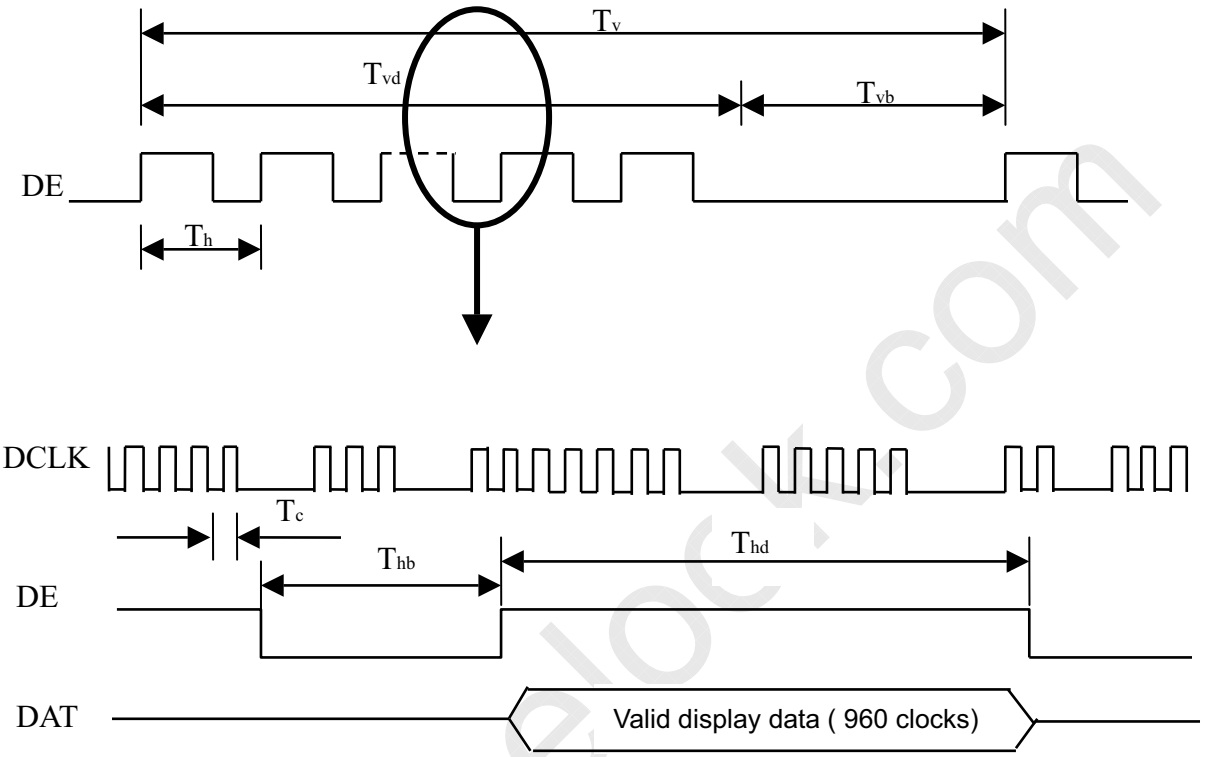
Note (1) Please make sure the range of pixel clock has follow the below equation：

$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

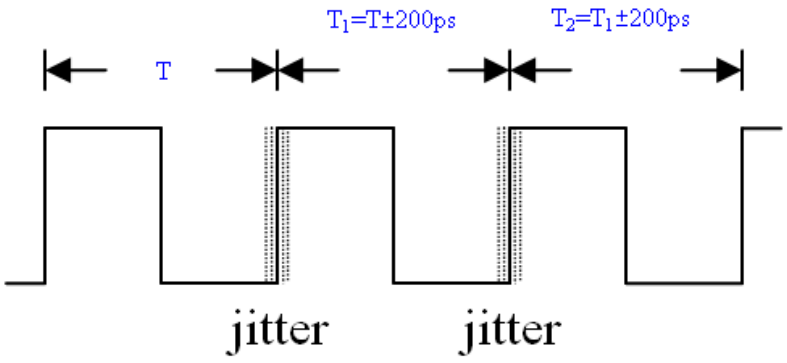
$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below：

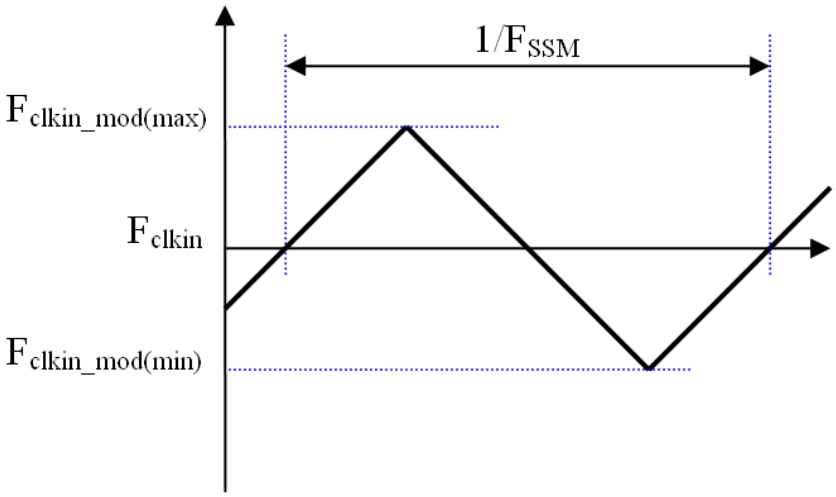
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

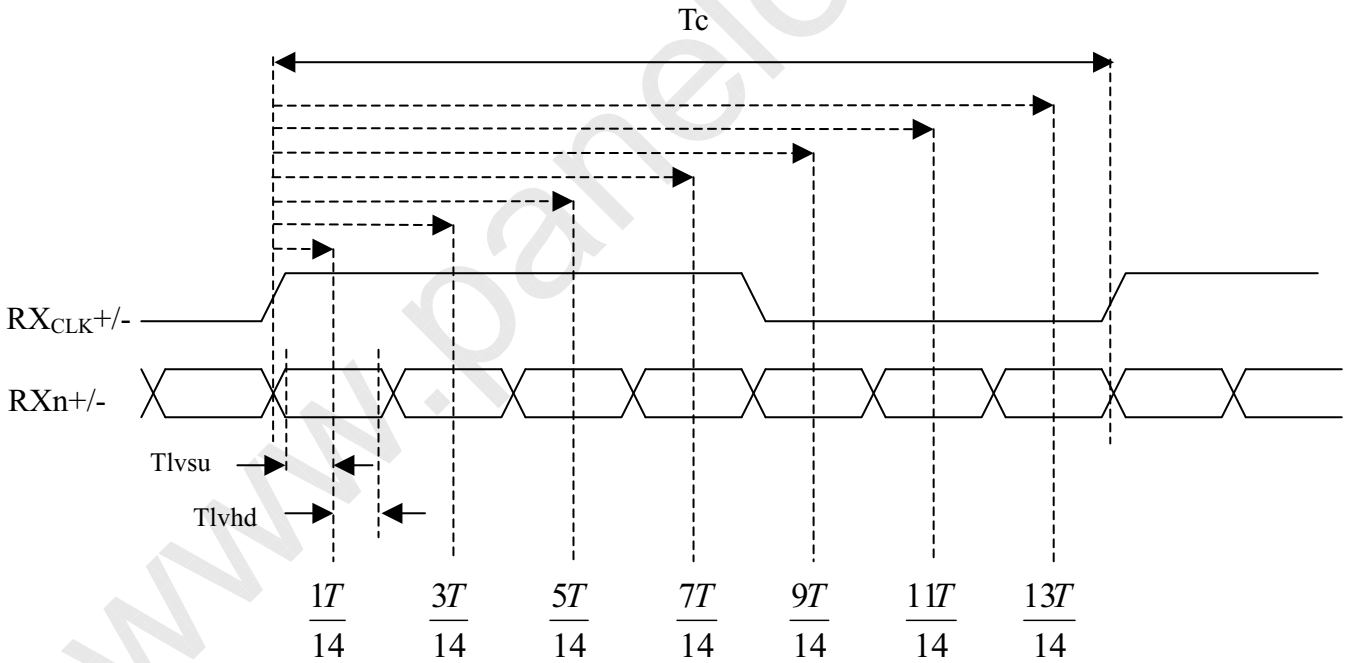


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

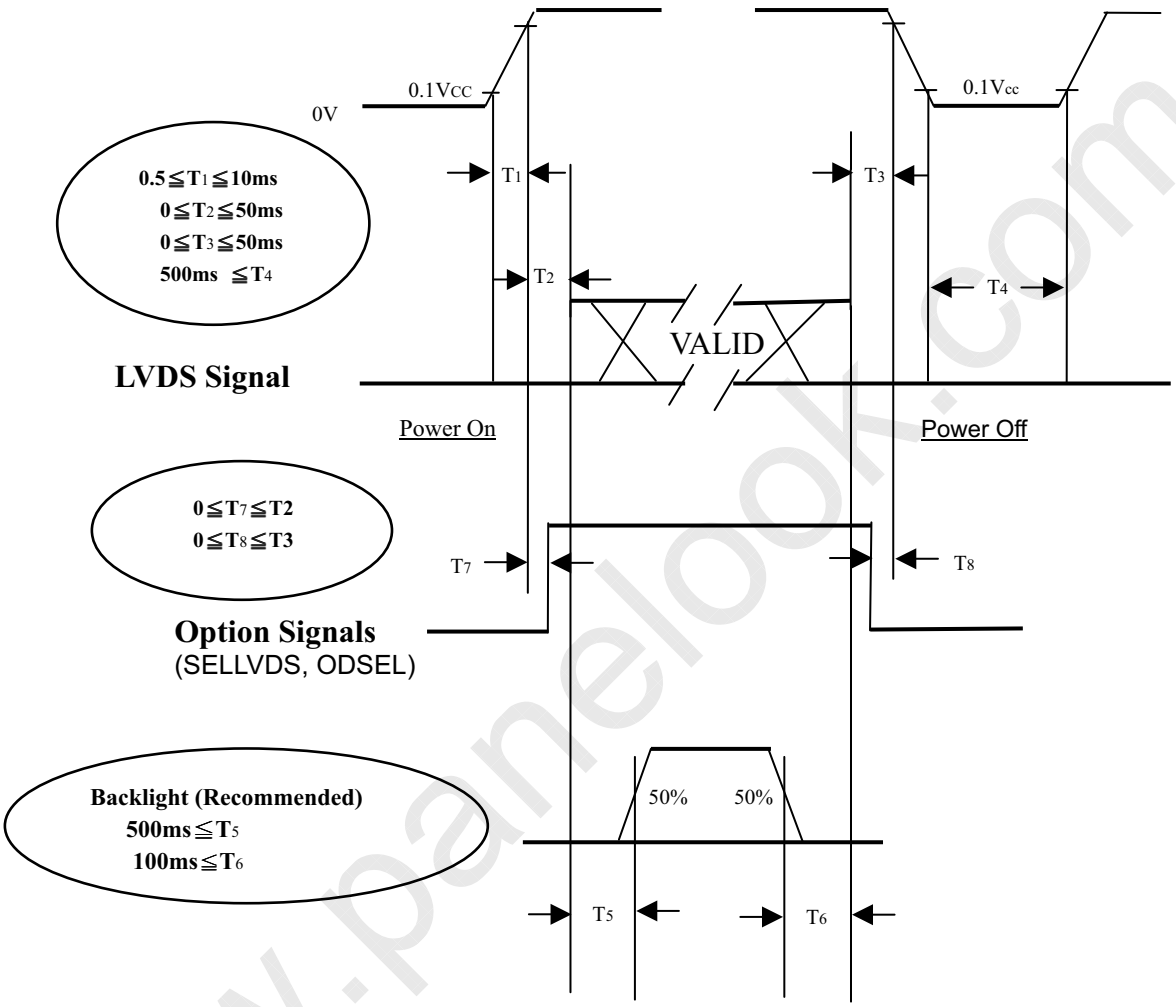


Note (6) : (ODSEL) = H/L or open for 50/60Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	11.0±0.5	mA
Oscillating Frequency (Inverter)	F_W	40±3	KHz
Vertical Frame Rate	Fr	60	Hz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (7).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing angle at normal direction	4000	6000	-	-	Note (3)
Response Time		Gray to gray		-	6.5	12	ms	Note (4)
Center Luminance of White		L_C		360	450	-	cd/m^2	Note (5)
White Variation		δW		-	-	1.3	-	Note (8)
Cross Talk		CT		-	-	4	%	Note (6)
Color Chromaticity	Red	Rcx		Typ.-0.03	0.651	Typ.+0.03	-	Note (1) Note (7)
		Rcy			0.326		-	
	Green	Gcx			0.299		-	
		Gcy			0.600		-	
	Blue	Bcx			0.145		-	
		Bcy			0.082		-	
	White	Wcx			0.329		-	
		Wcy			0.371		-	
	Color Gamut				72	-	%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	Note (2)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following :

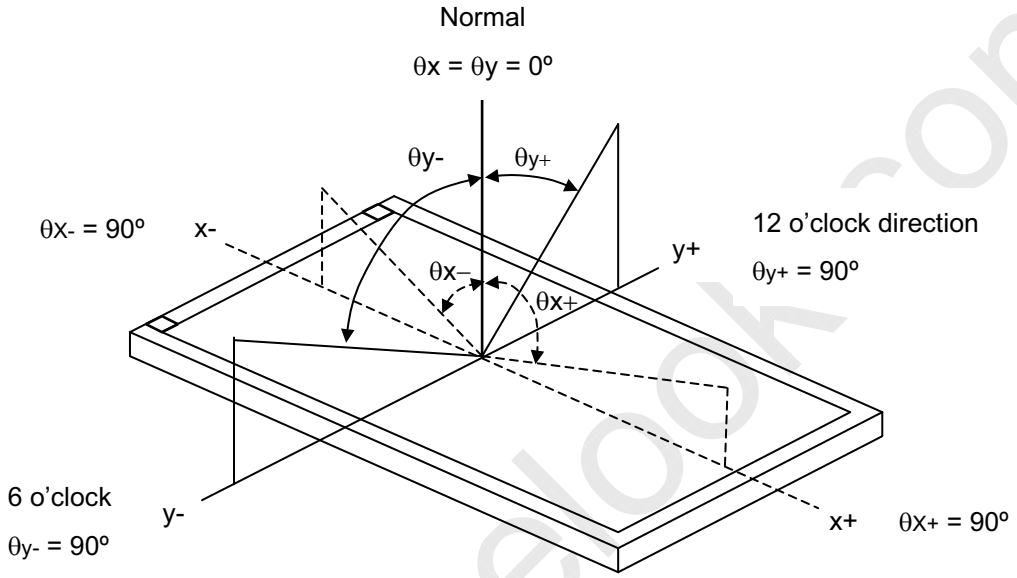
(a) Measure Module's and BLU's spectrum. BLU(for V460H1-L09) is supplied by CMO.

(b) Calculate cell's spectrum.

(c) Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (2) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

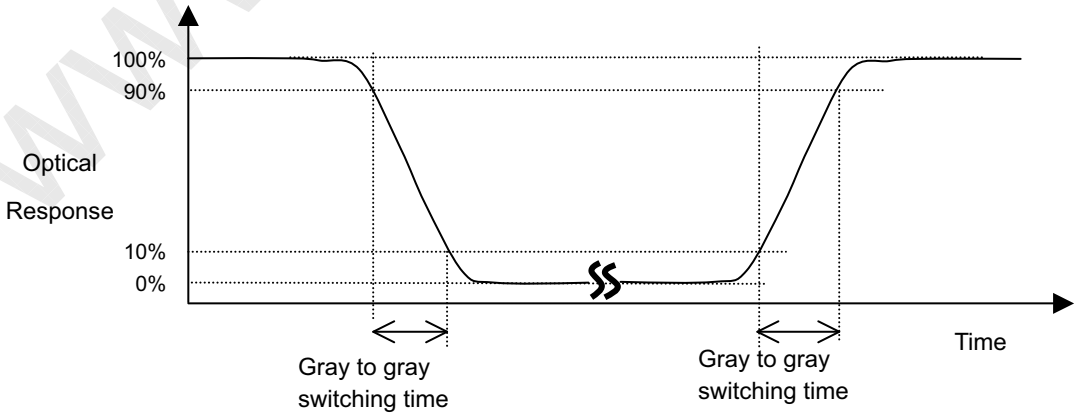
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7)

Note (4) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0 , 63, 127, 191, 255 to each other .

Note (5) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

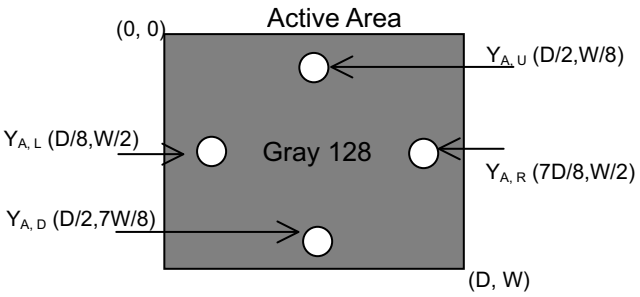
Note (6) Definition of Cross Talk (CT):

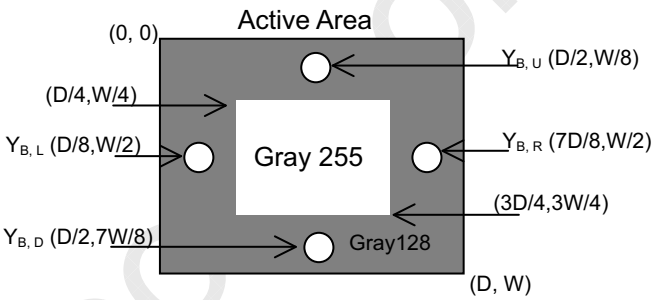
$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

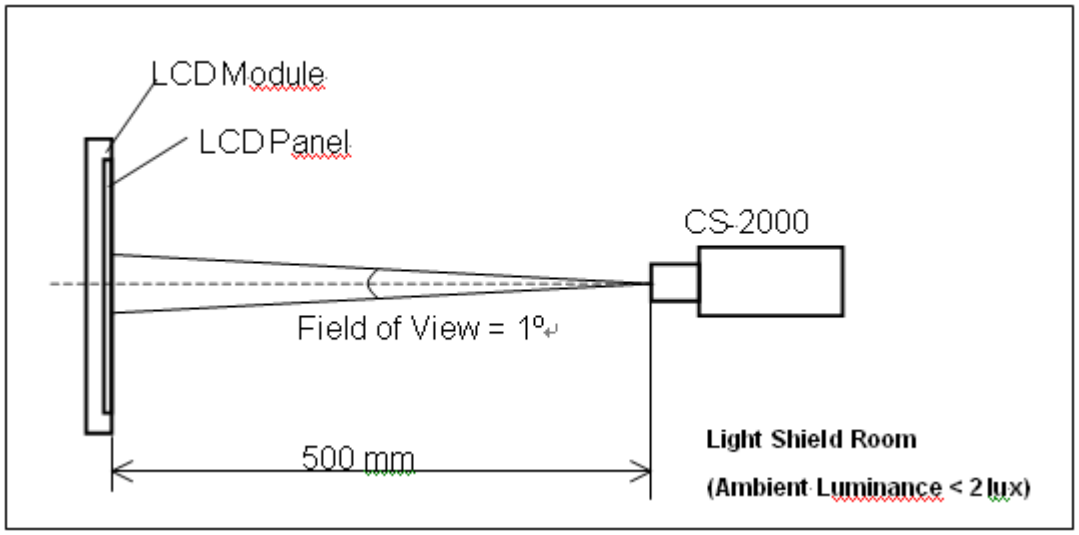
Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)





Note (7) Measurement Setup:

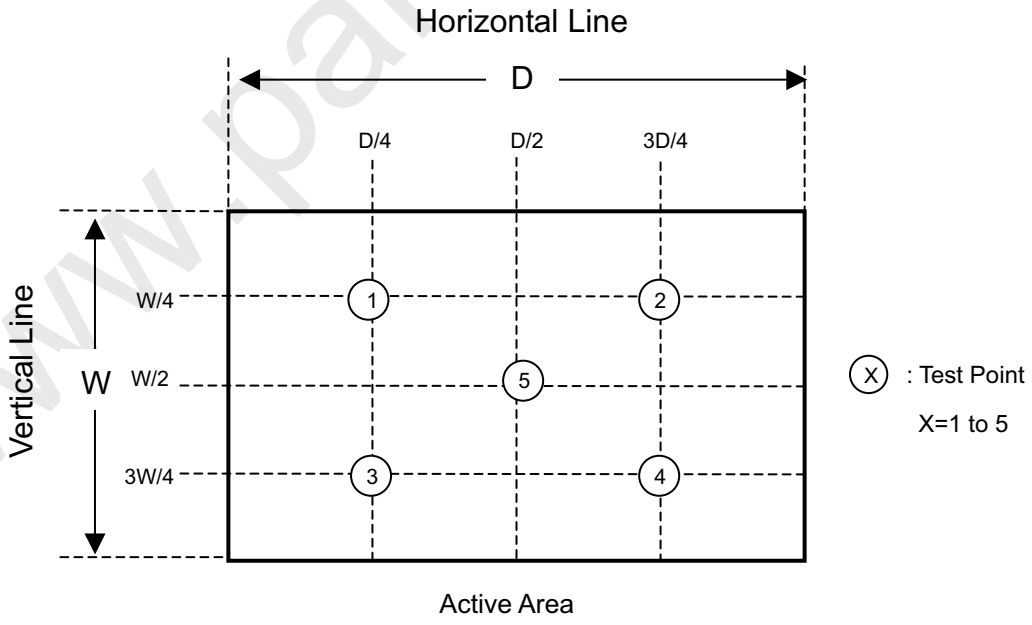
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (8) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

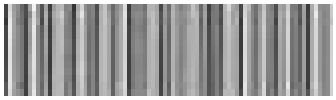


8. DEFINITION OF LABELS

8.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMO internal control.

V460H1-P09



XXXXXXXXXXXXX

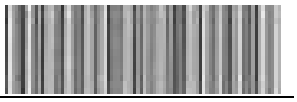
8.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation

P.O. NO._____

Parts ID._____

Carton ID._____ Quantities __8__



XXXXXXXXXXXXX

Made in Taiwan

(a) Model Name: V460H1– P09

(b) Carton ID: CMO internal control

(c) Quantities: 8

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 8 LCD TV Panels / 1 Box

(2) Box dimensions :1238 (L) X 842 (W) X 240(H)

(3) Weight : approximately 38Kg (8 panels per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

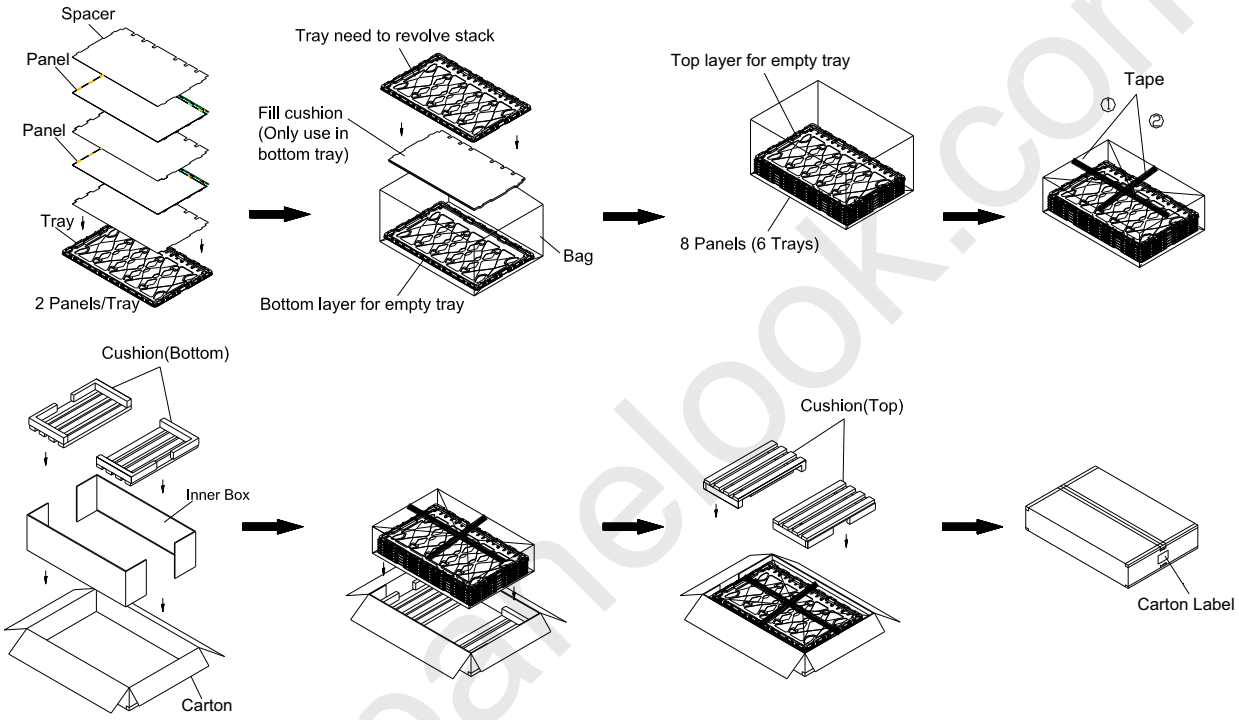
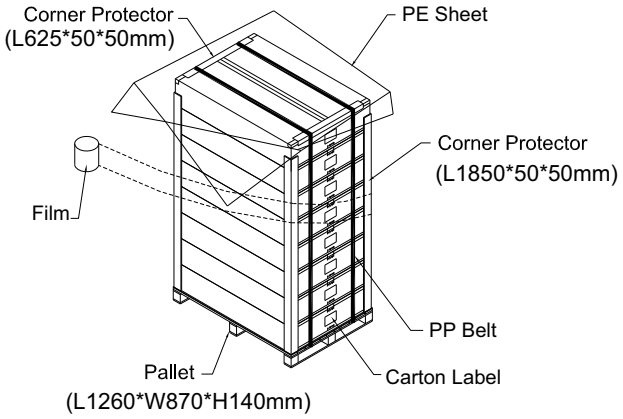


Figure.9-1 packing method

Sea & Land Transportation



Air Transportation

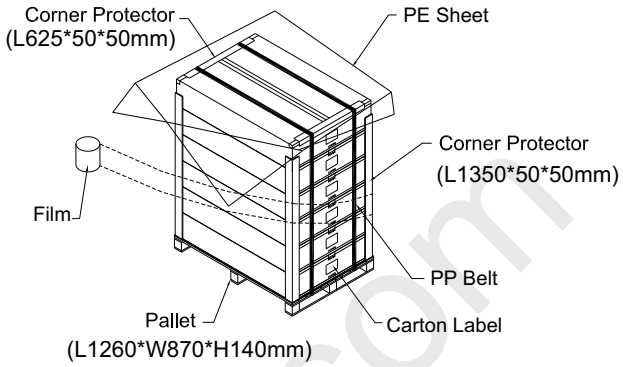


Figure.9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the product during assembly.

(2) To assemble backlight or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel will be damaged.

(4) Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(7) It is dangerous that moisture come into or contacted the product, because moisture may damage the product when it is operating.

(8) High temperature or humidity may reduce the performance of module. Please store this product within the specified storage conditions.

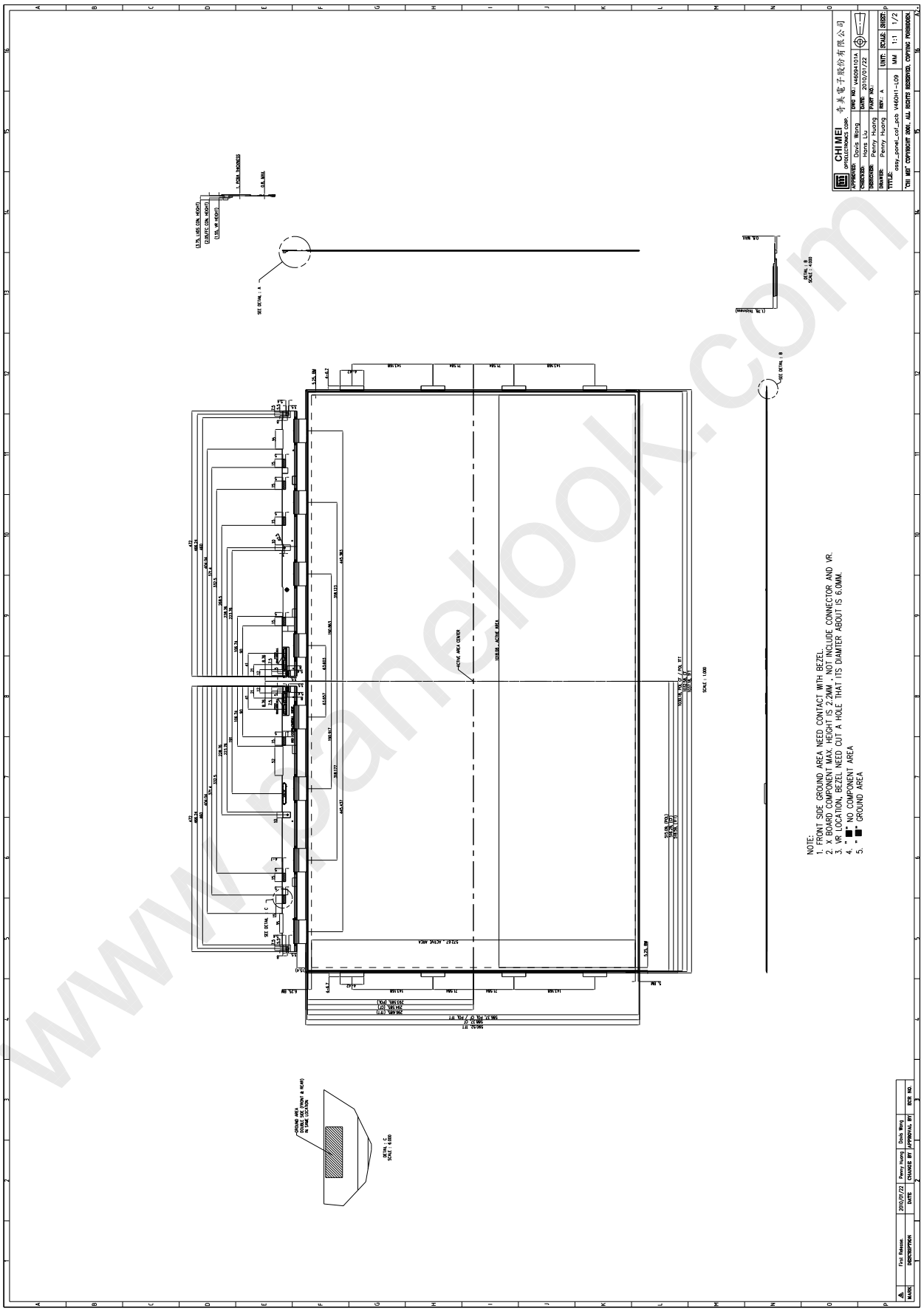
(9) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

10.2 SAFETY PRECAUTIONS

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the product's end of life, it is not harmful in case of normal operation and storage.

11. Mechanical Drawing



CHI MEI OPTOELECTRONICS CORP.

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Model No.: V460H1-P09

Approval