CHI MEI OPTOELECTRONICS CORP.

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Model No.: V460H2-LE1
Tentative

TFT LCD Approval Specification

MODEL NO.: V460H2 – LE1

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Version 0.0

CONTENTS

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 0.0	Apr. 12.'10	All	All	The Tentative Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V460H2-LE1 is a 46" TFT Liquid Crystal Display module with LED Backlight and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display true 1.07G colors (8bit+Hi-FRC -bit/color). The converter module for backlight is built-in.

1.2 FEATURES

- High brightness (450 nits)
- High contrast ratio (3000:1)
- Fast response time (Gray to gray average 5.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 240 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1018.08 (H) x 572.67 (V) (46" diagonal)	mm	(1)
Bezel Opening Area	1024.48 (H) x 578.67 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.1805 (H) x 0.5405 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	1.07G	color	
Display Operation Mode	Transmissive mode / Normally Black	-	
Surface Treatment	Anti-Glare Coating (Haze 11%) Hard Coating (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATION

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	1076.5	-	mm	(1)
	Vertical(V)	-	634.7	-	mm	
	Depth(D)		10.8		mm	To Rear
	Depth(D)		TBD		mm	To converter cover
Weight			TBD		g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	TST		-20	+60	ºC	(1)
Operating Ambient Temperature	TOP		0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	X,Y axis	-	35	G	(3), (5)
		Z axis		35	G	(3), (5)
Vibration (Non-Operating)	VNOP		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

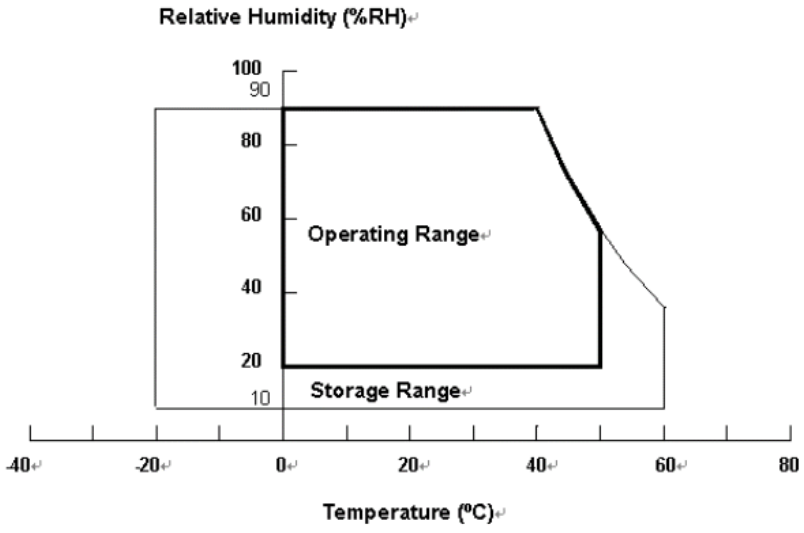
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stroed in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Light Bar Voltage	VW	–	60	V	
Converter Input Voltage	VBL	0	30	V	(1)
Control Signal Level	–	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum value s are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Contro.l Internal PWM Control and External PWM Control.

3. ELECTRICAL CHARACTERISTICS

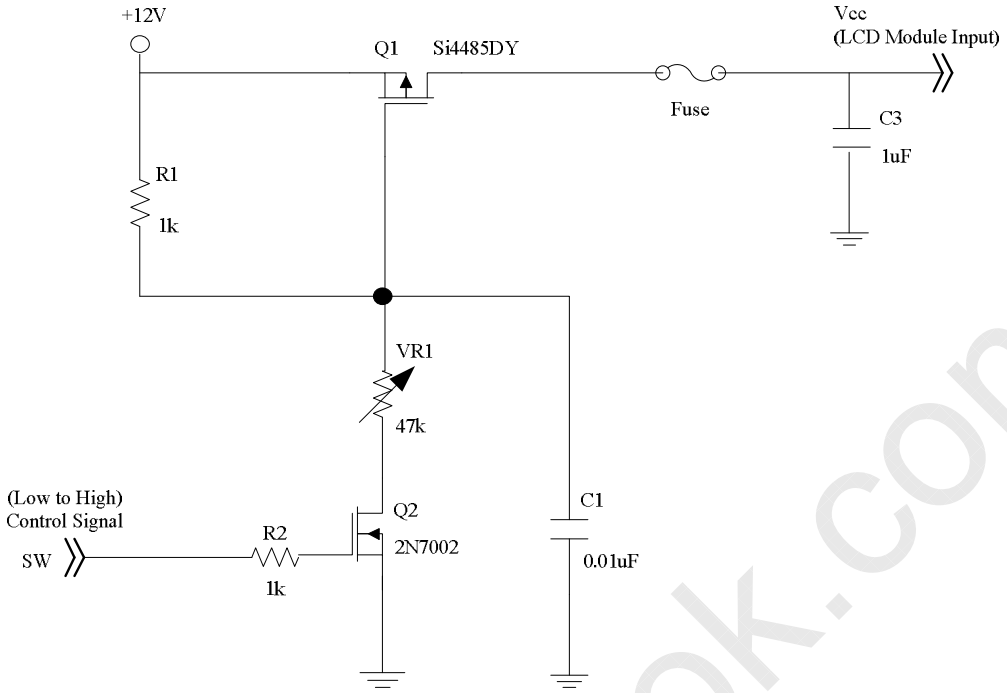
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

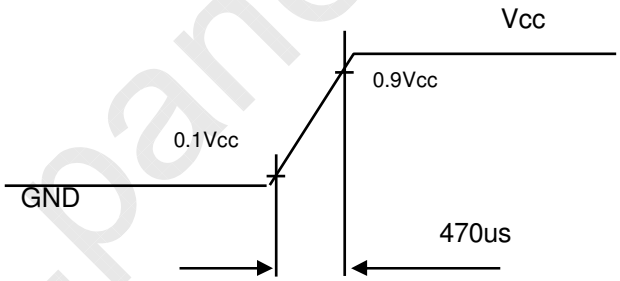
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	4	A	(2)
Power Supply Current	White Pattern	-	-	TBD		A	(3)
	Horizontal Stripe	-	-	TBD		A	
	Black Pattern	-	-	TBD		A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (Single-end)	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 240 Hz, whereas a power dissipation check pattern below is displayed.

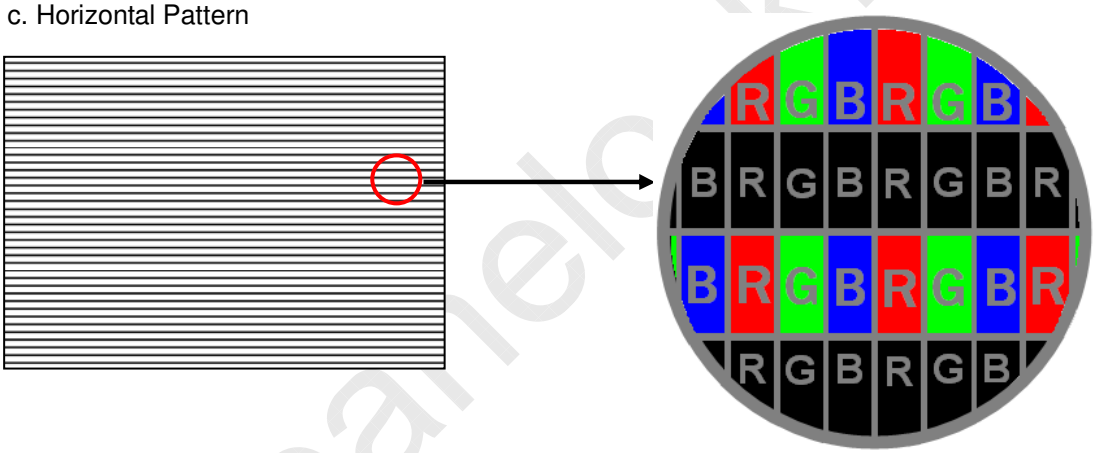
a. White Pattern

Active Area

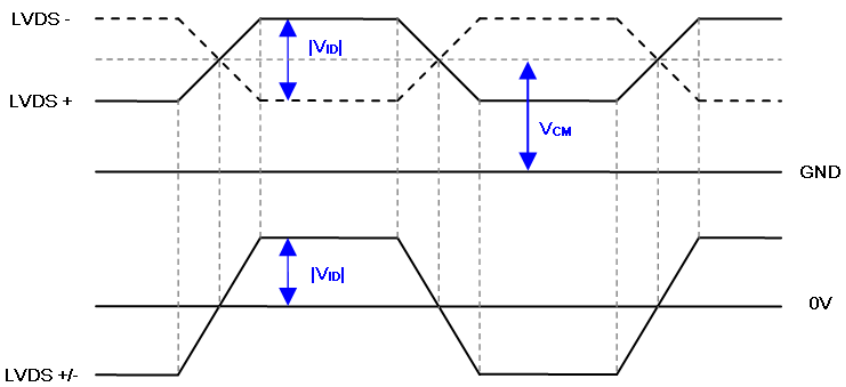
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT UNIT

3.2.1 LED CHARACTERISTICS (Ta=25± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Forward Voltage	V_W	3.0	3.2	3.5	V	I_L =120.0mA
LED Current	I_L	-	120		mA	

3.2.2 CONVERTER CHARACTERISTICS

(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	108	118.8	W	IL =120mA
Power Supply Voltage	VBL	22.8	24.0	25.2	VDC	
Power Supply Current	IBL	-	4.5	5.0	A	Non Dimming
Input Ripple Noise	-	-	-	912	mVP-P	VBL=22.8V
Dimming Frequency	FB	150	160	170	Hz	
Minimum Duty Ratio	DMIN	5	10	-	%	(2)

Note (1) The measurement condition of Max. value is based on 46" backlight unit under input voltage 24V, average LED current 120mA and lighting 30 minutes later.

Note (2) **5%** minimum duty ratio is only valid for electrical operation.

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	2.85	3.0	3.15	V	maximum duty ratio
	MIN		—	—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on
	LO		—	0	—	0.8	V	Duty off
Status Signal	HI	Status	—	3.0	3.3	3.6	V	Normal
	LO		—	0	—	0.8	V	Abnormal
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V_{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		TPWMR	—	—	—	50	us	
PWM Signal Falling Time		TPWMF	—	—	—	50	us	
Input Impedance		Rin	—	1	—	—	MΩ	
PWM Delay Time		TPWM	—	100	—	—	ms	
BLON Delay Time		T_{on}	—	300	—	—	ms	
		T_{on1}	—	300	—	—	ms	
BLON Off Time		Toff	—	300	—	—	ms	

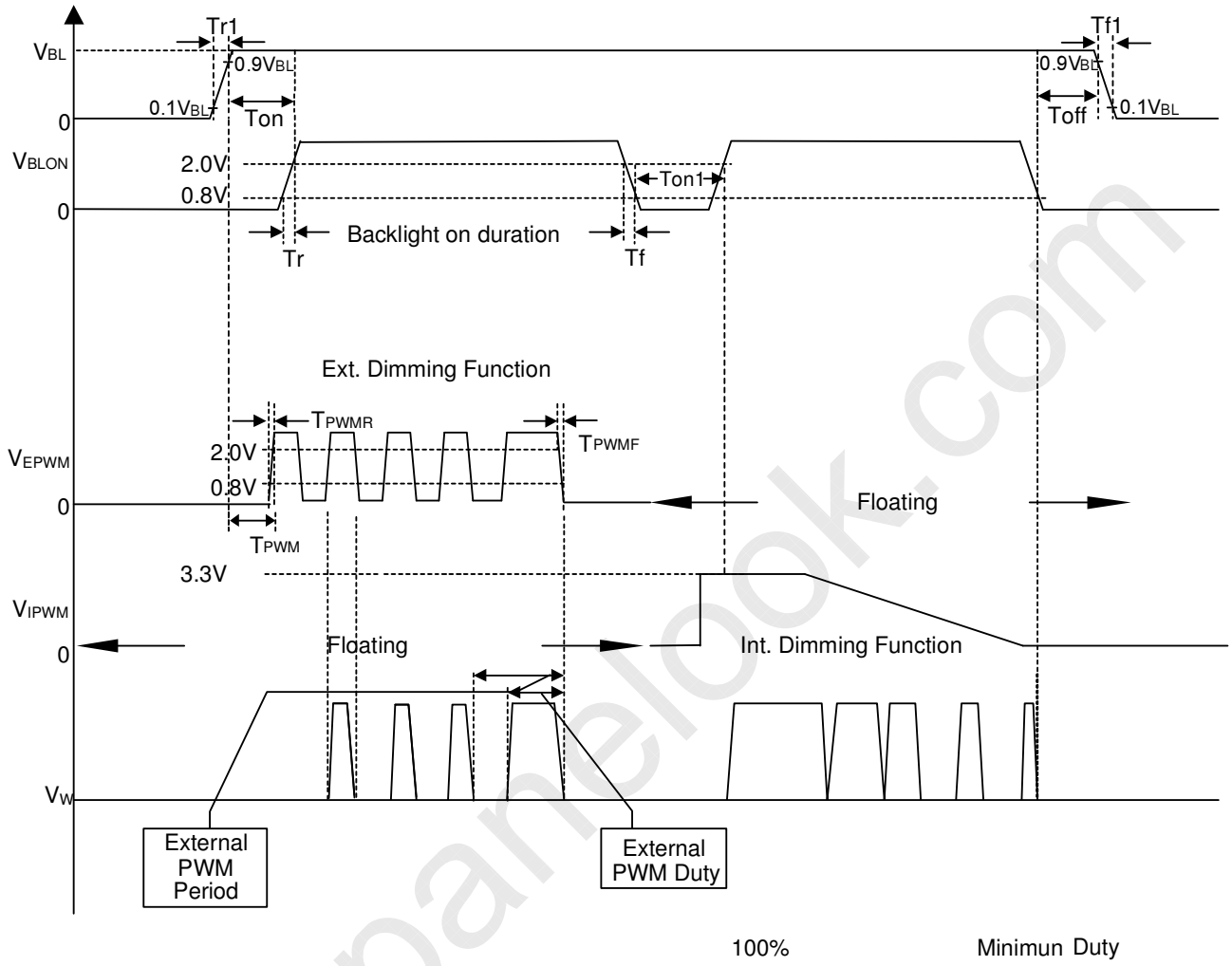
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

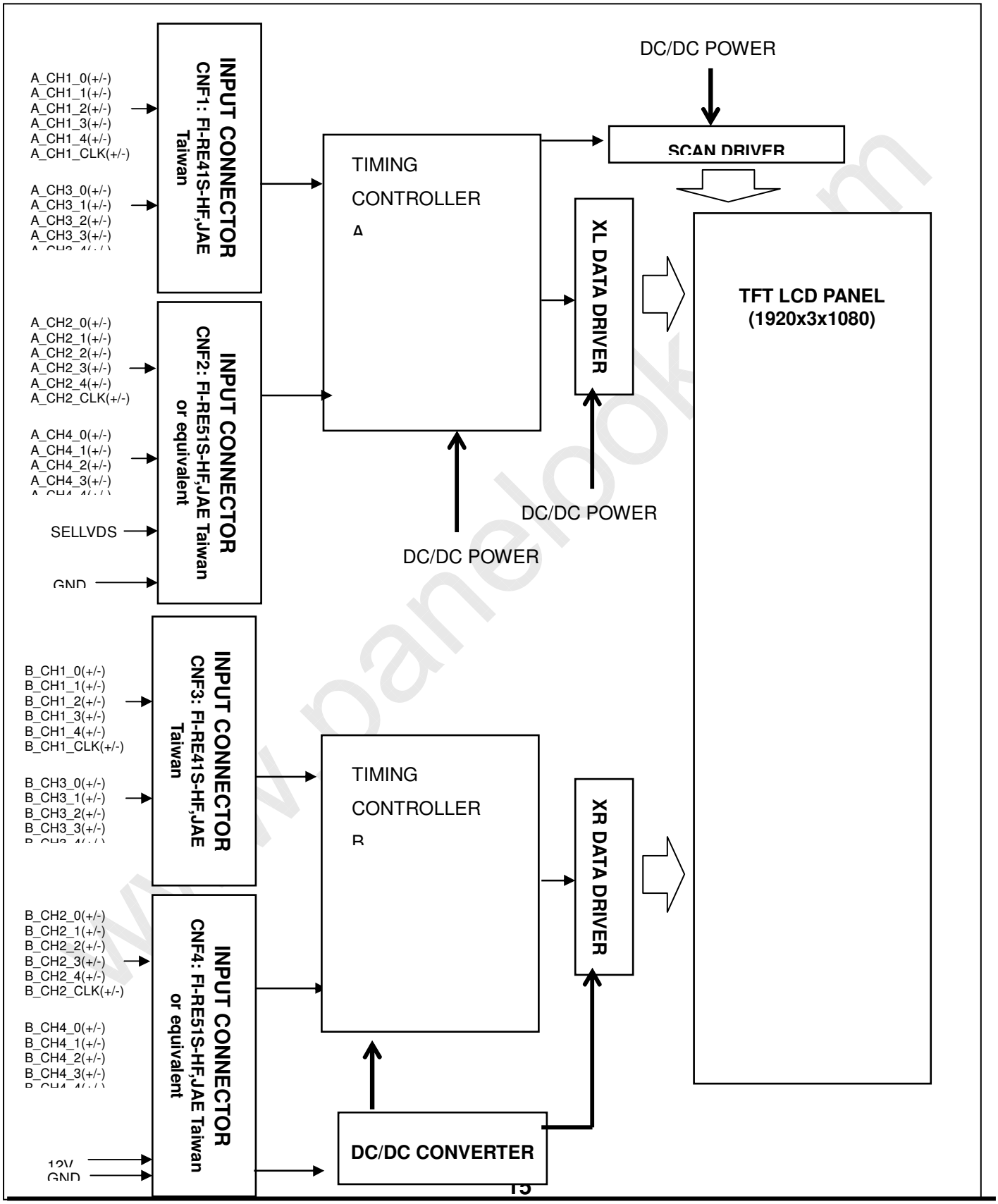
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Pin Assignment (FI-RE41S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	A_CH1[0]-	First pixel of A source. Negative LVDS differential data input. Pair 0	
11	A_CH1[0]+	First pixel of A source. Positive LVDS differential data input. Pair 0	
12	A_CH1[1]-	First pixel of A source. Negative LVDS differential data input. Pair 1	
13	A_CH1[1]+	First pixel of A source. Positive LVDS differential data input. Pair 1	
14	A_CH1[2]-	First pixel of A source. Negative LVDS differential data input. Pair l 2	
15	A_CH1[2]+	First pixel of A source. Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	A_CH1CLK-	First pixel of A source. Negative LVDS differential clock input.	
18	A_CH1CLK+	First pixel of A source. Positive LVDS differential clock input.	
19	GND	Ground	
20	A_CH1[3]-	First pixel of A source. Negative LVDS differential data input. Pair 3	
21	A_CH1[3]+	First pixel of A source. Positive LVDS differential data input. Pair 3	
22	A_CH1[4]-	First pixel of A source. Negative LVDS differential data input. Pair 4	
23	A_CH1[4]+	First pixel of A source. Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	A_CH3[0]-	Third pixel of A source. Negative LVDS differential data input. Pair 0	
26	A_CH3[0]+	Third pixel of A source. Positive LVDS differential data input. Pair 0	
27	A_CH3[1]-	Third pixel of A source. Negative LVDS differential data input. Pair 1	

28	A_CH3[1]+	Third pixel of A source. Positive LVDS differential data input. Pair 1	
29	A_CH3[2]-	Third pixel of A source. Negative LVDS differential data input. Pair 2	
30	A_CH3[2]+	Third pixel of A source. Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	A_CH3CLK-	Third pixel of A source. Negative LVDS differential clock input.	
33	A_CH3CLK+	Third pixel of A source. Positive LVDS differential clock input.	
34	GND	Ground	
35	A_CH3[3]-	Third pixel of A source. Negative LVDS differential data input. Pair 3	
36	A_CH3[3]+	Third pixel of A source. Positive LVDS differential data input. Pair 3	
37	A_CH3[4]-	Third pixel of A source. Negative LVDS differential data input. Pair 4	
38	A_CH3[4]+	Third pixel of A source. Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	GND	Ground	
41	GND	Ground	

CNF2 Connector Pin Assignment (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	A_CH2[0]-	Second pixel of A source. Negative LVDS differential data input. Pair 0	
11	A_CH2[0]+	Second pixel of A source. Positive LVDS differential data input. Pair 0	
12	A_CH2[1]-	Second pixel of A source. Negative LVDS differential data input. Pair 1	
13	A_CH2[1]+	Second pixel of A source. Positive LVDS differential data input. Pair 1	
14	A_CH2[2]-	Second pixel of A source. Negative LVDS differential data input. Pair 2	

15	A_CH2[2]+	Second pixel of A source. Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	A_CH2CLK-	Second pixel of A source. Negative LVDS differential clock input.	
18	A_CH2CLK+	Second pixel of A source. Positive LVDS differential clock input.	
19	GND	Ground	
20	A_CH2[3]-	Second pixel of A source. Negative LVDS differential data input. Pair 3	
21	A_CH2[3]+	Second pixel of A source. Positive LVDS differential data input. Pair 3	
22	A_CH2[4]-	Second pixel of A source. Negative LVDS differential data input. Pair 4	
23	A_CH2[4]+	Second pixel of A source. Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	A_CH4[0]-	Fourth pixel of A source Negative LVDS differential data input. Pair 0	
26	A_CH4[0]+	Fourth pixel of A source Positive LVDS differential data input. Pair 0	
27	A_CH4[1]-	Fourth pixel of A source Negative LVDS differential data input. Pair 1	
28	A_CH4[1]+	Fourth pixel of A source Positive LVDS differential data input. Pair 1	
29	A_CH4[2]-	Fourth pixel of A source Negative LVDS differential data input. Pair 2	
30	A_CH4[2]+	Fourth pixel of A source Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	A_CH4CLK-	Fourth pixel of A source Negative LVDS differential clock input.	
33	A_CH4CLK+	Fourth pixel of A source Positive LVDS differential clock input.	
34	GND	Ground	
35	A_CH4[3]-	Fourth pixel of A source Negative LVDS differential data input. Pair 3	
36	A_CH4[3]+	Fourth pixel of A source Positive LVDS differential data input. Pair 3	
37	A_CH4[4]-	Fourth pixel of A source Negative LVDS differential data input. Pair 4	
38	A_CH4[4]+	Fourth pixel of A source Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	SCL_I	No Connection	
41	GND	Ground	
42	C_LUT1	No Connection	
43	TCON_WP	No Connection	

44	SDA_I	No Connection	
45	GMA_SEL	No Connection	
46	C_TST_AGE	No Connection	
47	A_SCL	No Connection	
48	A_SDA	No Connection	
49	GND	Ground	
50	C_SEL_POL	No Connection	
51	LVDS_SEL	LVDS data format Selection (0V~0.7V/OPEN→VESA, 2.7V~3.3V→ JEIDA)	

CNF3 Connector Pin Assignment (FI-RE41S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	B_CH1[0]-	First pixel of B source. Negative LVDS differential data input. Pair 0	
11	B_CH1[0]+	First pixel of B source. Positive LVDS differential data input. Pair 0	
12	B_CH1[1]-	First pixel of B source. Negative LVDS differential data input. Pair 1	
13	B_CH1[1]+	First pixel of B source. Positive LVDS differential data input. Pair 1	
14	B_CH1[2]-	First pixel of B source. Negative LVDS differential data input. Pair l 2	
15	B_CH1[2]+	First pixel of B source. Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	B_CH1CLK-	First pixel of B source. Negative LVDS differential clock input.	
18	B_CH1CLK+	First pixel of B source. Positive LVDS differential clock input.	
19	GND	Ground	
20	B_CH1[3]-	First pixel of B source. Negative LVDS differential data input. Pair 3	

21	B_CH1[3]+	First pixel of B source. Positive LVDS differential data input. Pair 3	
22	B_CH1[4]-	First pixel of B source. Negative LVDS differential data input. Pair 4	
23	B_CH1[4]+	First pixel of B source. Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	B_CH3[0]-	Third pixel of B source. Negative LVDS differential data input. Pair 0	
26	B_CH3[0]+	Third pixel of B source. Positive LVDS differential data input. Pair 0	
27	B_CH3[1]-	Third pixel of B source. Negative LVDS differential data input. Pair 1	
28	B_CH3[1]+	Third pixel of B source. Positive LVDS differential data input. Pair 1	
29	B_CH3[2]-	Third pixel of B source. Negative LVDS differential data input. Pair 2	
30	B_CH3[2]+	Third pixel of B source. Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	B_CH3CLK-	Third pixel of B source. Negative LVDS differential clock input.	
33	B_CH3CLK+	Third pixel of B source. Positive LVDS differential clock input.	
34	GND	Ground	
35	B_CH3[3]-	Third pixel of B source. Negative LVDS differential data input. Pair 3	
36	B_CH3[3]+	Third pixel of B source. Positive LVDS differential data input. Pair 3	
37	B_CH3[4]-	Third pixel of B source. Negative LVDS differential data input. Pair 4	
38	B_CH3[4]+	Third pixel of B source. Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	GND	Ground	
41	GND	Ground	

CNF4 Connector Pin Assignment (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	GND	Ground	
7	GND	Ground	

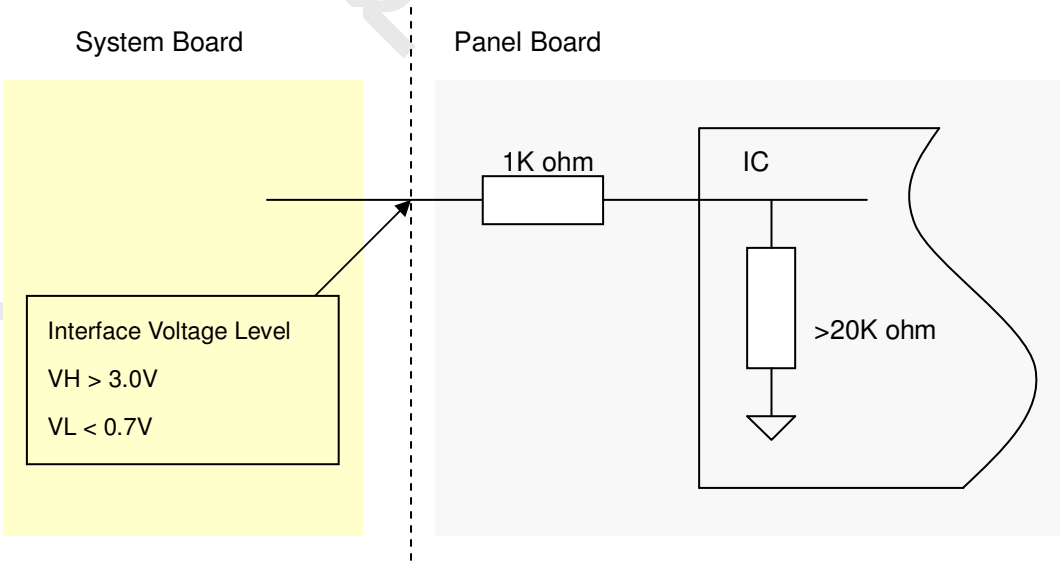
8	GND	Ground	
9	GND	Ground	
10	B_CH2[0]-	Second pixel of B source. Negative LVDS differential data input. Pair 0	
11	B_CH2[0]+	Second pixel of B source. Positive LVDS differential data input. Pair 0	
12	B_CH2[1]-	Second pixel of B source. Negative LVDS differential data input. Pair 1	
13	B_CH2[1]+	Second pixel of B source. Positive LVDS differential data input. Pair 1	
14	B_CH2[2]-	Second pixel of B source. Negative LVDS differential data input. Pair 2	
15	B_CH2[2]+	Second pixel of B source. Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	B_CH2CLK-	Second pixel of B source. Negative LVDS differential clock input.	
18	B_CH2CLK+	Second pixel of B source. Positive LVDS differential clock input.	
19	GND	Ground	
20	B_CH2[3]-	Second pixel of B source. Negative LVDS differential data input. Pair 3	
21	B_CH2[3]+	Second pixel of B source. Positive LVDS differential data input. Pair 3	
22	B_CH2[4]-	Second pixel of B source. Negative LVDS differential data input. Pair 4	
23	B_CH2[4]+	Second pixel of B source. Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	B_CH4[0]-	Fourth pixel of B source. Negative LVDS differential data input. Pair 0	
26	B_CH4[0]+	Fourth pixel of B source. Positive LVDS differential data input. Pair 0	
27	B_CH4[1]-	Fourth pixel of B source. Negative LVDS differential data input. Pair 1	
28	B_CH4[1]+	Fourth pixel of B source. Positive LVDS differential data input. Pair 1	
29	B_CH4[2]-	Fourth pixel of B source. Negative LVDS differential data input. Pair 2	
30	B_CH4[2]+	Fourth pixel of B source. Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	B_CH4CLK-	Fourth pixel of B source. Negative LVDS differential clock input.	
33	B_CH4CLK+	Fourth pixel of B source. Positive LVDS differential clock input.	
34	GND	Ground	
35	B_CH4[3]-	Fourth pixel of B source. Negative LVDS differential data input. Pair 3	
36	B_CH4[3]+	Fourth pixel of B source. Positive LVDS differential data input. Pair 3	

37	B_CH4[4]-	Fourth pixel of B source. Negative LVDS differential data input. Pair 4	
38	B_CH4[4]+	Fourth pixel of B source. Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	N.C.	No Connection	
41	GND	Ground	
42	N240_SYNC_ ASIC	No Connection	
43	N240_EN	No Connection	
44	N.C.	No Connection	
45	TCK	No Connection	
46	TDO	No Connection	
47	TMS	No Connection	
48	TDI	No Connection	
49	GND	Ground	
50	V33F	No Connection	
51	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) High=connect to +3.3V : JEIDA Format ； Low= connect to GND or Open : VESA Format.

Note (3) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.

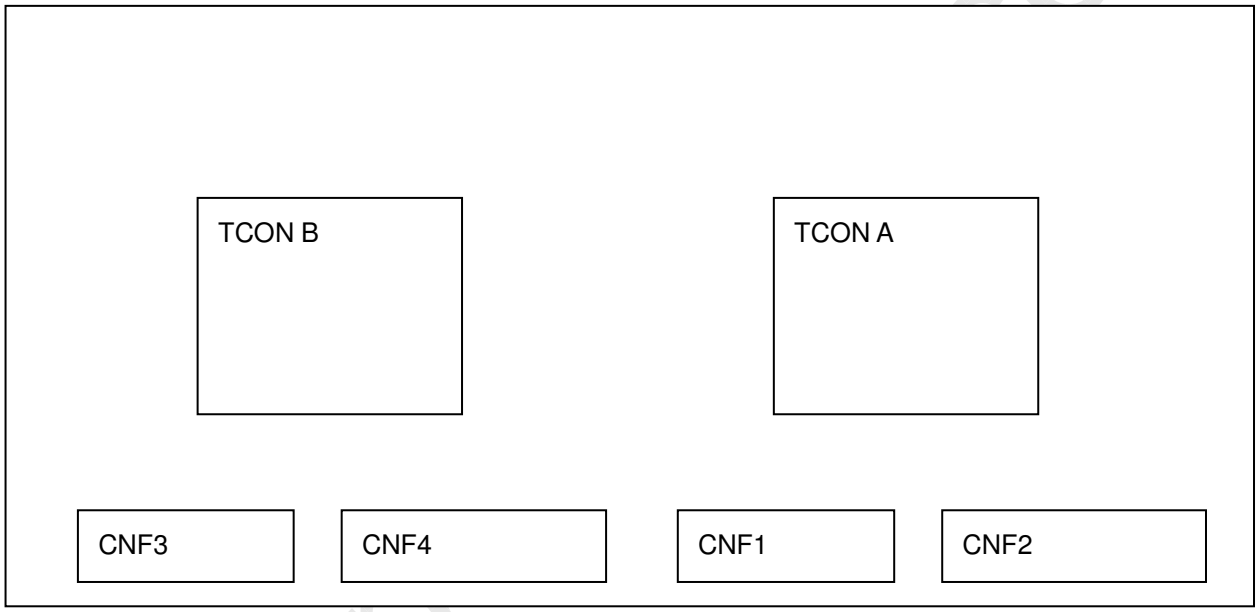


Note (4) LVDS 4-port of 1 source Data Mapping

Port	CH of LVDS	Data Stream
Port 1	1st pixel	1, 3, 5, ..., 1917, 1919
Port 2	2nd pixel	2, 4, 6, ..., 1918, 1920
Port 3	1st pixel	1, 3, 5, ..., 1917, 1919
Port 4	2nd pixel	2, 4, 6, ..., 1918, 1920

Note (3) I2C Clock and Data interface

Connectors on Control Board Arrangement:



5.2 CONVERTER UNIT

CN1: CI0114M1HR0-LF (CvilLux) or equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	STATUS	Normal (3.3V) Abnormal(GND)
12	E_PWM	External PWM Control Signal
13	I_PWM	Internal PWM Control Signal
14	BLON	BL ON/OFF

Note (1) Pin 12: External PWM control (use pin 12): Pin 13 must open.

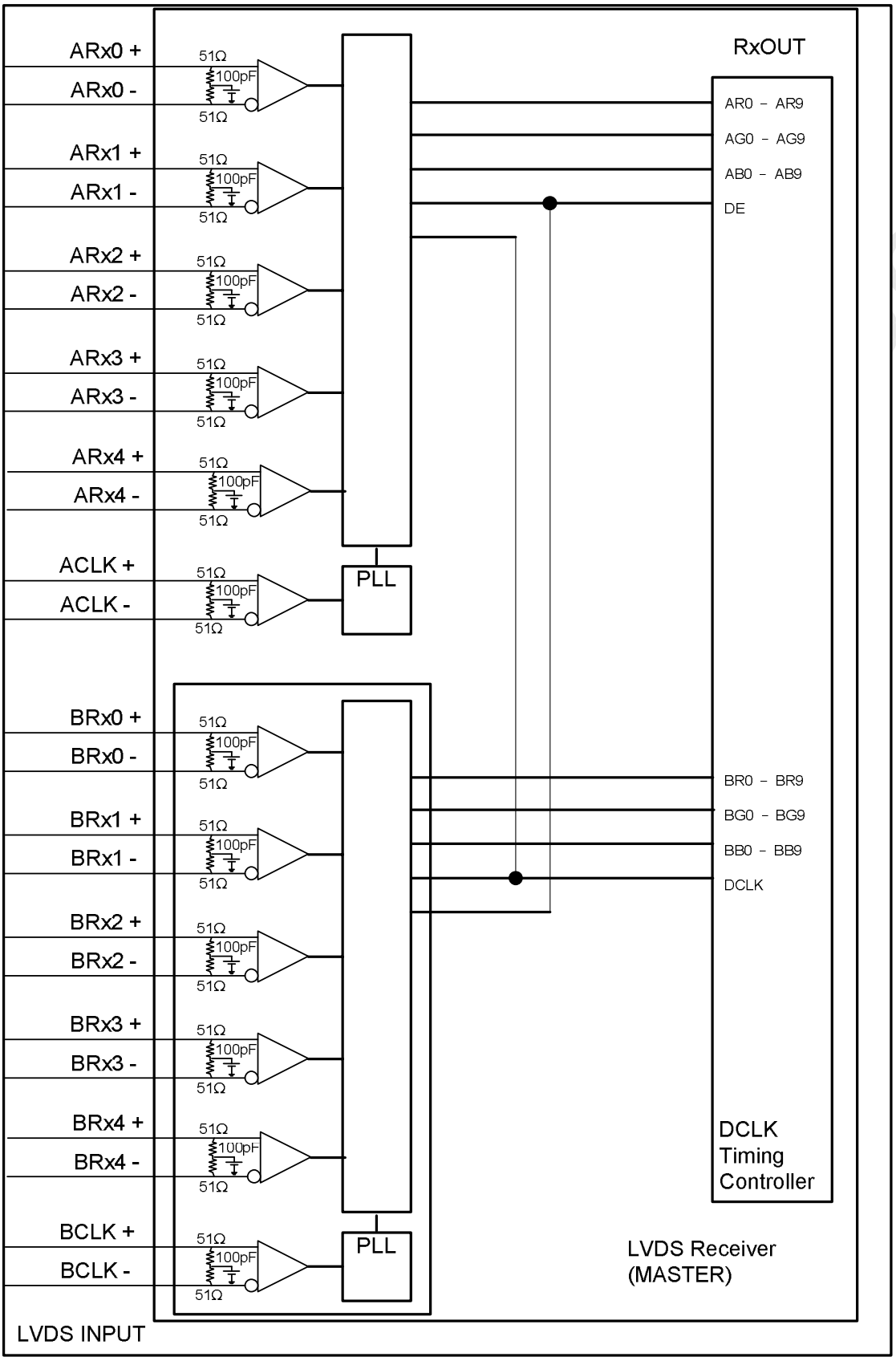
Note (2) Pin 13: Internal PWM control (use pin 13): Pin 12 must open.

Note (3) Pin 12 and Pin 13 can't open in the same period.

CN2~CN5: 51281-1094 (Molex) ,187059-51221 (P-TWO),7083K-F10N-00L (E&T)

Pin №	Symbol	Feature	NOTE
1	VLED	Positive of LED String	
2	VLED		
3	NC	No Connection	
4	NC		
5	NC		
6	N1	Negative of LED String	
7	N2		
8	N3		
9	N4		
10	N5		

5.3 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR9: Third pixel R data

CG0~CG9: Third pixel G data

CB0~CB9: Third pixel B data

DR0~DR9: Fourth pixel R data

DG0~DG9: Fourth pixel G data

DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

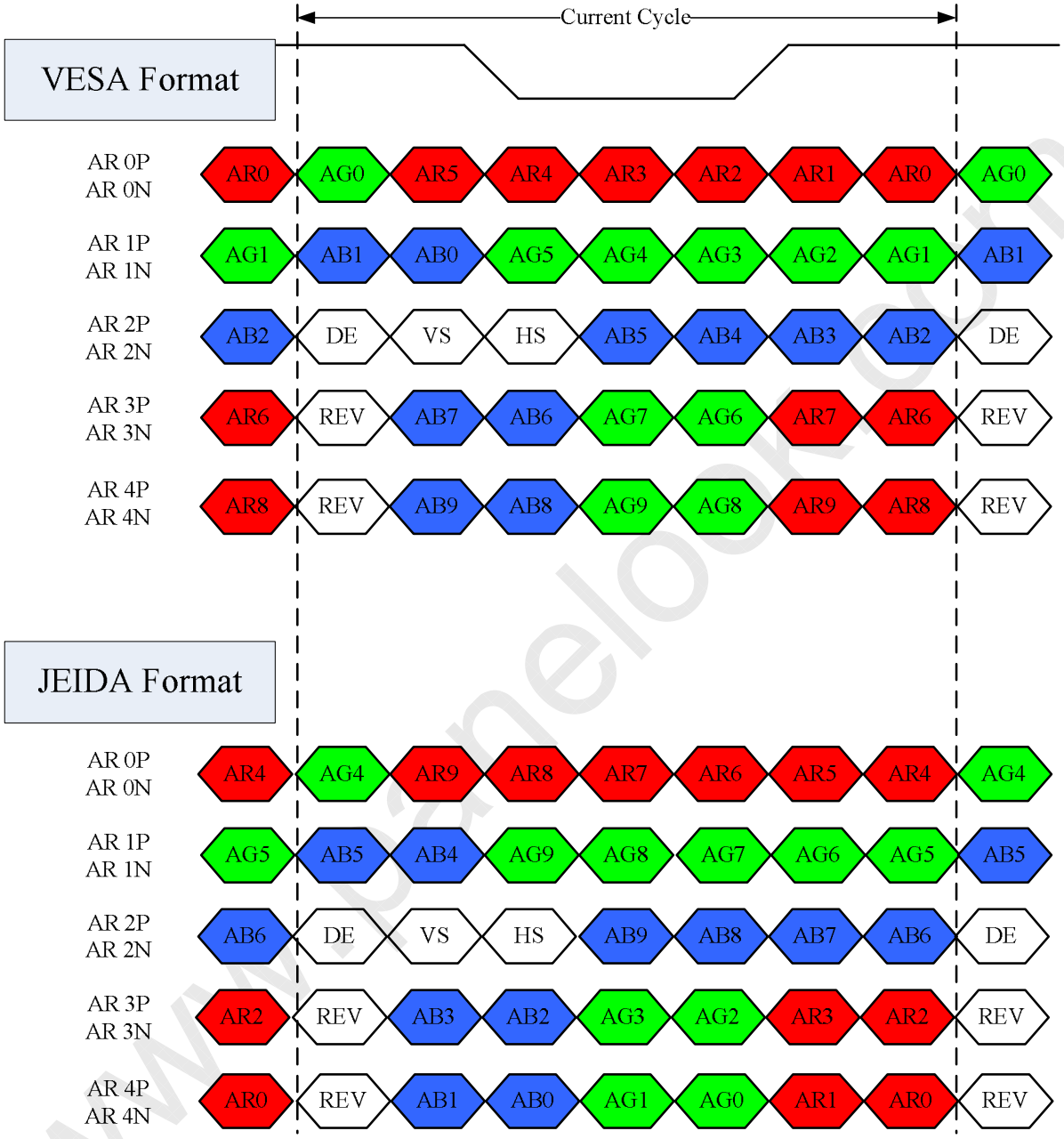
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.4 LVDS INTERFACE

VESA Format : SELLVDS = H or Open

JEIDA Format : SELLVDS = L



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE: Data enable signal

DCLK: Data clock signal

RSV: Reserved

5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0)/ Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (2)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green (1023)																														
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	97	100	103	Hz	(6)
		F_{r6}	117	120	123	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	—
	Blank	Thb	60	70	95	Tc	—

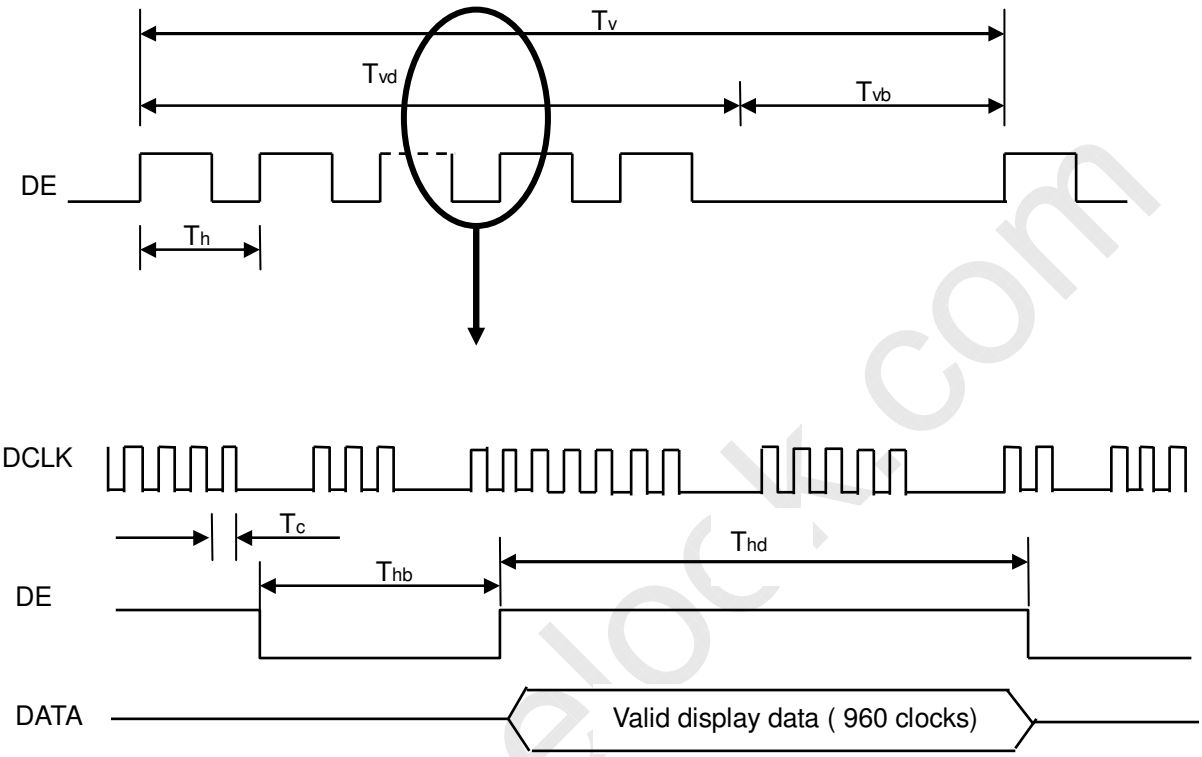
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

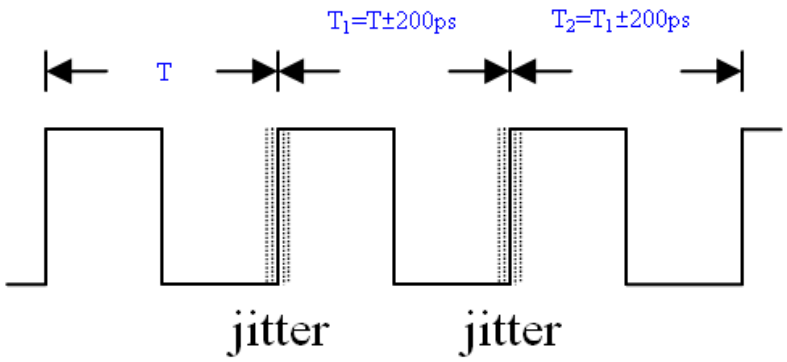
$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

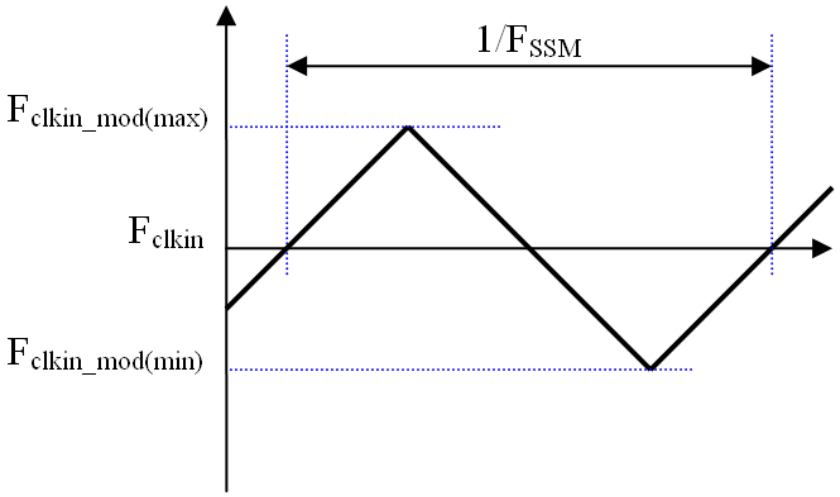
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

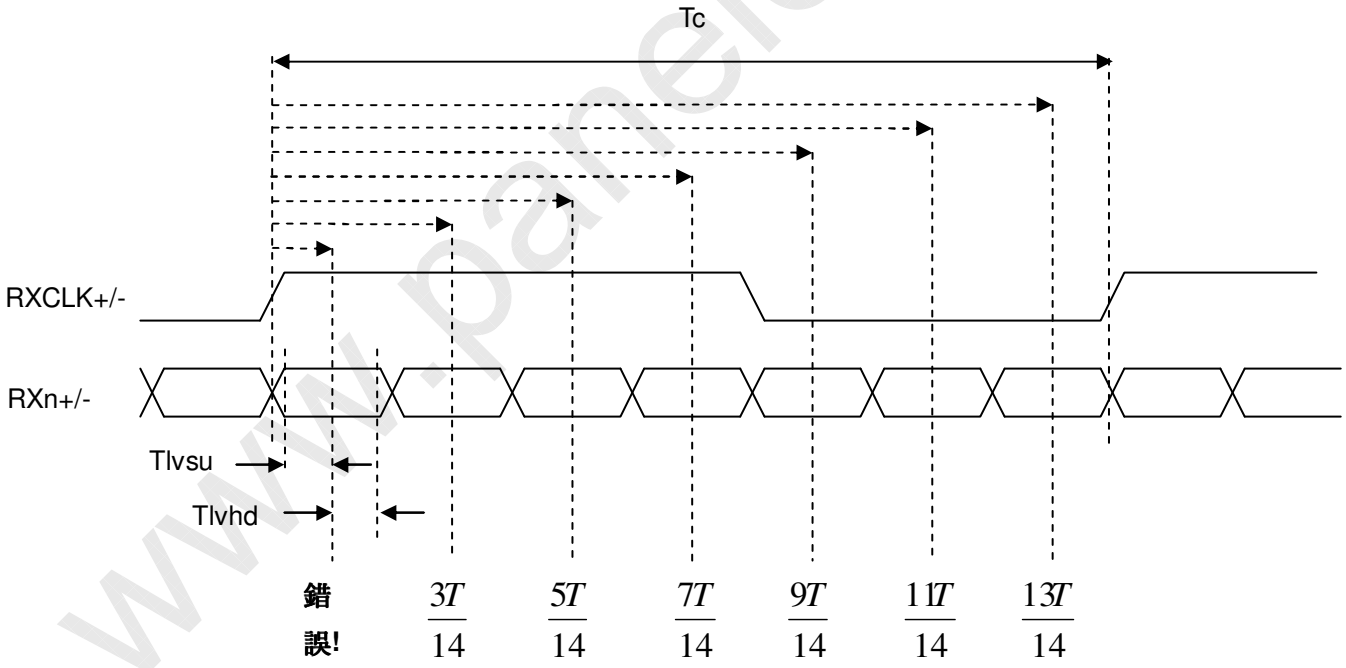


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) : (ODSEL) = H/L or open for 100/120Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

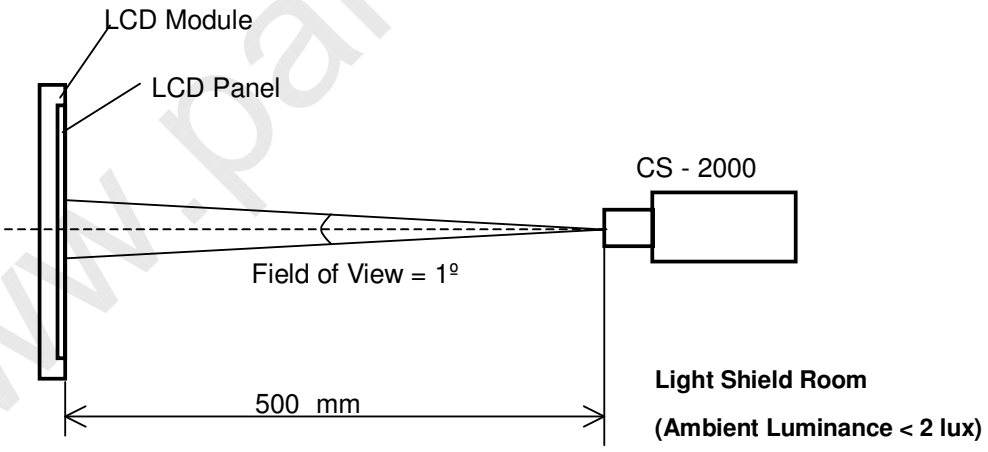
TBD

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	120 ±3.6	mA
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



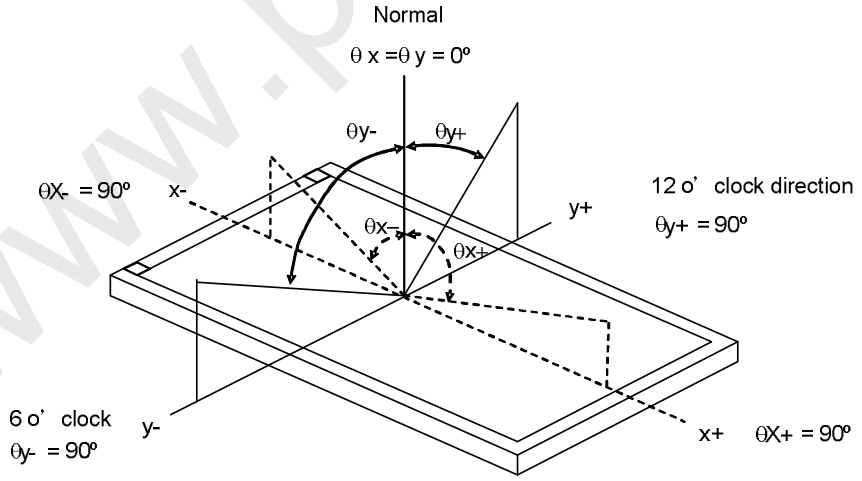
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing angle at normal direction	2000	3000	-	-	Note (2)
Response Time		Gray to gray		-	TBD		ms	Note (3)
Center Luminance of White		L_C			450	-	cd/m^2	Note (4)
White Variation		δW		-	-	1.3	-	Note (6)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ.-0.03	TBD	Typ.+0.03	-	
		Ry			TBD		-	
	Green	Gx			TBD		-	
		Gy			TBD		-	
	Blue	Bx			TBD		-	
		By			TBD		-	
	White	Wx			TBD		-	
		Wy			TBD		-	
	Color Gamut				72	-	%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	Note (1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR):

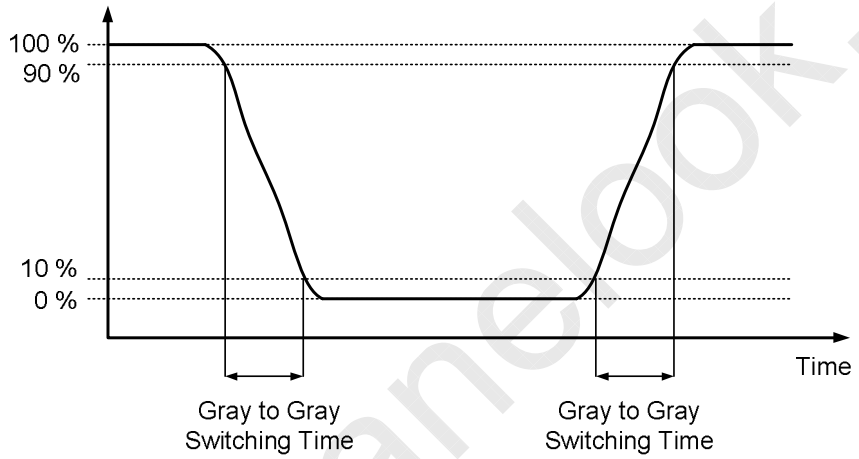
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:

Optical Response



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892, and 1023.Gray to gray. Average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892, and 1023 to each other.

Note (4) Definition of Luminance of White (LC):

Measure the luminance of gray level 1023 at center point and 5 points

LC = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

Note (5) Definition of Cross Talk (CT):

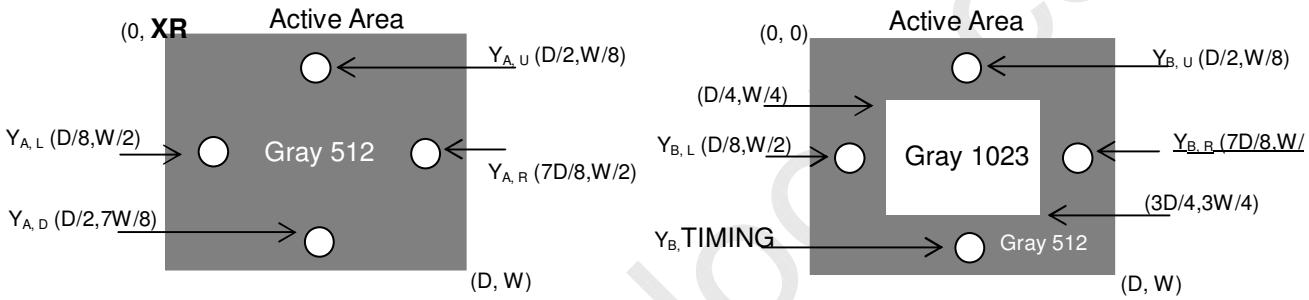
$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

(a)

Y_A = Luminance of measured location without gray level 1023 pattern (cd/m^2)

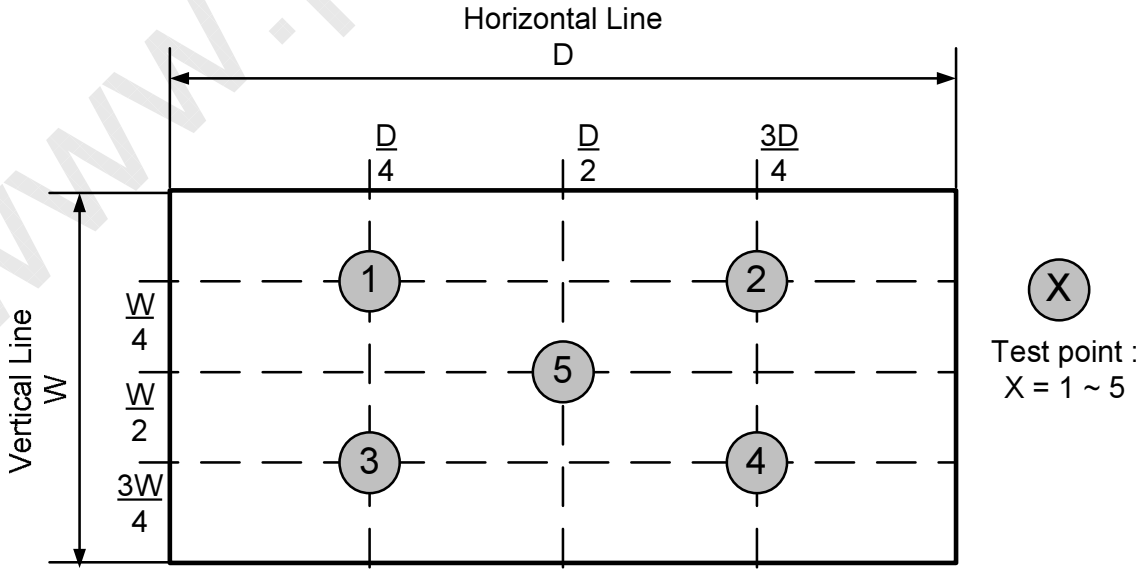
Y_B = Luminance of measured location with gray level 1023 pattern (cd/m^2)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

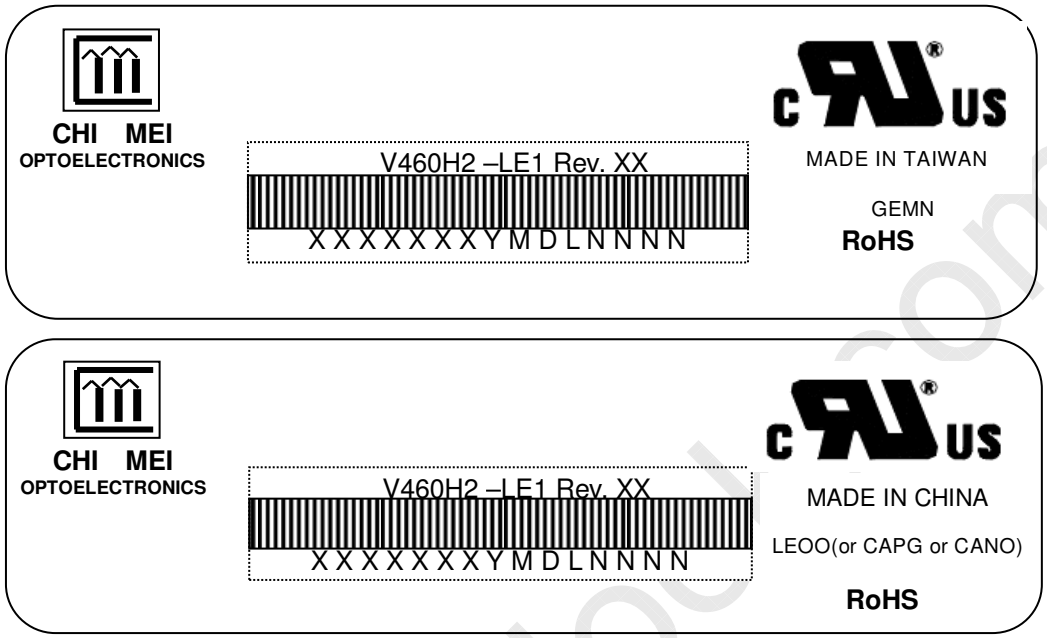
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V460H2-LE1

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- CMO Internal Use
- CMO Internal Use
- Revision
- CMO Internal Use

Serial ID includes the information as below:

Manufactured Date:

Year: 2001=1,2002=2,2003=3,2004=4…2010=0,2011=1,2012=2..

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

TBD

11. MECHANICAL CHARACTERISTICS

TBD